# THRESHOLD™

The EOS/ESD Association, Inc. newsletter, published for everyone with an interest in the understanding and control of electrostatic discharge.

EOS/ESD Association, Inc.
*Setting the Global Standards for Static Control!*

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WWW.ESDA.ORG


## You are invited to attend the ***New*** Emerging Technology Seminars, Monday September 8th at This Year's Annual EOS/ESD Symposium

### EOS/ESD Symposium
### September 7-12 at the Westin La Paloma in Tucson, AZ

For the first time, emerging technology seminars are offered in addition to the regular tutorials at the 2014 EOS/ESD Symposium. The emerging technology seminars are targeted to experienced ESD designers and technologists who would like to learn more about upcoming technologies to better assess the impact on ESD design and ESD protection concepts. They will provide a condensed and first hand overview of the technology with clear indications of ESD and reliability relevant aspects. This is a unique chance to get important information without needing to attend general semiconductor technology conferences. The two seminars below are being presented by leading experts in their field and will give the attendees an excellent insight into GaN and 3D IC technologies.

**NEW GaN-Based Devices: Technology, Physics and Reliability**
**1:00 p.m. - 2:30 p.m.**
*Matteo Meneghini, University of Padova*

GaN-based transistors have recently demonstrated to be excellent devices for application in the RF and power conversion fields. This short course will review the technology, physics and operating principles of GaN-HEMTs; moreover, we will describe the mechanisms that limit the dynamic performance, the lifetime and the ESD robustness of these devices. A critical review of the most recent studies on these topics will be also presented.

**NEW Emerging Technology Seminar 3D IC Stack Integration**
**3:00 p.m. - 4:30 p.m.**
*Bob Sankman, Intel*

3D stacking of silicon integrated circuits, using through silicon vias as the interconnect, has been an active topic in the research community for more than a decade. As appealing as the technology is, it has yet to have garnered wide acceptance in high volume products. A brief history of the 3D architecture, practical issues in design, fabrication and assembly of components will be discussed along with a perspective on what's to come in the future.

**2014 EOS/ESD Symposium Registration is Now Open!**

**www.esda.org/symposiaEOS-ESD.html**

## In this issue



Watch for the *Threshold* E-Newsletter by email!

## From the President

# *Change in the desert!*

ESD Association President;
Terry Welsher

The ESDA just completed another successful meeting series in Tucson, the site of this year's EOS/ESD Symposium, September 7-12, 2014. This will be the 4th time that the Symposium will be held at the Westin La Paloma. Many of us who have been there several times have commented to each other how much we enjoy this location. So while it is a familiar site, there was plenty of change apparent during this series. This was our first April meeting in Tucson. It turns out that it is surprisingly cool in southern Arizona in April and many of us found ourselves without sufficient sweaters and jackets on a few of the cooler, windier days. Even so the weather was great overall: crisp cool mornings and bright sunshine during the day. Another bonus was the blooming palo verde trees which put a different background and texture on our time there. Of course there were other changes. We were there in April after listening to members who needed ways to reduce travel costs. One April meeting has replaced the old February and June meetings. As a result we also learned, or had our expectations confirmed, that face-to-face meetings are in fact very important. There was a concerted effort by committee chairs and meeting participants to make the most of what is now reduced "face time". In that spirit, some meetings were set up in new arrangements intended to foster interaction and provide an open creative environment. Feedback on these new set-ups was very positive, but of course attendee feedback is very important so let us know if you have suggestions for further improvement.

Other change was in the air in the technical arena as well. A new crop of "buzz" words could be heard in the meetings and work rooms - 3D ICs, GaN, flat panel display, low voltage testing and requirements and many others – maybe you have heard of additional ones. The upcoming Symposium Technical Program and Tutorials will be delving into these topics and many others as well as introducing new ones. Hope to see you all there as change continues in the desert.

ESD Association

# 2015 Board of Directors Nominations

## ESD Association Members Can Cast Votes Before July 1, 2014

Nominations are placed and ESD Association members have been sent a link to this year's online voting system. Select up to four nominees to serve on the ESD Association Board of Directors for the three-year term beginning January 1, 2015. Members may cast "write-in" votes by typing the name(s) of a person(s) in the "write-in" box.

The following individuals are seeking a seat on the Board of Directors for the next term:

### Brett Carn

Brett Carn initially joined Intel Corporation in 1999 and is a Principal Engineer in the Corporate Quality Network. He has actively worked in the field of device level ESD at Intel. In that role, Brett chairs the Intel ESD Council overseeing component level ESD & Latchup testing across all Intel sites, defining internal test specifications, reviewing all Intel ESD design rules, overseeing the ESD target levels for all Intel products and leading post silicon ESD debug on a variety of products. Prior to joining Intel, he worked for Lattice Semiconductor for 13 years where he started working on ESD in the early 1990s. For Lattice, Brett set component ESD layout rules for the company as well as handling all ESD qualification testing and product debug. Since 2007, Brett has been a member of the Industry Council on ESD Target Levels and has helped author several whitepapers as well as been the lead editor on the last three whitepapers. Additionally, for the past year, Brett has been a member of the ESDA Education Council and is an active member of the joint ESDA/JEDEC CDM WG driving for a consolidated CDM ESD Specification. Brett received his B.S. in Electrical Engineering from Portland State University in 1986.

**Vision**

This is an interesting time in the ESD Industry. We have made great progress in getting alignment across the Industry on HBM and CDM target levels but there is still more work to do. We are just starting to recognize the importance of aligning the Industry on the importance of EOS and putting new focus on addressing the EOS side of the EOS/ESD Association. I am committed to ensuring these efforts continue and that we continue to look at new ways to increase awareness and define a joint direction between the system manufacturer and their suppliers regarding EOS. In addition, as a member of the Education Council I have seen the benefits the ESDA can offer in terms of training and I am committed to expanding our live/on demand course offerings, enabling the ESDA to reach a broader scope of engineers while improving Industry understanding regarding both ESD and EOS. We have made great strides over the past year in regards to merging the ESDA and JEDEC CDM specifications, but more than that, we need to look at opportunities to improve on our CDM testing methodology to eliminate the variability seen in a field-induced test setup. As an ESDA board member, I would like to keep focus on this as we move into advanced technologies, pushing IO performance, resulting in reduced ESD target levels where accuracy in the test method will become even more critical.

### Joshua (Yong Hoon) Yoo

Joshua (Yong Hoon) Yoo has worked in the static control industry since 1994, providing ionization systems and test equipment, technical support, and auditing services of manufacturing processes. He worked for MKS Korea as a senior applied technologist. In 2003, Joshua started his own company, Core Insight, Inc., for advanced static control products and services based in Korea. Joshua has been a member of the ESD Association since 2000 and is an active member of the SEMI ESD taskforce. He serves global electronic companies for static related yield impact improvements and quality and reliability issues. He has studied micro contamination and ESD control issues in the flat panel display (FPD) industry. He wrote and presented the paper "Comparing Room Ionization Technologies in FPD Manufacturing" at the 34th EOS/ESD Symposium in 2012 in Tucson, AZ. He invented alternative room ionization technology for the FPD industry for both contamination and ESD control. Joshua holds four patents for ionization technologies, and contamination control systems. He is a chair of ESDA's FPD working group and is currently gathering technical information for preparing a flat panel display stress testing standards within this group. He is also a member of the ionization working group. Joshua has been an instructor of the two-day seminar 'Essentials for ESD Programs' in Asia locations. He serves as an Asia publicity chair for the 2013 and 2014 International ESD Workshop. Joshua is an iNARTE certified ESD engineer and an ESD Association certified program manager. In 2011, he founded the Korea Local Chapter of the ESD Association and is currently president. With his effort, the Korea Local Chapter is one of the most active local chapters.

**Vision**

Joshua (Yong Hoon) Yoo has a vision for ESDA to be more globalized in activities and within the organization. He believes that ESDA needs to be leading the industry internationally and widely expand industry areas, such as flat panel display, optical device, LED, etc. Also, ESDA needs to be more global with localized activities in areas like China, India and many other Southeast Asian countries. ESDA has leadership to lead, educate, and publishing updated and new standards not only for these new industries but also geographical regions. These industries and countries are becoming more important manufacturing locations, as well as a growing consumer market. Joshua wants to serve ESD industry and work with ESDA to lead these industries and regions.

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## ESD Association

### 2015 Board of Directors Nominations continued

**Harald Gossner**

Harald Gossner, Senior Principal Engineer at Intel Mobile Communications, received his degree in physics (Dipl. Phys.) from the Ludwig-Maximilians-University, Munich in 1990 and his Ph. D. in electrical engineering from the Universität der Bundeswehr, Munich in 1995. For 15 years he has been working on the development of ESD protection concepts for bipolar, BiCMOS and CMOS technologies with Siemens and Infineon Technologies. In 2011 he joined Intel Mobile Communications overseeing the development of robust mobile systems. Harald Gossner has authored and coauthored more than 100 technical papers and one book in the field of ESD and device physics. He holds 50 patents on the same topics.

He has served in technical program committees of IEDM, EOS/ESD Symposium and International ESD Workshop. In 2010 he was responsible for the arrangements of IEW at Tutzing. He is General Chair of EOS/ESD 2014. He co-founded Industry Council on ESD Target Levels in 2006 and is co-chairing the council since then. He is involved in the further development of ESDA Advanced Topics business unit.

He was co-recipient of the best paper awards of EOS/ESD Symposium 2005 and 2012. His contributions to education were recognized by the Outstanding Contribution Award 2010 of ESDA Education Committee. He is member of the advanced topics and education committees responsible for the design tutorials. He is currently serving on the Board of Directors, elected in 2011.

**Vision**

After envisioning and driving an orientation towards new applications and system related aspects in my first term I now see the challenge to establish ESDA as the unique place for providing best ESD and EOS know-how to a large community of system and IC designers. As development activities have been shifted globally we also need to make sure that we address oversea locations with our education offer equally well. I will put my focus on both topics if I am reelected for a new term. The experience of co-chairing the international, cross-functional Industry Council and my multiple contacts to Asia and Europe will help me to work together with the ESDA board successfully on these targets.

**Michael G. Khazhinsky**

Michael G. Khazhinsky is currently a Senior ESD staff engineer/designer at Silicon Labs in Austin, Texas. Prior to joining Silicon Labs, he worked at Motorola and Freescale Semiconductors where he was in charge of the TCAD development and ESD/latchup protection solutions for emerging process technologies, with a focus on ESD-EDA. Michael has M.S.E.E. and M.S. Physics from the Moscow State Institute of Electronic Engineering, and Ph.D. in Physics from Western Michigan University. Michael served as a member of the IRPS, IPFA, IEW, and EOS/ESD Symposium Technical Program Committees, as well as a Workshop Chair, Technical Program Chair, Vice General Chair and General Chair of EOS/ESD Symposium. Michael co-authored over 30 external papers and gave a number of invited talks on ESD, EDA, process/device TCAD, and photonic crystals. He was a co-recipient of six EOS/ESD Symposium and SOI Symposium “Best Paper” and “Best Presentation” awards. Michael currently holds sixteen patents on ESD design, with additional patents pending. Michael is a Senior Member of IEEE.

**Vision**

I am asking for your support in reelecting me for the second term with the ESD Association Board of Directors. During my first term with the ESDA Board of Directors I led the optimization of the Symposium device/design tutorials and streamlined the review process. Team reviews were introduced that significantly improved the quality of offered tutorials and opened opportunity for the new tutorials such as System Level ESD design, RF ESD design, HV ESD design, Advanced Latch-up, TCAD, etc.

I am ready to take up new challenge and looking forward to expanding my responsibilities within the ESD Association. My vision is to broaden ESDA horizons. Recently I joined the Advanced Topics team. Its main goal is to help evolve ESDA into the areas where its participation is not prominent at the moment. We are currently working on such topics as Flat Panel Display, IP Design House Interface Requirements, EDA, Aerospace, 2.5D & 3D ICs, etc. With your help and feedback in identifying additional areas of opportunities for the ESDA we can make the work of the Advanced Topics team a success.

On my part I am ready for new challenges and opportunities that the Board of Directors position brings and I promise diligence, enthusiasm and energy to lead the Advanced Topics ESDA team and perform my other duties if reelected.

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ESD Association

## 2015 Board of Directors Nominations continued

**Charvaka Duvvury**

Charvaka Duvvury worked as a semiconductor technologist at Texas Instruments for more than 35 years. He is currently an independent consultant in ESD technology, resolving ESD reliability concerns and educating new generations of electronics engineers. He is also co-chair of the Industry Council on ESD, bringing the electronics industry together towards realistic goals on ESD. He received his PhD in Engineering Science and worked as Post-Doctorate Fellow in Physics before joining TI's Advanced CMOS Technology Group. While at TI he was also the Chair of the ESD Council for developing ESD technology. He was elected Senior Member (1990), Distinguished Member (1997) and TI Fellow (1997). He has significantly contributed to the industry by offering education in ESD for more than 25 years through tutorials at the ESDA, IEEE sponsored conferences, and the Berkeley Extension ESD Short Course program. He was elected as Board of Director for the ESDA during 1997 and has been serving as the Academic Outreach Chair promoting education and research about ESD in the universities. For these contributions he has been twice awarded the SRC's Outstanding Industry Liaison Award (1994 and 2012), IEEE Fellow (2008), and recently the IEEE Education Award from the Electron Devices Society (2013). He also received the Outstanding Contributions Award from the ESD Association (1990). Charvaka served on the TPC and twice as General Chair (1994 and 2005) of the ESD Symposium, and on other technical committees (IRPS and IEDM). He was editor of the TDMR for 10 years. While contributing to ESD he published over 150 papers and holds more than 70 patents.

**VISION**

A global focus on ESD education and providing opportunities for further research have become critical factors for support of the rapidly developing and broadly exploding electronic technologies industries. This is further substantiated by the ever increasing interest in ESD in emerging countries like China and India. As co-chair of the Industry Council for more than 7 years, while establishing the proper perspective on ESD requirements compatible with the advanced technologies, and as the original contributor to the ESDA's Technology Roadmap, I have the vision to promote this important objective on behalf of the ESDA. My years of experience as the Academic Education Liaison provides me the contacts and the leverage to make progress towards these goals. Also as co-founder of the ESD Research Council I can work with other Board members, the Advanced Topics Committee, and the technical colleagues at universities to improve the critical focus on ESD. In the same vein, with my experience of interactions with customers I can guide the education in ESD for benefit to the industry as a whole. The ESDA's motto has been to serve the industry and become globally known, and I intend to do my part in this endeavor if elected as Board member. Thank you.


# You are invited to join!

## Working Group 10.0 Handlers

The EOS/ESD Association, Inc (ESDA) Working Group 10.0 – Handlers is responsible for writing standards regarding ESD mitigation for various types of manual and automated assembly equipment.

Current standards include:

- ANSI/ESD SP10.1-2007 Automated Handling Equipment (AHE)
- ESD TR10.0-01-02 Measurement and ESD Control Issues for Automated Equipment Handling of ESD Sensitive Devices Below 100 Volts

Documents developed by the group will provide guidance to the industry on how to qualify equipment assembling electronic devices and PC boards. The standards will provide a methodology to test and measure generation of electrostatic charge as the devices are processed through the equipment. This information will be used to qualify and accept new handlers. Handler manufacturers are already asking if their equipment can safely process the newer device technologies and these standards will provide a means to verify that.

**For information about joining ESDA working groups please contact info@esda.org**

## Local Chapters

# "Local Sparks"

***The Local Chapter Connection***

### ASEMEP ESD Council
Makati City, Philippines
Contact: Celon Cada (Chairman)
E-mail: Celon.Cada@onsemi.com
no website available

Congratulations to our New Student Chapter! Look for photos and the official announcement in a future Local Sparks column.

### Chengdu Student Chapter ESD Association
Chengdu, China
Contact: Aihua Dong (President)
E-mail: aihua.dong@foxmail.com
no website available

### Indian ESD Association
Jayanagar, Bangalore, India
Contact: Akshinthala Vijayendra
Phone: +91(0)9845030634
Fax: 91-80-255-34213
E-mail: 2nteknics@gmail.com
no website available

### Korea ESD Association
Contact: Joshua Yoo, President
Elly Koo, Liason
Phone: 82-31-750-9207
E-mail: info@esd.or.kr
www.esd.or.kr
The Chapter will also be hosting an ESD workshop on June 26-27 with various subjects including; device design, TLP testing, automotives, and factory control issues.

### North Central ESD Association
Bloomington, Minnesota
Contact: Dale Parkin
E-Mail: dale.parkin@seagate.com
www.esdnorthcentral.org

### Silicon Valley EOS/ESD Society
San Jose, CA
Contact: Wayne Tan, President
Phone: 408-660-8609
E-mail: SiVaReply2010@gmail.com
www.esdiscovery.org

### Texas ESD Association
Contact: Dave Swenson, Liaison
Ph: 512-244-7514
E-mail: static2@swbell.net
www.Centxesdassoc.homestead.com

### Northeast ESD Association
Contact: Ted Dangelmayer
Phone: 978-282-8888
E-mail: ted@dangelmayer.com
www.nechapter-esda.org

The Chapter will also be hosting its spring regional tutorials on May 5-7, 2014 at the Teradyne Conference Center 600 Riverpark Drive North Reading, MA. Courses include:

- Class 0 Devices & Boards - ESD Controls and Auditing Measurements
- ESD Standards Overview for the Program Manager
- Packaging Principles for the PrM
- Ionization Issues and Answers for the PrM
- Flooring Selection: Uncovering Maintenance, Ownership and Performance Pitfalls

Registration information is available on the ESDA website at:
www.esda.org/calendar

## Q&A

**Q.** I work for a company that provides soldering robots. A customer has asked us to provide a certificate proving that the machine is ESD certified. I'm not even sure where to begin.

**A.** This is not a common question but we expect it will be one asked more often from now on. We imagine that the customer is interested in knowing how safe the soldering robot is, as it relates to charging or discharging to their products, during manufacture. The ESDA has a soldering iron test procedure that is used to evaluate normal (hand-held) soldering and de-soldering equipment that could certainly be used to evaluate the soldering robot. Basically, you would measure the voltage present on the actual part of the robot that would touch the product being manufactured. You might want to obtain a copy of the test method and study it to determine if you can make it work for your equipment.

**ESD STM13.1-2000 Electrical Soldering/Desoldering Hand Tools**

This standard test method provides electric soldering/desoldering hand tool test methods for measuring the electrical leakage and tip to ground reference point resistance, and provides parameters for EOS safe soldering operation.

There are also test procedures established for CE marking that would evaluate the equipment in terms of ESD susceptibility and radiated emissions within the IEC61000 series of standards. There may be something in those documents that may be useful as well.

*The response given is a service to industry; the ESDA is not responsible for content. The users of this information need to determine the suitability of the response.*

Certification

# ESDA Certification - Making a Strong Statement!

The principle goal behind the ESD Association's Professional Certification programs is to ensure the understanding of the standard practices, test methods, and problem solving techniques used to control ESD. Many certified professionals view certification as a feather in their cap that entitles them to bragging rights; however, this is by no means the main reason for individuals to pursue certification. The primary reasons include increased employability, greater growth potential, and networking opportunities. Individuals who increase their effectiveness and knowledge with certification not only improve their performance on the job, but can command greater compensation and enjoy greater job security. Networking gained through certification training is essential to career development, and the ability to connect with ESDA professionals can be a huge benefit to those just entering the ESD arena as well as more established professionals.

**Certified Professional-Program Manager**

The ESDA has made it easier for individuals who are interested in obtaining program manager certification by now offering many of the classes online. Courses that are offered online include:

- Cleanroom Considerations for the Program Manager
- Ionization Issues and Answers for the Program Manager
- System Level ESD/EMI: Testing to IEC and Other Standards
- Packaging Principles for the Program Manager
- ESD Association Standards Overview
- Device Technology and FA Overview
- Electrostatic Calculations for the Program Manager and the ESD Engineer

The ESD Association now recognizes 59 Certified Professional-Program Managers

- Ronald J. Gibson
- John T. Kinnear Jr.
- Stephen A. Halperin
- David E. Swenson
- Leo G. Henry
- Arnie Steinman
- Christopher W. Long
- Michael Hopkins
- Kevin Duncan
- Carl Newberg
- Douglas Miller
- Timothy A. Prass
- Dale Fuller
- Brad Klepsa
- Marcus Koh
- Jim Krzmarzick
- Jeff Salisbury
- Luis Velazquez
- John Clack
- Timothy T. Fox
- Christopher Lemke
- Daniel Mitchell
- Patsawat Tachamaneekorn
- Kep Pen Yan
- Matt Banning
- Minh Do
- William Foster
- David N. Girard
- David Hattz
- Michelle Lam
- Roger Peirce
- Michael Scott
- Michael Vickers
- Christopher Almeras
- James Cramb
- Timothy Jeffries
- Paul Keep
- Andrew Kopanski
- Canon Laverty
- Ronnie Millsaps
- Tim Peterson
- Douglas Rogers
- Eric Williams
- Rich West
- Humberto Hernandez
- Jad Allam
- Shane Heinle
- Michael Lauritzen
- Stephen Martin
- Younchul Oh
- Becky Amundsen
- Joshua Yoo
- Jearell Kelley
- Jay Skolnik
- Julian Tyler
- Sunisa Chobsri
- Chin Siang Tay
- Arnel Jalbuena
- Jim Evevsky

**Certified Professional-Device Design**

Created for device design engineers the ESDA is now developing device design certification courses for online delivery.

The ESD Association recognizes 10 Certified Professional-Device Designers

- Leo G. Henry
- Charvaka Duvvury
- Mike Hopkins
- Steven H. Voldman
- Robert A. Ashton
- Warren R. Anderson
- Mike Chaine
- Gianluca Boselli
- Rosario Consiglio
- Charles Meyerson

The ESD Associations Newest certification program is coming up on its first year anniversary. Many of those certified are looking to fulfill their annuall recertification requirements.

First year requirements are to complete one continuing education course of their choice. The second years requirement is to attend the ESD Stress Testing Standard Updates course. In preparation for those who are in the process of first year recertification, we will offer one new elective "ESD Test Simplification with Approved Sampling Methods in HBM" This class will focus on the new HBM document about to be released. Additionally the the Standards Update class is being developed and will launch online later this year.

The ESD Association now recognizes 25 Device Stress Testing Certifications

- Kenneth Brooks
- Ephrem Gebreslasie
- James Goussy
- Pradeep Sharma
- Thomas Chang
- Yan Gao
- You Li
- Bill Reynolds
- Lin Lin
- Chris Seguin
- Bill Russell
- Rahul Mishra
- Richard Poro
- Moon Lee
- Mark Sharp Jr.
- Fan Zhou
- Richard Desautels
- Zhen Li
- William Young
- Thoma Luzi
- Sasa Vidic
- Chris Langone
- Dave Drew
- Chi Tai Hong
- David Rose

## Standards

Standards Working Group Summary
April 2014 Meeting Series
Westin La Paloma, Tucson, AZ

**WG2.0 – Garments**

The committee discussed the exploration of a test method for garments made with buried conductor fiber which does not result in either a conductive or static dissipative resistance with ANSI/ESD STM2.1-2013. The WG will proceed with contacting garment manufacturers of buried conductor fabrics to obtain six sets of the same garment for testing, determine an inductance measurement on circulated samples, and ask garment manufacturers of buried conductor fabric to participate in the evaluation of a test method for buried conductor garments.

**WG3.0 – Ionization**

The committee reviewed and adjudicated comments on the five-year review of ANSI/ESD STM3.1 that were submitted by members of the Technical and Advisory Support (TAS) committee. The document will be circulated for STDCOM vote-by-mail before the September meeting series.

The committee also reviewed a new technical report - Test Methods for Air Assist Bar Ionizer, Soft X-ray (Photon) Ionizers, and Alternative Room Ionization. The document will be submitted for TAS review before the September meeting series.

**WG4.0 – Worksurfaces**

The committee continued working on the five-year review updates to ANSI/ESD STM4.1. Test procedures and drawings were discussed for the new sections on carts and shelving. There will also be an additional annex describing the testing of conveyors when used as a work surface.

**Adhoc–Electrical Overstress (EOS) Best Practices Task Group**

The committee reviewed the proposed document scope and relationship of the committee's work to other EOS efforts in the industry (Industry Council, ESDA EOS TR, and SEMI EMC). The committee will interact and harmonize where possible with the Industry Council work on EOS. The on-going literature review was discussed. Although there have been many studies, documents, and practices identified, some gaps remain. The committee discussed the EOS fishbone diagram which has been used in several other documents and a decision was made to modify the diagram to reflect the manufacturing focus of the document.

**WG5.0 – General Device Testing**

The committee updated the ESD handling boilerplate as follows:

"ESD damage prevention procedures shall be used before, during, and after CDM and post parametric testing.

NOTE: See the latest revision of ANSI/ESD S20.20, JESD625, or IEC61340-5-1 for guidance."

A proposal to produce a technical report on ESD thresholds and data sheets was presented. The purpose of this TR is to provide guidance on how to interpret ESD HBM and CDM withstand thresholds and to provide recommended data sheet formats for reporting the information. Provision of supplemental information that gives a better representation of relative risk will be included. The formats will also address confusion between device level HBM data and IEC test results.

**JWG – (HBM) Device Testing**

The status of JS-001-2014 was reviewed and a process for collecting all soft copies of figures and charts was initiated. A subcommittee will begin revising the technical report user guide to align with JS-001-2014. An update was given about the "Advanced Statistical Sampling" project. Though some questions remain, the results show that the method is viable and produces expected results in reduced test time and more realistic threshold results. A draft document will be circulated to the JWG for comment between meeting series. A presentation was given to review of the work of the Next Generation ESD Team. The work on software for data entry for HBM was discussed and the committee was re-constituted. The last hour was spent brainstorming items for future work. Among the items discussed were changes in the ESD threshold definition, testing no-connects, and testing at low voltage (i.e., 50 volts).

**JWG – (CDM) Device Testing**

After a brief review of activity since the September face-to-face meeting (including the 12-tester FFPA Ipeak centering experiment comparing to JEDEC), the JWG reviewed the TAS comments from a second review of the joint document draft. Minor editorial changes were made to the document that will be circulated for STDCOM VBM by mid-April. There may be additional investigation comparing waveforms from ferrite-free JEDEC probe assemblies with those from ferrite-free ESDA assemblies.

A presentation on "Improving CDM Current Measurements" focusing on the probe assembly effect on the CDM waveform was given.

The contact CDM technical report draft status was discussed and a draft will be sent to JWG for review.

A representative from the JEITA (Japan) reliability standards group has inquired about possibly harmonizing their CDM waveform data and their document with the JWG document. The JWG will request more information for comparison.

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## Standards

**WG5.4 – (TLU) Device Testing**

First, the Transient Latch-up workshop at the EOS/ESD Symposium 2013 was summarized. Several attendees face Transient Latch-up problems in different applications and have their own Transient Latch-up characterization methodology. There was consensus among the attendees of the workshop to ask the ESD Association to develop a Transient Latch-up characterization methodology. According to the attendees, the characterization method should include at least two trigger pulses with different pulse parameters.

The status of the new Transient Latch-up standard practice was reviewed. A first draft was already reviewed by the members of the SP Writing Team; however, the first draft of the document was significantly extended and changed based on the inputs of the Transient Latch-up workshop and further technical input from members of the working group.

After intense technical discussions, the working group decided on the latch-up trigger pulse parameters, the different test modes, power supply response verification, and compliance and de-coupling of the power supplies. An updated version of the second draft will be distributed to the working group in May. Based on the current document, key experiments will be carried out by members of the working group to prove the feasibility of the methodology. In the next face-to-face meeting in September 2014, the remaining technical issues should be solved based on the results of these experiments. The standard practice should be ready for submission to TAS at the end of 2014 or the beginning of 2015.

**WG5.5 – (TLP) Device Testing**

The committee adjudicated industry review comments on ESD DSTM5.5.1-2014. The document will be submitted to HQ between meeting series. In addition, the committee reviewed the precision analysis of the round robin data for vf-TLP, which was approved by TAS. A TR will be drafted to summarize the data, the precision analysis, and the conclusion. It will address the issue of the noisy data. Revisions will also be made to ANSI/ESD STM5.5.2 to re-designate the document as an STM and then it along with the TR will be submitted to TAS before September. The WG will begin combining STM5.5.1 and STM5.5.2 once both of the current documents are published. The following three presentations were given:

1) Transient analysis - the WG concluded that this was a relevant topic and should be addressed. The goal is to start with experiments to see what different methods/tools give and write a report on the results. The goal is to start experiments after the September meeting.

2) Calibration for different pulse widths - The WG agrees that this is something to be addressed in the merged document. It will not affect the current plan.

3) Effect of reverse reflections – the WG concludes that this is something to be considered for the merged document or in a separate set of application notes/TR.

**WG5.6 – (HMM) Device Testing**

A presentation that reviewed some HMM pulse sources was provided. Each complies with the waveform requirements of the ANSI/ESD SP5.6 requirements as well as the IEC 61000-4-2. The rather loose specifications for the waveform gives a large latitude in meeting these requirements and the presenter was looking for guidance on what the waveform should look like between the currents defined at the specified times. It was pointed out that there is an equation in the IEC 61000-4-2 standard which describes the waveform. This could be used as a template for building a pulse source.

A series of single laboratory measurements were made as preliminary measurements to help define the cause of the wide variations in the failure levels during the round robin. The measurements showed voltage and current capture from three ESD guns and a TLP base pulse source along with the failure levels which resulted. The measurements showed better repeatability than some of the round robin results. The measurements also pointed out the need to adjust for the 50-ohm impedance of the voltage measurement equipment, or to adjust the measurement setup to eliminate this need for the correction.

The remainder of the meeting was spent discussing the wisdom of continuing working group efforts with regard to the use of ESD guns, rather than simply describing a pulse source which would have a pulse shape compliant with the ANSI/ESD SP5.6 or IEC 61000-4-2 waveform but not having the wide tolerance of the IEC waveform. In the end it was accepted that the industry wants to have a method using the ESD gun and we need to better understand why the round robin results are not as good as they should be.

**WG9.0 – Footwear**

The WG adjudicated industry review comments and the document will be submitted to HQ for publication prior to the September meeting series.

**WG10.0 – Handlers**

The WG completed the adjudication of VBM comments on five-year revisions to ANSI/ESD SP10.1. Technical changes were made so the document will be circulated for a STDCOM recirculation vote between meeting series. The WG also discussed a new TR on conductive nozzles and grippers, which members will review a draft between meeting series. The WG will be completing further testing related to discharge currents to targets for the new document on testing done in handlers. The committee is also looking for new members and participation, as well as, the use of handling equipment for testing.

*Continued on page 10*

## Standards

**WG11.0 – Packaging**

The committee finished adjudicating industry review comments for ESD DSTM11.13 and the document will be submitted to HQ for publication. The WG completed adjudicating STDCOM VBM comments for STM11.11 and STM11.12 and the documents will be submitted to HQ for industry review distribution. The committee will be undertaking round-robin testing that will include both the surface and volume resistance test methods. The committee reviewed ANSI/ESD S541 for five-year review revisions and will circulate the document between meetings. The committee identified a need to explore expanding the shielding test method in ANSI/ESD STM11.31 to allow evaluation of boxes and other packaging forms. This area will be discussed further at future meetings.

**WG13.0 – Handtools**

The committee completed the adjudication of STDCOM VBM comments on ESD WIP13.1-2013 and the document will be forwarded to headquarters for a recirculation vote. The committee also reviewed the status of ESD WIP13.2 and will begin working on the document at the next meeting series.

**WG14.0 – System Level ESD**

The committee discussed the recent major revisions to ESD WIP14.5 - EMC Scanning based on STDCOM VBM and TAS comments. The document will be submitted to HQ for a second STDCOM VBM based on the number of changes. The committee also discussed the creation of the CDE test method and the current status of ESD WIP14.3 and ESD WIP14.4. A draft document will be circulated prior to the September meeting series for discussion. A presentation was given on System Level ESD Modeling. The committee ended the meeting with a discussion about possible new work including correlation testing in EMC scanning and the CDE test method.

**WG15.0 – Gloves**

The committee reviewed the status of ESD WIP15.2 and discussed a suggestion to include the use of a contact electrostatic voltmeter (ESVM) instead of, or in addition to, the current Faraday Cup measurement. The committee will complete single laboratory evaluations using the both contact and non-contact ESVM's and Faraday Cup measurements before the September meeting series.

**WG17.0 – Process Assessment**

The committee reviewed TAS comments on TR17-01-14 "ESD Process Assessment Methodologies in Electronic Production Lines – Best Practices Used in Industry" with a summary of papers published at the Symposium. The document will be submitted to HQ for publication between meeting series. A presentation was given on experiments performed at Infineon and Intel on discharges of charged devices and boards under typical process conditions. The methodology and the results of the work will be used in the new document on process assessment.

IEC TC 101 and the German ESD Forum agreed to cooperate with the ESDA on a document on process assessment. The purpose of the document is to help the industry in assessing ESD risks in production by process evaluation. A draft document is expected by June.

**WG19 – Aerospace**

The committee meeting consisted of a series of presentations to validate the connection between ESD Control Programs as one component of a quality system. Further discussions are taking place to determine the correct direction for a quality control type-document. The quality control document addressing the request from WG19 will be published as a TR.

**WG20.20 – ESD Control Program**

The committee reviewed TAS comments on revisions to ANSI/ESD S20.20 following committee conference calls between meetings. The document will be distributed for a recirculation vote by May 1.

**WG53 – Compliance Verification**

The committee reviewed changes based on comments from the STDCOM courtesy review. The document will be submitted to HQ for publication before the September meeting series.

**WG 97.0 – Footwear Systems**

The committee adjudicated industry comments on ESD DSTM97.1 and the document will be submitted to HQ for publication. The WG began adjudicating STDCOM VBM comments on ESD WIP97.2 and will finish between meeting series.

**Flat Panel Display (FPD)**

The committee reviewed the scope of the committee and added the handling of ESD issues in FPD during fabrication, module assembly, but not completed product or display device. Investigation includes ESD damages on TFT LCD device, Damage Mechanism, Propose Possible Stress Testing Method and Factory Control Guideline. A technical report is being drafted and will be distributed to the WG for discussion in September.

## ESDA Spotlight

### The spotlight is on volunteer Bart Keppens

Volunteering to help at ESDA events has been rewarding: you get to work together across company boundaries to a shared goal, meeting new people, learning from each other, seeing different opinions on many topics.

Bart Keppens received a master degree in Electronics Engineering from Groep T, Leuven in 1996. His master thesis, together with his colleague Steven Servaes, titled 'Transmission Line Pulsing (TLP) technique for analyzing ESD reliability', performed at IMEC (under supervision of Koen Verhaege and Christian Russ), received the BARCO-award for best Industrial Engineer thesis in 1996. The outcome was a 500 Ohm, 100ns TLP system to analyze packaged samples. Thanks to Steven's custom relay-in-a-coax design, it had a sub 1ns rise time.

In August 1996 Bart joined IMEC's reliability group, led by Guido Groeseneken, where he supported the 'ESD' and 'Non Volatile Memory' groups in various ways: Creating test chip layout (0.7um BCD, 0.5um, 0.25um, 180nm CMOS), performing electrical characterization and programming control software for the lab equipment. The first TLP system from the 1996 master thesis was continuously improved with new control software, a measurement database and on-wafer analysis possibilities. A second TLP was created in 2000, based on a solid-state pulse generator. Together with ESD experts like Guido, Christian Russ, Karlheinz Bock, Vesselin Vassilev, Vincent De Heyn, and Natarajan Mahadeva Iyer the know-how on TLP construction, usage, and control software led to Bart's first publication at the EOS/ESD Symposium in 2001 in Portland and a panel member job.

In May 2002 Bart joined Sarnoff Europe, Belgium, solving ESD related problems for customers worldwide, first as an ESD engineer, then later as technical leader, ESD design specialist. Since 2006, Bart supports the Business Development initiatives as Technical Director for ESD. In June 2009, Sarnoff Europe became 'SOFICS - Solutions for ICs' where Bart now is Director Technical Marketing.

In total, Bart (co-) authored about 40 peer-reviewed published articles in the field of 'on-chip ESD protection' and 'ESD analysis'. Invited papers on ESD solutions and TLP analysis techniques have been delivered at the RCJ ESD symposium in Japan almost every year since 2006 and on Taiwan ESD's conference since 2009. Bart has been a member of the Technical Program Committee ('TPC') of the EOS/ESD symposium since 2003, and a member of the ESREF TPC in 2003, 2005, 2007, 2009, and 2010. A member of the Taiwan ESD and Reliability conference TPC since 2010. Bart acted as a Workshop Panel member on ESD topics during various conferences (EOS/ESD Symposium and RCJ) and presented invited tutorials at Taiwan ESD and

*Continued on page 12*

## ESD Association

Reliability conference in 2008, 2010, and 2012. Bart holds several on-chip ESD protection design patents.

Bart is married to Saskia and they have two daughters, Hanne (15) and Nienke (13). In his free time, Bart enjoys solving (binary) Sudokus, walking the dog, biking, and more recently running. Building up from no physical fitness and 20kg overweight to a full marathon within one year helped to realize that with dedication, perseverance, and support from family, friends, and colleagues once believed unreachable goals can be met. Thanks to frequent work related travel, Bart can now run at great locations around the world: Across Golden Gate bridge, around Tokyo's imperial palace, below Taiwan's tallest (Taipei 101) building…

Attending EOS/ESD conferences or IEW workshops is always a great experience. The conference is a good opportunity to meet with ESD colleagues from other companies and talk to friends that moved abroad. Many of the tutorials are useful for new hires as well as refresh insights for others. Moreover, for an IP company like Sofics it is extremely important to understand the upcoming problems, new test approaches. Attending the ESDA conferences and workshops is an efficient way to gather that new info. Because the conference is smaller than the giant conferences like IEDM, DAC, IRPS, attendees at EOS/ESD or IEW get to know each other better and get an opportunity to talk to and learn from the experts. Volunteering to help at ESDA events has been rewarding: you get to work together across company boundaries to a shared goal, meeting new people, learning from each other, seeing different opinions on many topics.

## Did you Know?

The ESD Association is successful because of its network of members who volunteer to carry out its mission and activities. Without volunteers, the ESD Association could accomplish very little. Volunteers have been very busy this year helping to organize ESDA events and activities. There are also volunteers who contribute their time on projects that are just as important to the ESD Association.

Liza Ariffin from Evans Analytical Group helped us with just such a project. After input from exhibitors at the 2013 Symposium the ESDA decided to change the lead retrieval process (means for capturing sales leads generated at the Symposium) for the coming year. Liza volunteered to create a new lead retrieval form that will be used by this year's exhibitors at the symposium. Great job, Liza! Thank you for your help.

The Association would also like to recognize another group of volunteers who were instrumental in translating and producing both a Thai and Korean version of the "Highlights and key concepts of Footwear/Flooring standards" online webinar. Joshua Yoo, of Core Insight, assisted in translating the webinar into Korean. Dutharuthai Na Pombejara (Nuss) of Seagate, created the Thai version. August Tazzoli of Maxim Integrated provided technical assistance in linking and editing files for the final MP3 presentations. The translated webinars are now available through our library of On-Demand webinars. To register please visit www.esda.org/onlinecourses.html.

For more information on volunteer opportunities with the ESD Association visit www.esda.org/CSP.html.

ESDA Academia

# ESD and EMC Activities at LAAS-CNRS

by Marise Bafleur,
ESDA Academia Chair

Scientific campus of the University of Toulouse where LAAS-CNRS is located.

The Laboratory of Analysis and Architecture of Systems (LAAS) is a CNRS (National Scientific Research Center) research unit associated with the University of Toulouse. LAAS-CNRS is also part of the 34 "Carnot Institutes" network (http://www.instituts-carnot.eu) that is committed to develop research for companies' innovation. The surrounding economical ecosystem is very rich since Toulouse is the town where AIRBUS aircrafts are assembled and several space industries (CNES, ThalèsAleniaSpace, Astrium, Intespace) are located as well as automotive equipment suppliers (Continental) and semiconductor companies (Freescale Semiconductor and ON Semiconductor).

Aerial view of LAAS-CNRS

LAAS-CNRS (http://www.laas.fr) carries out research activities on different types of systems: micro and nano systems, embedded systems, integrated systems, large scale systems, biological systems, mobile systems, autonomous systems and critical information systems, with application domains such as: aeronautics, space, transportation, energy, services, health, telecommunications, environment, production and defense. LAAS is organized in 8 research areas: Critical Information Processing, Networks and Communications, Robotics, Decision and Optimization, Micro Nanosystems RF and Optical, Nano-Engineering and Integration, Energy Management, MicroNanoBio Technologies.

Since 2012, Marise Bafleur is heading the "Energy Management" area whose research activities focus on three main topics:

- Integration of active and passive power devices
- Power conversion and energy management
- Robustness and reliability: ESD/EMI, radiation hardening, electrothermal modeling

For the latter one, the motto is to master the energetic environment of embedded systems, and in particular ESD and EMC related disturbances. ESD research activities started at LAAS-CNRS in 1996 with a PhD thesis [DEL99] in cooperation with Motorola Semiconductor under the supervision of Nicolas Nolhier. The motivation was to take advantage of the strong expertise of our research team in the field of power devices to apply them in this new field. EMC research activities are more recent (2009) and correspond to the reinforcement of the research team with two renowned experts in electromagnetic compatibility. There is now a strong convergence between ESD and EMC, in particular regarding modeling approaches at system level.

Today, six permanent researchers (Marise Bafleur, Sonia Ben Dhia, Alexandre Boyer, Fabrice Caignet, Nicolas Nolhier and David Trémouilles), two engineers (Nicolas Mauran and Manuel Cavarroc), five PhD and one postdoctoral students are currently involved in the ESD/EMC research activities. To support them, we have developed and set up two characterization platforms: one for ESD and the other for EMC including both commercial and original in-house test benches. Among the original test benches, we can cite: a near-field scan table allowing both EMC and ESD studies, TLP/VF-TLP test benches coupled to a photoemission camera, double-pulse TLP test bench for system level ESD characterization, wafer-level HBM, a 60ps-resolution transient TLP measurement method for the characterization of overshoots.

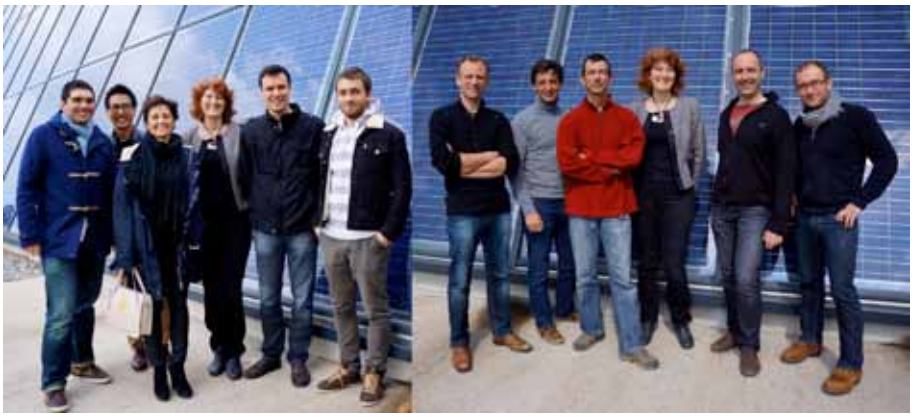
Firstly, LAAS-CNRS focused its ESD activities on the design of high-robustness ESD protections in cooperation with silicon foundries: Freescale Semiconductor,

*Continued on page 14*

## ESDA Academia

ESD and EMC Activities at LAAS-CNRS continued

ON Semiconductor, STMicroelectronics. Concurrently, we developed simulation and characterization methodologies to get a deep understanding of the involved physical mechanisms. It has to be noted that LAAS-CNRS was among the first laboratories investigating the ESD reliability of MEMS (within the framework of AMICOM European Network of Excellence). The studied device was a 40GHz MEMS RF capacitive switch. Two major results have been highlighted. Firstly, the MEMS ESD robustness is extremely low (under 100V) and some external protections are needed. Secondly, an innovative method of accelerated test for capacitive MEMS was proposed.



Left photograph: EMC team (V. Tomasevic, H. Huang, S. Ben Dhia, M. Bafleur, A. Boyer, M. Cavarroc). Right photograph: ESD team (F. Caignet, N. Mauran, N. Nolhier, M. Bafleur, D. Trémouilles, B. Courivaud).

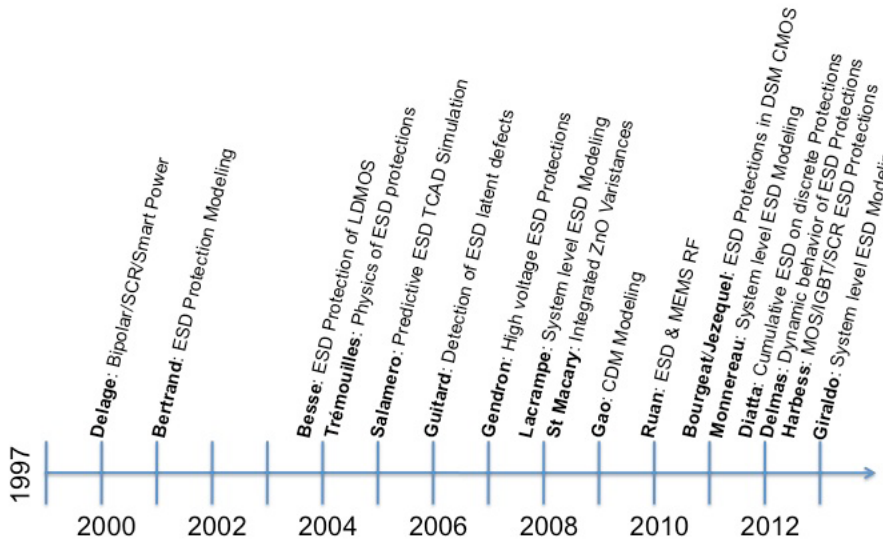
In 2006, LAAS-CNRS pioneered new studies on system level ESD by proposing behavioral modeling approaches and characterization methodologies. As of today, 18 PhD theses were defended in cooperation with industrial companies and academic laboratories resulting in 30 publications in international journals, 70 conferences and 4 patents. It has to be noticed that all these PhD students easily found employment right after their defense in France, Europe and United States and for most of them in the field of ESD.

Current ESD research activities are mostly focused on system level ESD and on studying the reliability and robustness of emerging power technologies.

Regarding system level ESD, two PhD theses are currently going on: one under the supervision of Nicolas Nolhier related to the design and optimization of transient voltage suppressors (TVS) and the other under the supervision of Fabrice Caignet and Marise Bafleur on system level ESD behavioral modeling and related characterization methodologies.

Innovative TVS structures based on 3D technologies issued from integrated passive devices are studied in cooperation with IPDIA company [COU13]. They provide a very good trade-off between ESD robustness efficiency (up to 33kV) and silicon area consumption. Given their compatibility with the technology of passive devices, they could also be co-designed and integrated with EMC filters.

Up to now, the impact on ICs of ESD stress at system level is still not well characterized. In particular, transient induced IC failure becomes an important concern. Transient electrical phenomena are powerful sources of interferences that can cause fatal (hard) failures but also functional (soft) ones such as electronic systems reset, data loss, or electronic systems reliability reduction. Nowadays, there are no robust methodologies, models and tools allowing the design of products that would result in hardening a




ESD PhD theses defended at LAAS-CNRS

*Continued on page 15*

## ESDA Academia

ESD and EMC activities at LAAS-CNRS continued

system for a certain requirement, whereas managing at the same time the safety margin. This work, in cooperation with Freescale Semiconductor, aims at developing a behavioral modeling approach based on experimental characterization of the IC for destructive failures in a first step and for functional robustness in a second one [BEG14].

Concerning emerging power technologies, namely wide band gap semiconductor to build power switches, David Trémouilles has initiated a research program to gain early assessment on reliability aspects, including ESD. SiC, GaN, diamond based devices are currently more or less mature and will sooner or later require thorough investigations on their reliability. SiC MESFET and GaN HEMT and diamond diodes are currently under investigation within the framework of one PhD thesis and one postdoctoral study in cooperation with CEA. This work benefits from a strong know-how on ESD testing and measurement acquired within the team along the years. High bandwidth and accuracy, large current and voltage measurement techniques are useful not only to characterize and study device behavior during an ESD stress but also to gain knowledge on the fast switching/transient operation made possible using wide band gap devices. In addition, to provide technologies with new overvoltage protection capabilities, a more fundamental research based on zinc-oxide nanoparticles is carried out to integrate varistor devices. Overall, the outcome of these studies would allow proposing simple solution to improve ESD robustness of future and emerging power electronic technologies.

With the increasing integration of various electronic functions within a same miniature system, the concerns about electromagnetic compatibility (EMC) issues are growing. In a context of severe requirements in term of EMC certification, especially for safety critical applications (e.g., aeronautics, space, automotive, health), EMC is an important source of redesign and extra-cost for manufacturers which do not integrate this constraint early in their own design and validation flow. Our research objectives are twofold:

- Developing measurement methods to improve the understanding of EMC related problems and their location within small integrated electronic systems.
- Proposing modeling and simulation methods to predict electromagnetic emission (EME) and susceptibility (EMS), and evaluating the risks of non-compliance of an electronic systems in a given environment (e.g., the influence of harsh environment).

In this context, Sonia Ben Dhia pioneered an original work on the impact of aging of ICs on the long-term EMC. It was shown through several experimental and modeling studies that the IC aging (accelerated in nanoscale technologies and in harsh environment) can induce non-negligible drifts of EME and/or EMS levels and then non-compliance risks. This work [BOY13] obtained the best paper award at EMC COMPO 2013 conference in Nara (Japan). This work was sponsored by the French space agency (CNES) and the ANR (The French National Research Agency).

Another original breakthrough is the design of on-chip sensors to characterize electrical signals induced in an IC during conducted susceptibility tests, with a good time resolution (10 ps). Such sensors are also used to characterize transient events in the substrate of an IC (AUTOMICS European project) or the propagation of an ESD stress within an IC and for modeling validation.

EMC methodologies can also be useful to cryptography. Indeed, Alexandre Boyer is leading E-Mata-Hari project (funded by The French National Research Agency) whose objective is to evaluate and quantify the threat of electromagnetic attacks on secured ICs based on near-field injection. Our main task consists in developing miniature injection near-field probes to simulate cryptographic attacks and using on-chip sensors to characterize and model the interaction between the probe and the IC.

As mentioned earlier, there is a strong convergence between ESD and EMC approaches and having ESD and EMC experts in the same team is very valuable. We are then sharing and co-developing characterization methods to analyze EMC issues in ICs or miniature electronic systems, and ESD problems in larger system (typically an electronic board). We are concurrently working on two complementary approaches with reduced intrusiveness, good resolution and large frequency range:

ESD characterization platform

*Continued on page 16*

## ESDA Academia

ESD and EMC Activities at LAAS-CNRS continued

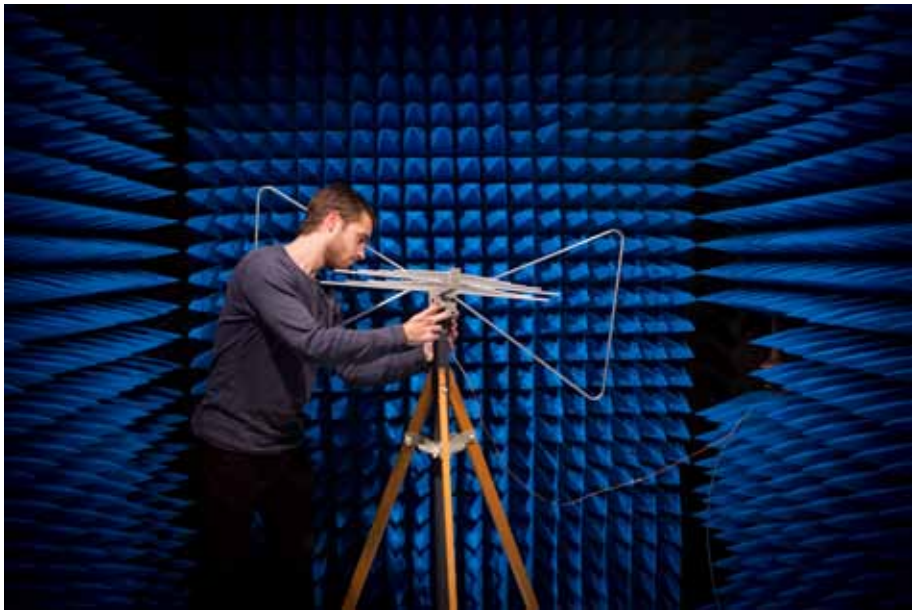
• On-chip sensors

• Near-field scan and miniaturized probes

The same synergy applies in the field of system level modeling: we use IBIS models initially developed by the EMC community and we enrich them with ESD models.

An important role of academic laboratories is dissemination of knowledge. To this purpose, since 2010, Fabrice Caignet is leading a discussion group at the ESDA standard committee to write a technical report on parameters extraction for system level ESD modeling. The ESDA Academia committee, funded in 2012 and chaired by Marise Bafleur, has the ambition to increase the synergies between universities and industry in the field of ESD. It has also setup a series of complimentary ESD web seminars, the first one was held on April 23, 2014 and a second one on August 7, 2014.

Since the involvement of LAAS-CNRS in the ESD field, research topics broadened from component to system and fruitful synergies have been created with the EMC community. In addition, some major breakthroughs either in characterization or protection design found applications in other domains such as radiation hardening of power devices [ARB13]. In Toulouse, EMC/ESD robustness is one of the hot research topics of Saint Exupéry IRT (Institute for Technological Research, http://www.irt-saintexupery.com) dedicated to aerospace and embedded systems and LAAS-CNRS is one of the key involved academic labs. One challenge within this starting program is the study of the impact of combined stresses (temperature, ESD, EMC, radiations…).



EMC characterization platform – Courtesy INSA - Baptiste Hamousin

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Marise BAFLEUR received her Ph.D. degree in 1982 from Paul Sabatier University, Toulouse, France. In 1983, she was hired as a permanent researcher by the National Center for Scientific Research (CNRS) to carry out research activities at the Laboratory of Analysis and Architecture of Systems (LAAS-CNRS) in Toulouse, France. From 1997 to 2005, she was heading the ESD research team. Since 2012, she is in charge of the “Energy Management” research area whose main activities focus on the integration of advanced power devices, passive components and DC-DC converters, energy-autonomous wireless sensor networks as well as on providing integrated ESD protection solutions for advanced CMOS and smart power technologies. Her major research interests are smart power integration issues (isolation technologies, protection against minority carrier injection, latch-up), design, modeling and characterization of protection structures against electrostatic discharges (ESD) for smart power and advanced CMOS integrated circuits and more recently, energy harvesting solutions for battery-free wireless sensors. She is author and co-author of five patents, 80 papers in refereed journals and more than 140 papers into international conferences. Since 2012, she is chairing the ESDA Academia committee.

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## Live Online Classes

5/13/2014 11:00 AM EST *Packaging Principles for the PrM Part3
6/10/2014 11:00 AM EST ESD Robust LDMOS Design Essentials (an IEW presented seminar)
6/19/2014 11:00 AM EST *System Level ESD/EMI – System Level ESD Testing & Evaluation to the IEC ESD Standard Part1
7/10/2014 11:00 AM EST * System Level ESD/EMI – System Level ESD Testing & Evaluation to the IEC ESD Standard Part2
7/15/2014 11:00 AM EST * Device Technology and FA Overview Part1
7/16/2014 11:00 AM EST * Device Technology and FA Overview Part2
7/17/2014 11:00 AM EST * Device Technology and FA Overview Part3
7/24/2014 11:00 AM EST *System Level ESD/EMI – System Level ESD Testing & Evaluation to the IEC ESD Standard Part3
8/7/2014 11:00 AM EST Texas Instruments-University ESD Research (Complimentary Webinar)

## On-Demand Online Classes

Advanced ESD/EMI Auditing Techniques
**Advanced HBM – Dealing with Tester Parasitics, High Pin Count, and Two Pin Testing
**CDM Testing Essentials
Charged Board Events: A Growing Industry Concern
*Cleanroom Considerations for the PrM 3 one hour sessions
Compliance Verification: Pitfalls of Auditing
Controlling ESD in Automated Equipment by Proper Grounding
Developing a Compliance Verification Program
Device Testing Correlation to Root Cause Failure Analysis
Electric Fields
Electrostatic Attraction
*Electrostatic Calculations for the PrM 4 one hour sessions
Electrostatic Discharge Effects In Integrated Circuit Technologies
**Essentials for Controlling the ESD Work Area
ESD Problem Solving
**ESD Fundamentals I for Stress Testing
**ESD Fundamentals II for Stress Testing
*ESD Standards Overview for the PrM 3 one hour sessions
**Fundamentals of Failure Analysis
**Fundamentals of System Level Testing
Grounding in an Electrostatic Protected Area
**HBM & MM Testing Essentials
Highlights and Key Concepts of Footwear/Flooring Standards
**High Speed Digital Oscilloscope Fundamentals
**HMM – System Level Testing of Components
Integrated Circuit ESD Fundamentals 3 hour class
*Ionization Issues and Answers for the PrM 3 one hour sessions
**Latchup Testing and Troubleshooting
Susceptibility Testing of Devices and Systems
**TLP Fundamentals – Understanding the Equipment Options and IV Data
The Good, The Challenges, and the Improvements in CDM ESD Testing
Ultra-Sensitivity Trends and CDM
**VF-TLP, An Introduction to Capabilities and Applications

*Taking all parts of this online class will fill the requirement for the full length tutorial that is a requirement of the ESDA Program Manager Certification curriculum. Details on the Professional Certification Programs offered by ESDA are on our website at www.esda.org/certification.html.

**This online class is required for Device Stress Certification. Details on Professional Certification Programs offered by ESDA are on our website at www.esda.org/certification.html. **This online class is an elective for Device Stress Certification. Details on Professional Certification Programs offered by ESDA are on our website at www.esda.org/certification.html.

## Calendar of Events

**May 6-8, 2014**
**Northeast Local Chapter Tutorials**
- **Class 0 Devices & Boards - ESD Controls and Auditing Measurements**
- **ESD Standards Overview for the Program Manager★★**
- **Packaging Principles for the PrM★★**
- **Ionization Issues and Answers for the PrM★★**
- **Flooring Selection: Uncovering Maintenance, Ownership and Performance Pitfalls**

Teradyne Conference Center 600 Riverpark Drive • North Reading, MA

**May 13, 2014 - ONLINE TRAINING**
**11:00 AM EST (One Hour Class)**
Packaging Principles for the PrM Part 3 ★★

**May 19-22, 2014**
**8th Annual International Electrostatic Discharge Workshop (IEW)**
Grand Hotel de Paris, Villard de Lans, France

**June 19, 2014 - ONLINE TRAINING**
**11:00 AM EST (One Hour Class)**
System Level ESD/EMI – System Level ESD Testing & Evaluation to the IEC ESD Standard Part 1 ★★

**July 10, 2014 - ONLINE TRAINING**
**11:00 AM EST (One Hour Class)**
System Level ESD/EMI – System Level ESD Testing & Evaluation to the IEC ESD Standard Part 2 ★★

**July 15, 2014 - ONLINE TRAINING**
**11:00 AM EST (One Hour Class)**
Device Technology and FA Overview Part 1 ★★

**July 16, 2014 - ONLINE TRAINING**
**11:00 AM EST (One Hour Class)**
Device Technology and FA Overview Part 2 ★★

**July 17, 2014 - ONLINE TRAINING**
**11:00 AM EST (One Hour Class)**
Device Technology and FA Overview Part 3 ★★

**July 24, 2014 - ONLINE TRAINING**
**11:00 AM EST (One Hour Class)**
System Level ESD/EMI – System Level ESD Testing & Evaluation to the IEC ESD Standard Part 3 ★★

**August 4-6, 2014**
**EOS/ESD Symposium for Factory Issues-Singapore**
Regional English Language Center (RELC),
30 Orange Grove Rd, Singapore 258352

**August 7, 2014 - COMPLIMENTARY WEBINAR (No Cost)**
**11:00 AM EST (One Hour)**
Texas Instruments-University ESD Research

**September 4-12, 2014**
**ESD Association Meeting Series**
**EOS/ESD Symposium and Tutorials ★**
Westin La Paloma, Tucson, AZ

**October 7-9 2014**
**ESD Device Design Essentials**
**Advanced ESD Characterization and Test Methods**
Fraunhofer Institution for Modular Solid State Technologies EMFT, Munich, Germany

**October 15-16, 2014**
**• Fundamental handling practices to reduce the risk of ESD damage**
**• Installing the most basic ESD control program (ESD Control on a shoestring budget)**
**• Simplified measurements to ensure that an ESD control program is working and a review of best practices used by major companies today.**
ESD Association, Rome NY

**October 28-29, 2014**
**Essentials for ESD Programs**
**Factory: Technologies • Controls • Procedures**
Holiday Inn City Center, Munich, Germany

**October 30 – 31, 2014**
**EOS/ESD Symposium for Factory Issues-Germany**
Holiday Inn City Center, Munich, Germany

**December 8-9, 2014**
**ESD Program Development & Assessment (ANSI/ESD S20.20 Seminar)**
ESD Association, Rome NY

★★ESD Certified Program Manager Course
★ESD Certified Device Stress Testing Course


Registration for onsite Tutorials available online at www.esda.org/onlineregistrations

## Photo Corner


ESDA friendships across the globe!

## Editorial Deadlines

*Threshold*™ is published six times a year by the ESD Association, a not-for-profit corporation. It strives for the advancement of theory and practice of electrical overstress avoidance and of allied arts and sciences and the maintenance of a high professional standing among its members and others.



*Threshold*™ Publication Schedule

| Issue | Deadlines |
|---|---|
| January/February | Nov. 19 |
| March/April | Feb. 1 |
| May/June | April 1 |
| July/August | June 1 |
| September/October | Aug. 1 |
| November/December | Oct. 1 |

**Threshold Institutional Listings**
Space in the Threshold Institutional Listings, which appear at the bottom of newsletter pages, can be purchased for $600.00 for six consecutive issues. Listings will also appear in the online calendar. Larger contributions are welcome. No agency fee is granted for soliciting such contributions. Inquiries, or contributions made payable to the ESD Association, should be sent to:
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