45th ANNUAL ELECTRICAL OVERSTRESS/ELECTROSTATIC DISCHARGE SYMPOSIUM CALL FOR PAPERS

Including the EOS/ESD Manufacturing Track

October 1-6, 2023 **Riverside Convention Center** **Riverside, CA, USA**

The EOS/ESD Symposium is dedicated to the understanding of issues related to electrostatic discharge and electrical transients/overstress, and the application of this knowledge to the solution of problems in consumer, industrial, and automotive applications, including electronic components, as well as in systems, subsystems, and equipment.

Special Focus Modules

Automotive

The electronics content in the automotive industry has increased rapidly in the last few years. The car electrification process is currently ongoing to reduce the environmental impact and the latest advancements in the autonomous driving and infotainment fields are bringing new complex systems with advanced technologies and new materials. The combination of stringent qualification requirements and highly demanding application needs is therefore defining new challenges for ESD design and innovative solutions must be identified. Inputs on all ESD/EOS topics related to the automotive field are solicited for this special focus module of the 2023 EOS/ESD Symposium.

Communications featuring Photonics

Power-efficient electronic devices capable of high-speed communication are essential in today's electronics-dominated world. At the same time, photonics is becoming the ultimate medium for high-speed optical communications with low latency, low energy consumption, and high speed, leading to end-to-end network paths. As all these applications become increasingly critical, the reliability of the communication designs becomes crucial. The complexity of the circuits required for ESD and EOS protection and mitigation continue to expand as well. We are seeking original works in various domains of communication, such as IoT, RF, 5G, photonics, HSS, etc. that contain a range of technologies from advanced to mature silicon-based technologies to Si-photonics.

Emerging Technologies

The scaling of CMOS technologies continues with a clear outlook beyond the current 3 nm nodes. 2.5D and 3D packaging technologies become mainstream and enable previously unseen product performance. The use of advanced technologies, high application performance, and heterogeneous integration concepts brings up new challenges for the ESD protection design. This requires a deep understanding of technology and the use of powerful EDA tools for ESD modeling and design verification. For the 2023 EOS/ESD Symposium we are looking for original publications that showcase the advances and challenges at the technological level.

Device Testing and Characterization

Innovative trends such as technology scaling, Ultra-Wide Band RF, and multi-dimensional packaging continue to drive complexity for ESD solutions. These trends and the accompanying complexity of ESD protection solutions will in turn, drive innovations in ESD device testing and characterization. Understanding the underlying device physics is the best way to meet these challenges. However, conventional ESD characterization methods are often inadequate to provide this understanding. Publications that report on innovative testing and characterization methods or techniques being used to probe these advanced protection circuits are solicited.

EMC & ESD Co-Design

The solutions to address conflicting EMC and ESD problems often require co-design efforts, leading to innovative solutions at the component and system level while meeting design targets with minimal trade-offs. The problems requiring co-design can be situations such as harmonic generation issues due to ESD protection components on high-speed interfaces, reducing EMI on interfaces while protecting against ESD transients, and maintaining signal integrity. We are looking forward to interesting EMC/EOS/ESD co-design problems and solutions in this special focus module for the 2023 EOS/ESD Symposium.

GaN and SiC in Power and RF Applications

Wide-bandgap (WBG) semiconductors, such as gallium nitride (GaN) and silicon carbide (SiC) are driving radical transformation in power electronics, LEDs, and communications. When compared to silicon, the superior physical and electronic properties such as higher efficiency and switching frequency, higher operating temperature, and higher operating voltage make WBG semiconductors ideally positioned for use in electrical vehicles, solar, and other clean and eco-friendly energy sources. These fast-growing application areas for WBG include opportunities as discrete ESD solutions. At the same time, many applications require innovative approaches to meet ESD manufacturing robustness targets. Inputs in this emerging area of research are solicited in this special focus module.

Submission Options

Technical Paper	Technical Poster
Abstract: 2-4 pages	**Abstract:** 1-2 pages
Final Manuscript: 6-10 pages	**Final Manuscript:** 3-5 pages
Presentation: Maximum 20 slides	**Presentation:** Maximum 10 slides

Abstract (Paper/Poster) submission due February 6, 2023: Your original 50-word abstract and summary of work to be expanded in a full technical paper or a technical poster must clearly and concisely present specific results and explain the importance of your work in the context of prior work. Authors are required to use the applicable abstract submission template available at https://www.esda.org/events/45th-annual-eosesd-symposium-and-exhibits. The final classification of abstracts as full technical papers or technical posters is at the discretion of the technical program committee. Full manuscripts of accepted technical papers and technical posters will be due before the conference. Registration for the conference is required for the author presenting the paper.

The technical program committee accepts unpublished technical papers/posters for peer review with the understanding that the author will not publish the work elsewhere prior to presentation at the Symposium. Presentation of your work at the earlier International ESD Workshop (IEW) will not preclude your EOS/ESD Symposium abstract submission. The submission must follow guidelines and be expanded significantly for the EOS/ESD Symposium. Publication of accepted papers/posters in any form prior to presentation at the Symposium may result in the paper being withdrawn from the Symposium Proceedings. Authors must obtain appropriate company and government clearances prior to submitting an abstract.

Suggested Submission Topics

Advanced CMOS (Analog/Digital) EOS/ESD and Latch-up

- ESD Issues in Advanced Technologies (Multi-gate, FinFET, SOI, SiGe, Compound, Graphene, nanowire, etc.)
- On-Chip ESD Protection Devices & Techniques in Advanced CMOS Technologies
- IC Design and Layout Issues
- Circuit Simulation of EOS/ESD Events in Advanced CMOS Technologies
- DC/Transient Latch-up Issues and Solutions, Troubleshooting, Simulation
- ESD Issues in 2.5D & 3D Stacking and TSV

ESD Protection in Bipolar, RF, High Voltage, and BCD Technologies

- ESD Issues in Bipolar, RF, High Voltage, and BCD Technologies and Power Technologies (SiC, GaN, etc.)
- On-Chip ESD Protection Devices & Techniques in Bipolar, RF, High Voltage, and BCD Technologies
- IC Design and Layout Issues
- Circuit Simulation of EOS/ESD Events in Bipolar, RF, High Voltage, and BCD Technologies
- DC/Transient Latch-up Issues and Solutions, Troubleshooting, Simulation
- ESD Circuit Simulation and Co-Design

Numerical Modeling and Simulation for On-Chip ESD Protection

- ESD Device TCAD Simulation
- Simulation Tool and Methodology
- Numerical Modeling and Physics of EOS/ESD Events
- TCAD/Circuit Co-simulation

EOS/ESD Failure Analysis, Troubleshooting, and Case Studies

- EOS/ESD Case Studies, Reviews, and Analysis
- EOS/ESD Phenomena in MEMS (Microelectromechanical Systems)
- Failure Analysis Techniques and Interpretations
- EOS/ESD Component Failure Analysis
- Testing of MR/TMR Heads and Ultra-Sensitive Devices
- EOS/ESD Protection for Aircraft, Spacecraft, and Avionics

Device Testing: Testers, Methods, and Correlation Issues

- Novel EOS/ESD Test and Characterization Methods
- Transmission Line Pulse Testing Systems
- Novel TLP Measurement Results
- HBM, CDM Tester Issues and Solutions
- Tester Correlation Issues
- Standards – Round-Robin Testing, Results, and Analysis

System Level EOS/ESD/EMC, HMM

- System Level EOS/ESD/EMC Test Methods
- System Level EOS/ESD Modeling and Simulation
- EOS/ESD Simulators, Calibration, and Correlation
- Transient ESD/EMI Induced Upset
- Case Studies, Reviews, and Analysis
- Standard Test Boards as an Early Measure of Robustness

Chip/Module/Package EOS/ESD Electronic Design Automation

- Novel EOS/ESD EDA Tools
- ESD Checking and Verification Methodology
- Application of EDA tools for EOS/ESD Failure Analysis, Design, and Verification

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