

# CALL FOR PAPERS

IEEE INTERNATIONAL INTEGRATED RELIABILITY WORKSHOP

# IIRW

IEEE

INTERNATIONAL INTEGRATED  
RELIABILITY WORKSHOP

**October 8-12, 2017**

**Stanford Sierra  
Conference Center  
Fallen Leaf Lake,  
CA, USA**

**Abstract Deadline**  
July 10, 2017

**Late News Deadline**  
August 21, 2017

**General Chair:**  
Tom Kopley  
ON Semi, USA

**TPC Chair:**  
Luca Larcher  
U. Modena, Italy

**For More Information:**  
[www.iirw.org](http://www.iirw.org)

The **IEEE International Integrated Reliability Workshop (IIRW)** focuses on ensuring electronic device reliability through fabrication, design, testing, characterization, and simulation, as well as identification of the defects and physical mechanisms responsible for reliability problems.

**Outstanding features** of the IIRW are

- Strong plenary, invited, and tutorial presentations
- Strong technical program (platform and posters)
- Unparalleled opportunities to meet world-leading experts
- Discussion and special interest groups
- Unique rustic and secluded environment

**IIRW 2017** invites abstracts related to the reliability of

- Gate/Interconnect dielectrics (SiO<sub>2</sub>, SiON, high-k, low-k)
- Conventional and emerging memory devices (RRAM, etc.)
- CMOS, non-CMOS (III-V), and novel devices
- MEMS and other sensors
- Transistor reliability (hot carriers, NBTI/PBTI, TDDB)
- Defects
- Modeling and simulation of reliability issues
- Interconnects
- Impact of transistor degradation on circuit reliability
- Design-in reliability (products, circuits, systems, processes)
- Customer/manufacturer product reliability requirements
- Wafer level reliability tests
- Single event upsets and irradiation related reliability issues

**Your two page abstract should state clearly and concisely the results of your work and why they are significant. Representative data and figures that support your proposal are REQUIRED.**

Please submit your abstract [here](#).

For more information, contact the technical program chair:

**Luca Larcher**

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