Physical Process, Device and Circuit Simulation (TCAD) in Application to Industrial ESD R&D

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Tutorial Goals

- Deliver the concept of a new effective alternative TCAD approach for industrial ESD design and demonstrate the methodology on representative simulation examples

- Promote the Physical Approach for industrial ESD design:
  - Guess the physical mechanisms or effects
  - Setup simulation representing the guess
  - Simulate (calculate and compare the consequences)
  - Verify by experiment defined upon simulation

- The learning is based on multiple examples to explain:
  - How to transform ESD design challenges at all levels into simulation problem statements
  - How to perform numerical simulation and comparative data analysis
  - How to apply the simulation results to define the experiments and to resolve the design challenges
Outline

• Introduction
  • Industrial ESD design
  • Traditional and alternative TCAD approach.

• A novel TCAD workflow to address the technology needs

• Examples of analysis at different ESD design levels
  • Conductivity modulation in semiconductor structures
  • Standard and ESD devices
  • ESD clamps and network
  • Analog product cases, system level and foundry

• Conclusions
Advanced Workflow as Combination of Traditional and Alternative TCAD

- Traditional approach to obtain the parameters for diffused profiles
- Parameterized TCAD approach to generate parameterized devices and circuits
Summary

• A novel way to address physical design of ESD device and circuit solutions is fully validated for application to analog IC products design

• This new advanced methodology utilizes:
  • One time input from physical process simulation for single mask implant profiles
  • Extraction of the diffused profile parameters: vertical – Gaussian; lateral – error functions
  • Or alternative fitting from SIMS and electrical data for foundry processes
  • One time made parameterized device templates to generate FEM devices
  • Mixed-mode analysis with simultaneous variation of the circuit and device parameters
  • Circuit and device optimization loops.

• The methodology is already widely used for a broad spectrum of ESD IP development from HV system level solutions to LV nano scale devices