Tutorial DD221/FC221
Correlation of ESD Robustness and Handling Threats

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Purpose

• Understand the ideas of the basic ESD qualification models as e. g. Human Body Model, Charged Device Model, ...
• Learn typical failure modes and understand which waveform parameters of the models are decisive
• Learn some basic measurement methodologies of charging/discharging in a manufacturing environment
• Get familiar with the waveforms of typical “real-world” ESD events and understand how to assess the waveforms with respect to device qualification tests
Outline

• Motivation: ESD standards and qualification
• Process assessment
• The five “most important” ESD stress scenarios
  – Human Body Model
  – Machine Model
  – Charged Device Model
  – JEDEC JESD78 latch-up
  – ESD system level tests
    (e.g. IEC 61000-4-2)
• Do these stress scenarios cover all possible “real world threats”? 

• Intention, model, waveform
• Target levels
• Fails in testing and in field
• Correlation testing/field
  • How can we measure “real world threats”?
  • Consequences
Motivation
ESD Qualification

- Qualification procedures define the model (= the standard) and the target threshold level
- Target levels (in kV) are decreasing based on product analysis and improved ESD control measures
- BUT: What means “kV”?  
  - Voltage in tester defines stress current depending on test set-up
  - Voltage in process is depending on process and measurement method
- A lot of money is spent for ESD (testing, protection measures)!

→ Is this already sufficient to avoid field returns?
Summary

- **Human Body Model** and **Charged Device Model** testing can reproduce different field fails caused by handling; qualification tests are worst case
  - HBM and CDM robustness levels are absolutely useful for production and assembly lines
- *(Static) latch-up* is mandatory to avoid field fails
- ESD system level tests (e.g. IEC 61000-4-2) are inevitable; however, often very difficult to correlate with field problems
- **New test methods** (e.g. Transient Latch-up, Charged Board Event, Cable Discharge Event) are required to address “new” failure mechanisms