DD103: An Overview of Integrated Circuit ESD:
The ESD Threat, Testing, Design Concepts and Debugging

Alan Righter

Warren Anderson
Outline

• Introduction
• ESD Definitions, Electrostatics, and ESD Basic Concepts
• ESD Stress Models and Standards
• Introduction to Transmission Line Pulse (TLP)
• ESD Design Window and ESD Protection Network Design
• Power Clamps and Tradeoffs
• Input Protection and Output Drivers
• RF ESD Protection
• Integration Issues
• CDM Protection Guidelines
• ESD Design Verification
• Conclusions
Introduction

• This tutorial was created for IC designers and other non-ESD engineers who do not have a working knowledge of ESD
• This tutorial will provide the fundamentals to enable them to more easily integrate ESD protection into their designs
• This tutorial will be useful for a wide range of specialists
  – I/O designers
  – Layout designers
  – Test engineers
  – Failure analysis engineers
  – Quality and reliability engineers
  – Architects
• The student will
  – Understand the fundamentals of ESD design
  – Know the variables that affect ESD robustness
  – Understand why ESD design needs to be addressed early in the IC design cycle
  – Understand ESD testing
  – Be able to interpret failure analysis data
  – Improve interactions with ESD design specialists
Conclusion

• This tutorial will cover the basics of
  – Electrostatics and ESD controlled workspaces
  – Testing of integrated circuits for ESD robustness
  – The fundamentals of IC ESD design
  – Verification of ESD design
  – Fundamentals of ESD debugging

• This tutorial will enable you to
  – Know the fundamental issues of ESD
  – Better prepare you to interact with experts
  – Understand how ESD needs to be considered within the design flow