

TABLE OF CONTENTS

1.0 INTRODUCTION	1
1.1 PURPOSE	1
1.2 SCOPE	1
2.0 USER GUIDES	1
2.1 CONTACT AND GROUNDING ISSUES DURING TLP TESTING	2
2.2 OSCILLOSCOPE CORRECTIONS	6
2.3 TLP CALIBRATION.....	7
2.4 BURN-IN, INITIAL PULSES TO REDUCE CONTACT RESISTANCE.....	11
2.5 TEST FIXTURES	13
2.6 MEASUREMENT WINDOW SELECTION.....	15
2.7 BIASED TLP MEASUREMENTS	18
2.8 TLP LOAD LINES AND SNAPBACK DEVICES	23
3.0 APPLICATION GUIDES	28
3.1 CORRELATION BETWEEN HBM AND TLP	28
3.2 CORRELATION BETWEEN TLP AND ESD SYSTEM LEVEL STRESS	30
3.3 CHARACTERIZATION FOR SYSTEM EFFICIENT ESD DESIGN (SEED).....	33
3.4 POWER PROFILE TLP	35
3.5 MOS SAFE OPERATING AREA CHARACTERIZATION USING TLP	37
3.6 GATE OXIDE CHARACTERIZATION.....	40
3.7 STOP & GO TLP	43
3.8 REPETITIVE TLP	45
 Figures	
Figure 1: Basic Connection Scheme	2
Figure 2: 4-Point-Kelvin Connection Scheme	3
Figure 3: Connection Scheme with Additional DC Bias Signals	4
Figure 4: Voltage Transients Measured with and Without Correct Ground Connection	5
Figure 5: TLP I-V Curves of a 5-Ohm Resistor before and after Signal Path Compensation	6
Figure 6: Uncorrected TLP Data.....	7
Figure 7: Components in Blue Dealt with by the Correction	8
Figure 8: Circuit Models of Correction Needed	8
Figure 9: Correction Rotation and Calibration Stretching Data Points	9
Figure 10: Components in Orange Dealt with by the Calibration	9
Figure 11: Typical I-V Plot of Short (Blue Curve) Calibration Caused by Oxides on Tungsten Needles.....	11
Figure 12: Typical I-V Plot of Short Calibration with Osmium Tip Needles	12
Figure 13: Coaxial RF Probe with a Single Probe Needle for the Signal with a Clip and Flexible Connector Connected to a Second Probe Needle to be Used for the Ground Connection.....	13

Figure 14: Example of Wafer Probes for Carrying a Balanced TLP Signal to Two Wafer Probe Needles.....	14
Figure 15: Comparison of the Same 100 ns TLP Data on a 1-Ohm Resistor Using a Single Point, 7 Points Over in a 2.8 ns Window, and 51 Points in a 20 ns Window	15
Figure 16: Example of Waveform with Ringing and Suggested Measurement Window	16
Figure 17: Sample of TLP I-V Curves Taken with Different Time Windows.....	17
Figure 18: Illustration of the Problem of Applying a TLP Stress to a Biased Node and use of a Bias Tee to Overcome the Problems.....	18
Figure 19: Configuration A - Kelvin or Pseudo Kelvin Measurement in Which the Voltage Probe is on the DUT side of the Bias Tee; Configuration B – a TDR Setup in Which the Voltage and Current Probes are on the TLP Pulse Source Side of the Bias Tee	19
Figure 20: TDR TLP Measurements of a Zener Diode Without a Bias Tee and with a Bias Tee with Voltages of 0 to 5 Volts Without Correction Factors	20
Figure 21: TDR TLP Measurements of a Zener Diode Without a Bias Tee and with a Bias Tee with Voltages of 0 to 5 volts with Correction for Bias Voltage but not for Voltage Build up Across the Capacitor or Resistance in the Bias Tee	20
Figure 22: TDR TLP Measurements of a Zener Diode Without a Bias Tee and with a Bias Tee with Voltages of 0 to 5 Volts with Correction for Bias Voltage and Voltage Across the Bias Tee but no Correction for Resistance in the Bias Tee.....	21
Figure 23: TDR TLP Measurements of a Zener Diode Without a Bias Tee and with a Bias Tee with Voltages of 0 to 5 Volts with all Corrections.....	21
Figure 24: Kelvin TLP Measurements of a Zener Diode with and Without a Bias Tee with Voltages of 0 to 5 Volts with no Corrections Needed.....	22
Figure 25: Equivalent Circuit for a TLP Tester	23
Figure 26: Three Load Line Examples for Several DUT Resistances.....	24
Figure 27: Schematics of Two TLP Systems with Different Impedances.....	25
Figure 28: Schematics for Calculating Load Line Resistance	25
Figure 29: Low-Current TLP Measurements of a TVS with a Large Snap-back Using Both a Standard TDR System and a High Impedance System	27
Figure 30: Correlation Plots of HBM Failure Voltage and TLP Failure Current	29
Figure 31: ESD System Level Stress Pulses with Two Different Discharge Networks	30
Figure 32: High-Current Characterization of DP USB Signal Pin.....	34
Figure 33: TLP Characteristics with Different Pulse Durations	35
Figure 34: Power-to-Failure vs. Pulse Duration	36
Figure 35: Gate Bias Setup for Electrical SOA Measurements.....	37
Figure 36: Gate Bias Setup for Electrical SOA Measurements.....	38
Figure 37: MV NMOS device SOA characterization.....	38
Figure 38: HV NMOS device SOA characterization	38
Figure 39: Schematic Representation of the Three Main Different Characterization Methods of Gate Oxides.....	40
Figure 40: Set-up Configuration Used for the Gate Oxide Time Dependent Dielectric Breakdown Experiments.....	41
Figure 41: Pulse Waveform for a 4.64-Volt Stress Sensed at the Gate.....	41
Figure 42: Voltage Acceleration for nFET at 25°C	42
Figure 43: Three Consecutive TLP Runs on a Polysilicon Resistor.....	43
Figure 44: TLP Characteristics of Two Consecutive Runs on the Same DUT.....	44

Figure 45: Step Size Effect in 1 ns (VF-)TLP Testing on LVTSCR; and 100 ns-TLP Characteristics for 2 HV ggNMOSTs, One of Which Shows a Clear Progressive Soft Leakage..... 45

Figure 46: Leakage Current vs. Number of Pulses at 3 Fixed Current Levels for the ggNMOSTs of Figure 40; and Wear Out Effect in Metal Line Resulting from Repetitive 100 ns TLP Stress 46

Figure 47: Wear-Out Plot - Failure Level vs. Number of Pulses 46

Tables

Table 1: Calculations of TLP Impedance Using a 200-Volt TLP Voltage, 50-Ohm R_{Cable} , 500-Ohm R_{Series} , and 50-Ohm R_{Scope} 26