# TABLE OF CONTENTS

1.0 PURPOSE ........................................................................................................................................... 1

2.0 INTRODUCTION ................................................................................................................................... 1

3.0 ESD CHECKS THROUGHOUT IC DESIGN FLOW .............................................................................. 2

   3.1 PRODUCT DEFINITION PHASE ........................................................................................................ 3

   3.2 CHIP ARCHITECTURE PHASE ......................................................................................................... 4

   3.3 MODULE AND FULL IC DESIGN PHASE .......................................................................................... 4

      3.3.1 Floorplanning of the Chip Architecture Modules and the Standard Digital I/O and Power Banks .............................................................................................................. 4

      3.3.2 Design of IP Modules and Analog I/O Pad Rings .................................................................. 4

      3.3.3 Full Chip IP and I/O Integration, Including Package ............................................................ 5

   3.4 DESIGN QUALIFICATION PHASE .................................................................................................. 5

4.0 BASIC ESD CONCEPTS ....................................................................................................................... 6

   4.1 ESD DESIGN WINDOW .................................................................................................................. 6

   4.2 SINGLE DEVICES FAILURE CONDITIONS .................................................................................. 7

      4.2.1 Passive Elements .................................................................................................................... 8

      4.2.2 Diodes ................................................................................................................................... 9

      4.2.3 Bipolar Transistors .............................................................................................................. 10

      4.2.4 MOS Transistors ................................................................................................................. 11

   4.3 GENERIC TOPOLOGY FAILURE CONDITIONS ............................................................................. 12

      4.3.1 Serial Connections .............................................................................................................. 12

      4.3.2 Parallel Connections ........................................................................................................... 13

   4.4 ESD PROTECTION TOPOLOGY FAILURE CONDITIONS ............................................................. 14

   4.5 OVERVIEW OF ESD PROTECTION APPROACHES .................................................................... 16

      4.5.1 ESD Protection Devices ....................................................................................................... 16

      4.5.2 ESD Protection Circuits ....................................................................................................... 17

5.0 VERIFICATION OF CIRCUITS TO BE PROTECTED FROM ESD .................................................. 20

   5.1 VERIFICATION OF CIRCUITS THAT CANNOT SHUNT ESD ENERGY ....................................... 20

      Rule 5.1.1 Verify Protection of Pad-Connected Gate Oxides .......................................................... 20

      Rule 5.1.2 Verify Protection of Decoupling Capacitors (VDD-VSS) ............................................. 24

      Rule 5.1.3 Verify Protection of Gates along Power Cross Domains Paths .................................... 25

      Rule 5.1.4 Verify Protection of Weak Devices (e.g. DeNMOS, LDMOS, Small Width Devices, etc.) ......................................................................................................................... 27

   5.2 VERIFICATION OF CIRCUITS THAT ARE REQUIRED TO SHUNT ALL ESD ENERGY ............. 30

      Rule 5.2.1 Verify Self-Protecting Transistors (e.g. I/O Buffer) have Appropriate Parameters (Width, Gate Length, Metal Routing, etc.) ................................................................. 31

      Rule 5.2.2 Verify Self-Protecting Embedded/Body Diodes have Appropriate Parameters (Perimeter, Anode-Cathode Spacing, Metal Routing, etc.) ....................................................... 31

      Rule 5.2.3 Verify Self-Protecting Capacitors have Appropriate Capacitance .................................. 31
5.3 VERIFICATION OF CIRCUITS THAT ARE ABLE TO SHUNT A PORTION OF THE ESD ENERGY

Rule 5.3.1 Verify Avoidance of Big Buffer Topologies Forming Low Impedance Path during ESD

Rule 5.3.2 Verify Avoidance of Parasitics Forming Low Impedance Path During ESD

Rule 5.3.3 Verify Avoidance of any Topologies with Ability to Sustain ESD Current in Normal Device Operating Mode (Diode, BJT, FET, Mixed-Voltages) Forming Low Impedance Path during ESD

6.0 VERIFICATION OF ESD PROTECTION NETWORK INTEGRATION

6.1 CELL LEVEL ESD CHECKS

Rule 6.1.1 Verify that Correct Version of the Device/Design Kit/Cell/Library is being used when using Standard Library Cells or Parameterized Cells (PCELLs)

Rule 6.1.2 Verify Compliance of Individual and Multiple Cell Devices with ESD Geometrical Rules

Rule 6.1.3 Verify ESD Protection Element between I/O and Power (VDD, VSS) Rails, including Correct Device Polarity, within I/O Cell

Rule 6.1.4 Verify Power Clamp Between Power Rails (VDD, VSS), Including Correct Device Polarity, within I/O or Supply Cell

Rule 6.1.5 Verify Trigger Circuit Implementation in Transient-Triggered Designs

Rule 6.1.6 Verify Termination Cell Implementation

Rule 6.1.7 Verify Interface Cell Implementation

Rule 6.1.8 Verify Device Rating Compliance in Cell Implementation

Rule 6.1.9 Verify Robustness of Metal Lines and Interconnects along the ESD Protection Discharge Path

Rule 6.1.10 Verify Compliance of Extracted Metal Resistances of the Paths within the Cell with Allowed Design Limits

Rule 6.1.11 Verify Implementation of Secondary ESD Protection Scheme

6.2 INTRA POWER DOMAIN ESD CHECKS

Rule 6.2.1 Verify that the Correct Type and Most Recent Version of I/O Cell is used in the I/O Bank

Rule 6.2.2 Verify the Compliance with I/O Placement Rules for ESD Distributed Schemes

Rule 6.2.3 Verify the Presence of Intended ESD Current Path for Each Pin-Pair Combination within an I/O Bank

Rule 6.2.4 Verify Robustness of Metal Lines and Interconnects for all ESD Discharge Paths within an I/O Bank

Rule 6.2.5 Verify Compliance of Estimated Bus Resistance Between Pad and ESD Cell/Device in an I/O Bank

Rule 6.2.6 Check the Integration of ESD Protection Elements and Bumps/Bondpads

Rule 6.2.7 Verify the ESD Triggering and Clamping Characteristics taking into Account Power Domain Capacitance

Rule 6.2.8 Perform First Order Evaluation of ESD Robustness by Calculating Pad Voltage for ESD Stress within the I/O Bank

6.3 INTER POWER DOMAIN ESD VERIFICATION
Rule 6.3.1 Verify that the Correct Type and Most Recent Versions of ESD Cells Between Power Domains are used ................................................................. 78
Rule 6.3.2 Verify the Presence of Intended ESD Current Paths Between any Pin Pairs Belonging to Different Power Domains ........................................ 78
Rule 6.3.3 Verify Placement/Connectivity of Correct ESD Cells Between Power Domains ........................................................................................................ 80
Rule 6.3.4 Verify Metal Width and Interconnect for Routes Between Power Domains, Including ESD Cells Along the ESD Discharge Path ......................... 82
Rule 6.3.5 Verify Compliance of Estimated Bus Resistance Between Two Pads in Different Power Domains with Design Limits ........................................ 86
Rule 6.3.6 Perform First Order Evaluation of ESD Robustness by Calculating Pad Voltage for ESD Stress Between Power Domains ................................ 87

6.4 PACKAGE LEVEL ESD CHECKS ......................................................................................................................... 90
Rule 6.4.1 Verify the Integrity of the Overall ESD Protection Network Achieved at Package Pin Level .................................................................................................. 90
Rule 6.4.2 Verify that Package RLC Network is Compatible with Overall ESD Protection Scheme ......................................................................................................... 93
Rule 6.4.3 Verify the Integrity of the Overall ESD Protection Network Achieved at Package Pin Level when Having Multi-Die (System in a Package) Designs .......... 95
Rule 6.4.4 Verify that CDM Peak Current of the Package-Die System is Below the Maximum CDM Current Tolerated by the IC .................................................. 96

7.0 OVERVIEW OF ESD EDA VERIFICATION APPROACHES ......................................................... 99
8.0 CONCLUSIONS ......................................................................................................................................................... 104
9.0 ACKNOWLEDGEMENTS ............................................................................................................................................ 104
10.0 GLOSSARY/DEFINITIONS ................................................................................................................................. 104
11.0 REFERENCES ........................................................................................................................................................... 107

TABLES
Table 1. Cell Level ESD Check Summary ................................................................................................................. 43
Table 2. Example of an RC-Triggered Clamp Design Specification ........................................................................... 50
Table 3. ESD EDA Rules Summary .......................................................................................................................... 101

FIGURES
Figure 1: Simple ESD Verification Flow Mapped to Sample IC Design Flow and Referenced to Rules ................................................................. 2
Figure 2: Generic ESD Design Window ....................................................................................................................... 6
Figure 3: Wunsch-Bell Model for Power to Failure vs. Time to Failure ...................................................................... 7
Figure 4: Voltage Acceleration of NFET Stressed in Inversion for Seven Oxide Thicknesses (6.85 to 1.1 nm) ................. 8
Figure 5: Generic Two-Pin Representation of Passives ......................................................................................... 8
Figure 6: Generic Two-Pin Representation of Diodes. .......................................................... 9
Figure 7: Generic NPN Bipolar Representation. .................................................................. 10
Figure 8: Generic MOS Representation. ............................................................................ 11
Figure 9: Generic Serial Connection. .................................................................................. 12
Figure 10: Example Topology for Serial Connection. ............................................................ 13
Figure 11: Generic Parallel Connection of Basic Element. .................................................... 13
Figure 12: Example Topology for Parallel Connection. .......................................................... 14
Figure 13: Design Case with ESD Energy Shunted Through the ESD Clamping Device. ...... 15
Figure 14: Design Case with ESD Energy Shunted Through the Circuits to be Protected. ...... 15
Figure 15: Design Case with ESD Energy Shared Between the ESD Clamp Circuit and the Circuit to be Protected. .............................................................................. 16
Figure 16: ESD Elements with Various Triggering Mechanisms. ......................................... 17
Figure 17: Rail Clamp vs. Local Clamp Based Protection Approaches. ................................. 18
Figure 18: Using Low Resistance Master VSS Bus vs. APD Connected Ground Domains. .... 19
Figure 19: Breakdown Voltage Acceleration as a Function of the Physical Oxide Thickness for NFET and PFET Stressed at 25°C in the HBM Range of Time for a Normalized Size of 1.2 μm². ........................................................ 21
Figure 20: Pad-Connected Gate Oxide................................................................................... 21
Figure 21: Generic Secondary Protection Element to Reduce Voltage Built Across a Gate Oxide.................................................................................................................. 23
Figure 22: As the Parasitic Resistance from the Primary ESD Protection Element to VSS Pad Exceeds a Critical Value, the Need for a Secondary ESD Protection Element to the Input Arises .................................................................................. 23
Figure 23: Decoupling Capacitor Example (VDD-VSS). .......................................................... 24
Figure 24: Example Case of Decoupling Cap Insertion for Flip-Chip ESD Protection in I/O ..... 25
Figure 25: Typical Signal Cross-Domain ESD Issue. ............................................................... 25
Figure 26: Simplified Cross-Domain Resistive ESD Network Model ................................ 26
Figure 27: Full-Chip Cross-Domain Voltage Map for Stress Between Domain 3 and Domain 1, with Indication of Over-Voltage Situation at the I/O Interface of Domain 1.............. 26
Figure 28: Screenshot of the Results of the Cross-Domain Schematic Checking Tool, Highlighting an NFET Device (N10) Whose Terminals are Connected to Two Different Power Domains. ........................................................................ 27
Figure 29: Illustration of ESD Shell Models for MOSFETS.................................................... 28
Figure 30: Tool Flow Chart.................................................................................................. 29
Figure 31: ESD Verification Flow From.................................................................................... 29
Figure 32: A Cross-Section Image of the Parasitic Bipolar that can be Formed when an N-Well is Connected to an I/O Pad that is too Close to Another N-Well Connected to a Different Pad ................................................................. 30
Figure 33: Screenshot of the DRC Tool Results Showing Error Regions Where an N-Well Resistor is Placed too Close to a PFET ........................................................................... 30
Figure 34: Generic Representation of Distributed Decoupling Capacitors Between Power Supplies .................................................................................................................. 32
Figure 35: Generic Ballasting Resistor to Protect a Topology Able to Withstand a Finite Current During ESD Conditions. ......................................................................... 33
Figure 36: “Big-Buffer” ESD Example .................................................................................. 34
Figure 37: Instruction Set Example in a Commercial Tool to Screen out Big-Buffer Topology in a Design Netlist ......................................................................................... 35
Figure 74: ESD Distributed Scheme Verification ................................................................. 63
Figure 75: Floorplan Example of Different I/O Cells for I/O Ring Layout ......................... 64
Figure 76: Example Placement of the Clamp (M1), Trigger Circuit (T) and Decoupling Capacitor (C1) I/O Cells in a Self-Protecting 24 I/O Bank .................................................. 64
Figure 77: Checking Missing ESD Protection Between VDD and VSS When I/O 1 and I/O 2 Share the Same Power/Ground Domains ....................................................... 65
Figure 78: Lacking of Both a Supply Clamp Cell and a Supply Controller Highlighting Rule 6.2.3 Violation ........................................................................................................ 65
Figure 79: Typical I-V Curve for a Snapback Clamp and I-V Curve for a Diode is a Degenerate Case with Vh=Vt1 .................................................................................. 66
Figure 80: Current Density Check of an HBM/MM Event with Diodes/Clamps Represented as I-V Curves ........................................................................................................... 66
Figure 81: ESD EM Map Shows the HBM Failure on P2 and AVSS Nets ................................. 67
Figure 82: Schematic Illustration of Metal Bus Resistance Between a Pad and ESD Device .. 67
Figure 83: Methodology Steps to Verify ESD Protection Network Using Validation Software to Analyze the Design Netlist ................................................................. 68
Figure 84: Software Highlights Parallel Power Clamps in Discharge Paths from Vdde Pad to Vsse Pad ................................................................. 68
Figure 85: Example of Rule 6.2.6 Showing that any VDD/VSS Bump Should be Electrically Close to an ESD Protection Element Within Rcrit Ohm ........................................ 70
Figure 86: Flip-Chip Example ............................................................................................ 70
Figure 87: Resistance Check Methodology Flow Diagram .................................................. 71
Figure 88: Simulation Flow Diagram of Software Tool for Full Chip ESD Network Verification ......................................................................................................................... 72
Figure 89: Detailed ESD Event Analysis Highlighting the Most Critical Layers, in Terms of Resistance or Current Density Violation ......................................................... 72
Figure 90: Visualization of the Current Crowding Issues that were Observed in the M9 Layer .. 73
Figure 91: Example of Rule 6.2.7 ........................................................................................ 74
Figure 92: Substrate Modeling for 3-D Mesh of RC Extraction and Distributed Well-Diode and Hooked up to Metal Grid RLC Network ......................................................... 74
Figure 93: CDM Failure Test Case with -500 Volt Zap on IOP Pin ......................................... 75
Figure 94: Power/Ground Grid RLC, Signal Coupled RC, Substrate RC, Well Diodes, Package RLC, and Pogo Pin RLC are Considered in the ESD CDM Simulation During a CDM Event .............................................................................................................. 75
Figure 95: Example of Pin to Pin Stress Condition on a Simple I/O Ring ............................. 76
Figure 96: Example of Rule 6.2.8 ........................................................................................ 77
Figure 97: Schematic of a Power Domain with Parallel Power Clamps and the Set of Two Piece-Wise Linear I-V Characteristics of the Power Clamps used for the Permutation Method ................................................................. 77
Figure 98: Typical Multiple Power Domains Implementations .......................................... 79
Figure 99: Circuit with Negative Supply Rail in Different Hierarchy ..................................... 80
Figure 100: A 5-Volt VDD is Protected Against its Neighboring 3.3-Volt VDD by a Grounded-Gate FET (ggFET) .................................................................................................. 81
Figure 101: Anti-Parallel Diodes Between Neighboring VDD Busses Creates a Short and Robust ESD Protection Path .................................................................................. 81
Figure 102: An Example Checking the Discharge Path Between Two I/O in Different Power Domains as Per Rule 6.3.4 .......................................................................................... 82
Figure 103: Screenshot of the Results of the Current Density-Based Tool Run, Showing Regions of High Current Spots Greater than the Allowed Maximum Current Densities in a Metal Bus .................................................................82
Figure 104: Optical Image of a Part After Failure Analysis, Showing Regions of BEOL Failure Matching the Predicted Failure Regions by the Current Density-Based Tool ..........83
Figure 105: Layout and Simulated Current Densities in the Top Metal Layers and Vias of an Input Circuit Containing a Pad, Two ESD Diodes, and Two Power Nets.................83
Figure 106: Current Densities in Selected Layers Over the Top Half of Np-Pw ESD Diode ....84
Figure 107: A 3D View of the Low-Capacitance Pad.............................................................................84
Figure 108: Individual Metal Layers Contributions (In Percent) to Total Pad Capacitance ........85
Figure 109: Flowchart of Verification ESD Tool .............................................................................85
Figure 110: A Diagram Showing the Shortest ESD Path Found by the Verification ESD Tool .......86
Figure 111: Estimating the Total Bus Resistance of the Bussing Connections Between Pads Belonging to Different Power Domains..................................................................................87
Figure 112: An Example of I/O Ring Analysis ..................................................................................88
Figure 113: Example of Voltage Drop Analysis in Multiple Power Domain System ..............89
Figure 114: Schematic Representation of Power Rails with the Main ESD Protection Elements and Schematic Indication Missing Connection Between VSSB and VSSP Leading to the Fail of the Parasitic Bipolar .......................................................90
Figure 115: Example of Rule 6.4.1 .................................................................................................91
Figure 116: Package Level ESD Network Verification ........................................................................92
Figure 117: CDM Waveforms for Different Package Trace Time Delays ........................................92
Figure 118: Current Through ESD Element at the Far End of the Transmission Line on Different Chip Pad ...................................................................................................................93
Figure 119: Schematic for Spice Simulation of CDM Waveforms ..................................................93
Figure 120: The Presence of the Package RLC Parasitics Could Lead to the Increase of the ESD Stress Levels Vdev at the Internal Circuit Nodes .........................................................94
Figure 121: Chip-Level CDF Model Extraction And Simulation Process Flow ..............................94
Figure 122: A Macromodel for Each Subsystem in a Chip, and Equivalent Circuits Driven by Protection Circuits, Input Buffer, and Output Buffer ..................................................94
Figure 123: Example of Cross-Die ESD Path in a Multi-Die (System in a Package Design) ......95
Figure 124: CDM Peak Current Dependence on Package Size and Type ........................................96
Figure 125: Flip-Chip Package Cross-Section; Cdit is Between the Silicon Die/Package and Metal Lid that is Separated by Thermal Interface Material (TIM) ........................................97
Figure 126: Two Paths of CDM Peak Current ................................................................................97
Figure 127: A Package with a 3-Layer Substrate Placed on the Field Plate of the FICDM Tester .........................................................................................................................................98
Figure 128: Data Flow Diagram of the Automated Peak Current Estimation Tool ......................98