Peyman Ensaf

Senior ESD/RFI Engineer

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Professional Summary

Detail-oriented electrical engineer with expertise in advanced circuit design, system-level problem-solving, and complex data analysis. Skilled in developing innovative solutions for signal integrity, power delivery, and electromagnetic compatibility (EMC). Demonstrates strong technical proficiency in system optimization, root cause analysis, and hardware validation. Thrives in dynamic environments that challenge intellectual curiosity and demand technical rigor. Seeking an electrical engineering role to leverage deep domain knowledge and analytical capabilities in driving high-impact, cutting-edge design and testing initiatives.

Experience

Senior ESD/RFI Engineer

Jan 2016 – Present

Intel Corporation

Hillsboro, OR

- Droving technical alignment across industry stakeholders within the ESD Council, shaping unified standards for direct pin ESD at the system level (SL-DPE).
- Hands-on experience with Fault Analysis (FA) tools such as ELITE and TIVA for detecting and diagnosing silicon-level failures resulting from intentional direct pin discharge events to high-speed Tx/Rx signal lines.
- Developed and deployed direct pin discharge test systems for Intel test silicon, improving insight into real-world ESD behavior, enabling upcoming products.
- Led cross-functional debug of inconsistencies between TLP, direct signal pin discharge measurements, and simulation outputs, significantly improving model accuracy for internal validation and external partner use.
- Led the EMC working group to define and implement quality testing standards across Intel business units, ensuring consistent electromagnetic compatibility practices.
- Supported near-field analysis on Intel platforms to debug RFI (Radio Frequency Interference) failures detected during far-field testing, improving system robustness.
- Performed detailed near field debugging on multiple Intel platforms, identifying root causes and guiding mitigation strategies for RFI issues.
- Headed the RFI working group to establish rigorous testing requirements for Intel server products, driving enhanced product compliance and performance.
- Directed Intel System ESD Working Group, unifying system-level ESD efforts across multiple sites to establish standardized practices and streamline collaboration.
- Managed engineering team responsible for quantifying, deploying, and proliferating a system-based tester (SBTS) at Intel's Costa Rica site, driving improvements in system-level test optimization and throughput.
- Engineered and proliferated direct pin discharge test fixtures using ferrites to eliminate initial peak in ESD gun waveforms, enabling precise I/O signal stress testing.
- Developed and implemented system-level ESD and RFI product qualification testing protocols for all Intel products, establishing testing infrastructure and leading debugging efforts across multiple teams.
- Developed, deployed, and maintained Intel system-level and direct pin discharge ESD specifications, along with RFI standards, ensuring consistent compliance and product reliability.
- Performed analytical modeling of capacitive coupling on USB, HDMI, and other cable types using experimental measurements; applied a star-tree approach to enhance accuracy of cable discharge modeling.

- Completed multiple research projects published through ESDA and IEEE, focusing on characterization of component-level ESD test results using advanced techniques such as convolution/deconvolution, FFT/IFFT, and transmission line modeling to enhance CDM discharge analysis.
- Co-developed multiple advanced test methodologies, including system-level ESD, direct pin discharge, radio-frequency interference (RFI), and ESD gun verification techniques.
- Conducted internal training sessions on system-level ESD, component-level ESD, direct pin discharge, and RFI, enhancing the capabilities of internal customers, engineers, and technicians involved in test execution.
- Consolidated Intel Oregon ESD laboratories by integrating system-level ESD, component-level ESD, and RFI near-field testing infrastructure into a unified lab compliant with all safety and installation standards. Successfully led the lab through external ISO 9001 certification and facilitated the procurement of multiple component ESD testers for deployment across various Intel sites.
- Managed a multidisciplinary team to analyze and optimize inventory problems through Lean and Six Sigma, achieving significant operational improvements.

Component Engineer June 1998 – Dec 2016

Intel Corporation Hillsboro, OR

- Performed qualification testing in the thermo-mechanical domain using environmental stress methods such as Temperature Cycling, Highly Accelerated Stress Test (HAST), and Bake to evaluate reliability and material integrity.
- Developed methodology and measurement techniques leveraging Raman spectroscopy to monitor transistor-level temperature at arbitrary locations across the silicon die.
- Developed processor reliability models based on power state (frequency) transitions by analyzing time-in-state metrics using both real-world workloads and synthetic benchmarks.
- Developed methodology and measurement techniques to estimate failure probability as a function of voltage, temperature, and humidity, supporting product qualification readiness and reliability assessment.
- Characterized Defects Per Million (DPM) rates through C4 bump reliability assessments, utilizing power and temperature mapping across the silicon die to identify failure-prone regions.
- Developed a methodology and supporting tool to calculate per-C4 bump current and temperature, enabling accurate estimation of bump-level reliability across the silicon die.
- Developed a methodology for cross-platform performance measurement using on-silicon ring oscillators as process and speed indicators.
- Delivered Intel training classes covering power management, thermal management, and transistor and circuit design principles.
- Developed a methodology for per-part binning based on voltage, temperature, and frequency parameters to optimize bin capacity during high-volume manufacturing.
- Performed transistor sizing to optimize circuit performance for subsequent generations, alongside RTL code development for comprehensive circuit validation.
- Developed a Monte Carlo–based statistical tool employing numerical modeling to project power consumption, product DPM, and frequency bin splits by analyzing transistor leakage and dynamic currents in processor power profiles.

Education

PhD. Candidate June 1997

University of Colorado CO

M.S. in Electrical Engineering June 1995

University of Denver CO

B.S. in Physics June 1987

University of Minnesota MN

Skills

- Leadership
- R&D within ESD
- 3D E/M Modeling
- Lean/6-Sigma
- Debugging
- Project Management
- RFI
- Analytical assessments
- Technical documentation
- Statistical analysis
- Mathematical modeling
- Design of Experiment

Fun Facts

- Classical Pianist
- Jazz/Blues Tenor Saxophonist
- Casual Swimmer/hiker

Publications

- Timothy J. Maloney, Peyman Ensaf" A Circuit Model for the Charged Device Model Spark", 2025 In-Compliance Journal https://incompliancemag.com/a-circuit-model-for-the-charged-device-model-spark/
- Peyman Ensaf, Timothy J. Maloney" CDE Modeling Using Star-Tree Impedance Networks for USB2 Cable", 2023 In-Compliance Journal https://incompliancemag.com/article/cde-modeling-using-star-tree-impedance-networks-for-usb2-cable/
- Harald Gossner, Brett W Carn; David Johnsson; Yagnesh V Waghela; Yingern Ho; Peyman Ensaf; Keneth Thomas; Nathan D. Jack" System Efficient ESD Design (SEED)", Intel DTTC 2022
- Peyman Ensaf, Timothy J. Maloney "An Experimentally Verified Methodology for Calculating Coaxial Cable Loss Effects on CDM Waveforms", 2020 EOS/ESD Symposium Proceedings
- Ronald R. DeLyser, Peyman Ensaf" Quality Factor Evaluation of Complex Cavities", U.S Air Force, Phillips Research and Development Laboratory, Airforce office of scientific research
- Timothy J. Maloney, Peyman Ensaf, Marcos Hernandez" Intrinsic Inductance and Time-Dependent Resistance of the FI-CDM Spark", 2024 EOS/ESD Symposium
- Peyman Ensaf, Timothy J. Maloney" Electrostatics of the Resistor-blocked CDM Probe Pulse", 2022 EOS/ESD Symposium
- Peyman Ensaf, Timothy J. Maloney" Comprehensive Transadmittance of the CDM Measurement System, Including Current Transformation in the Test Fixture", 2021 EOS/ESD Symposium Proceedings
- Robert A. Brown, Peyman Ensaf, Todd Marshall, Melinda Piket-May, Branko Popovic, and Zoya Popovic" Printed Microwave Couplers with Thermal Isolation" IEEE Microwave and Guided Wave Letters