EOS/ESD Association, Inc
1st Annual India ESD Forum
November 15-16, 2021

Our first one of a kind forum in India bringing forth the realities of ESD requirements in light of the rapidly advancing semiconductor technologies. This forum is designed to be a two-day online event to bring together key semiconductor companies in India and esteemed academic institutions to learn and exchange information about designing ESD protections at the cell level and chip level along with understanding of ESD testing and system level ESD and EMI concerns. Renowned experts from various industry leading organizations are presenting Tutorials and Invited talks.

November 15, 2021

Tutorial#1 9AM -12 noon IST (UTC+05:30):Tech Needs for ESD Enablement : Impact of Technology Parameters (Leakage, GOX etc), Technology Scaling vs ESD Design.
Presenter: *Gianluca Boselli, Texas Instruments*

Tutorial#2 1PM - 4PM IST (UTC+05:30): Circuit design – Pcell, Clamps Design, Different ESD Protection Concept.
Presenter: *Nate Peachey, Qorvo Inc.*

Invited Talk#1 4:30PM - 5:30PM IST (UTC+05:30): Design Constraints of ESD Circuits for High-Speed Applications.
Presenter: *Charvaka Duvvury, iT2 Technologies*

November 16, 2021

Tutorial#3 9AM -12 noon IST (UTC+05:30): SoC ESD Design and Verification.
Presenter: *Hans Kunz, Texas Instruments*

Tutorial#4 1PM - 4PM IST (UTC+05:30): System Level ESD (Board Design) & EMC (Board Design /EMI Immune Circuit Design) Design. Presenter: *Harald Gossner, Intel*

Invited Talk#2 4:30PM - 5:30PM IST (UTC+05:30): ESD Testing: Different TLP, Different IEC Testing, Surge Test etc.
Presenters: *Kathy Muhonen, Qorvo, Inc.; Heinrich Wolf, Fraunhofer EMFT*

Technical Committee Members: Nitesh Trivedi (Intel), Harshit Dhakad (Intel), Vicky Batra (ST), Prof Nihar Ranjan Mahapatra (IIT, Gandhinagar), Prof Maryam Shojaei (IIT, Mumbai), Prof Benny Karunakar (IIT, Roorkee), Hari Shanker Gupta (SAC, ISRO), Jagadeesha Mallaiah (Cadence), Nitin Bansal (Synopsys), ArulDas Divakaran (Samsung), Charvaka Duvvurry, Souvick Mitra (GF)

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Meet the Instructors

Dr. Gianluca Boselli completed his master in EE at the University of Parma (Italy, 1996) and his PhD at the University of Twente (The Netherlands, 2001), where he worked on high current phenomena in CMOS technologies. In 2001, he joined Texas Instruments, Inc., Dallas, Texas, where he focused on ESD and latch-up development for advanced CMOS technologies, with emphasis on process and modeling aspects. In 2009 he was promoted corporate ESD Design and Development Manager to support the entire Texas Instruments portfolio. Since 2014, his responsibilities extended into compact modeling, where he is now compact modeling corporate manager, with responsibility to deliver compact models and simulation infrastructures to Texas Instruments design community. He authored several papers in the area of ESD and latch-up. He presented his work at major conferences, including EOS/ESD Symposium, IEDM, and IRPS. He has also presented many invited tutorials and papers at various conferences, including EOS/ESD Symposium, IRPS, IEDM, ESREF, IEW, and RCJ. Dr. Boselli has been the recipient of the best paper award on behalf of Microelectronics Reliability Journal in 2000. He received the best paper award at the EOS/ESD Symposium 2002. He also received the Outstanding Symposium award at the EOS/ESD Symposium in 2002, 2006, and 2010. Dr. Boselli served multiple times as sub-committee chair for technical program committees (TPC) of EOS/ESD Symposium, IEDM, IRPS, IEW, and ESREF. He served as moderator and panelist in many workshops in ESD and latch-up area. Dr. Boselli has served as TPC chair at the EOS/ESD Symposium 2006, vice-general chair at the EOS/ESD Symposium 2007, and general chair at the EOS/ESD Symposium 2008. He is currently a member of the board of directors of EOS/ESD Association, Inc., where he is the President Emeritus. He is the recipient to ESDA Outstanding Contribution Award. Dr. Boselli is an IEEE senior member and holds over thirty patents with several pending. Dr. Boselli serves in the editorial board of the IEEE Transactions on Device and Materials Reliability (T-DMR).

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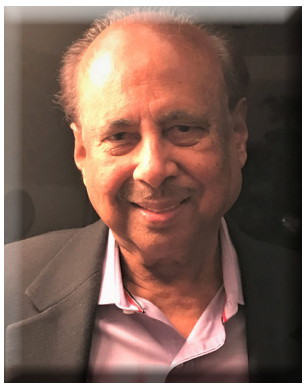

Charvaka Duvvury was a Texas Instruments fellow while he worked in the silicon technology development group. Charvaka is also a fellow of the IEEE. He is working as a technical consultant on ESD design methods and ESD qualification support. Charvaka received his PhD in engineering science from the University of Toledo. After working as a post-doctoral fellow in physics at the University of Alberta in Canada, he joined Texas Instruments, where he worked for more than 35 years. Charvaka has made numerous international presentations on ESD phenomena and protection design. He has published over 150 papers in technical journals and conferences and holds 75 patents. He has co-authored books on ESD design (ESD in Silicon Integrated Circuits, John Wiley & Sons, 2nd Edition 2002), hot carriers, and modeling of electrical overstress. He recently co-edited and authored System Level ESD Co-Design, John Wiley 2015. He is a recipient of the Outstanding Contributions award from the EOS/ESD Symposium (1990), Outstanding Mentor award twice from the SRC (1994 and 2012), and numerous best paper and best presentation awards from the EOS/ESD Symposium. He also received the IEEE Electron Devices Society Education Award (2013). He served twice as General Chair for the EOS/ESD Symposium during 1994 and in 2005. He was a contributing editor for the IEEE Transactions on Device and Materials Reliability (TDMR) from 2001 to 2011. Charvaka has been a member of the EOS/ESD Association board of directors since 1997, promoting university education and research in ESD. He is a co-founder and co-chair of the Industry Council on ESD Target Levels. Recently, Charvaka co-founded iT2 Technologies that features machine learning and AI-based software for ESD data analysis.

Harald Gossner is senior principal engineer at Intel. He received his degree in physics (Dipl. Phys.) from the Ludwig-Maximilians-University, Munich in 1990 and his Ph. D. in electrical engineering from the Universität der Bundeswehr, Munich in 1995. For 15 years he has worked on the development of ESD protection concepts with Siemens and Infineon Technologies. In 2010 he has joined Intel Mobile Communications overseeing the development of robust mobile systems. Harald has authored and co-authored more than 100 technical papers and two books in the field of ESD and device physics. He holds 50 patents on the same topic. He received the best paper award of EOSESD 2005 and 2012. Regularly he is lecturing tutorials at ESREF, IRPS and EOSESD symposium. He has served in technical program committees of IEDM, EOSESD Symposium and International ESD Workshop and is member of the board of directors of EOS/ESD Association, Inc. In 2006, he became co-founder and co-chair of the Industry Council on ESD Target Levels.

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Hans Kunz joined Texas Instruments as an ESD Specialist in 2003, after nine years at Dallas Semiconductor/Maxim. He was elected Senior Member of Technical Staff at Texas Instruments in 2012. His past responsibilities include the design, development and implementation of ESD protection circuits for analog CMOS and high-voltage BiCMOS technologies; he is currently focused on the development of ESD verification tools and methodologies. Hans has been active in the workshop process at both the EOS/ESD Symposium and IEW, serving as both panelist and moderator at various workshops and serving as the EOS/ESD Symposium Workshop Chair in 2010. He has been a member of the EOS/ESD Symposium Technical Program Committee every year since 2007. Hans has also been active in the educational tutorial process of the EOS/ESD Symposium, serving as a tutor since 2007. Hans is co-author of multiple publications related to ESD and received the Best Presentation Award for the 2006 EOS/ESD Symposium. He holds six patents in the area of ESD protection, with an additional eight pending. Hans received his B.S. degree in Physics from The University of the South and his B.S. in Electrical Engineering from The Georgia Institute of Technology.

Kathleen Muhonen is currently an ESD Engineer at Qorvo in Greensboro, NC. She is involved in ESD on-chip protection for mobile and millimeter wave applications. Kathleen is heavily involved with system level testing and helped standardize IEC testing of RF components and in ESD instrumentation for better ESD characterization of clamps and materials. Previously she was responsible for RF characterization and model support for SOI and GaAs technologies for power amplifiers, switches and antenna tuners. She has also done extensive work on developing state of the art harmonic characterization of semiconductors, breakdown models for SOI FETs and improving de-embedding techniques of large-scale switches. Kathleen's previous experience includes assistant professor at Penn State Erie, linearization design for base stations at Hewlett Packard and power amplifier design at Lockheed Martin and GE Aerospace. Kathleen is a member of the ESD Association and sits on all device testing standards committees, including serving as past TLP and HMM workgroup chairs. She has also served on the Board of Directors and is involved in the education committee for the ESDA. Her involvement in round robin testing for TLP, VF-TLP and IEC Component Testing has generated several papers presented at the EOS/ESD Symposium over the last decade. Kathleen received her BSEE degree from Michigan Technological University in 91, a MSEE from Syracuse University in 94 and a Ph.D.EE from Penn State University in 99.

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Nathaniel (Nate) Peachey received his Ph.D. in Physical Chemistry in 1994 from the University of Nebraska–Lincoln and then was awarded a Director's Funded Postdoctoral Fellowship at the Los Alamos National Laboratory (Los Alamos, NM) where he studied thin-film membranes for gas separation. In 1996, he joined Atmel Corporation in Colorado Springs as a thin-films process engineer. Over the next several years Dr. Peachey held various positions at Atmel including process engineer, technology development engineer, device engineer, and circuit design engineer. In 2003, he began focusing exclusively on ESD protection and I/O circuit design issues. In 2005 Dr. Peachey accepted the position of engineering manager for the newly formed ESD design group at RF Micro Devices. In this capacity, he was responsible for the development of ESD protection for all the technologies that RFMD designed in including both silicon and GaAs. Besides on-chip protection he led the development and improvement of the RF antenna ESD protection. In 2015 RFMD and Triquint Semiconductor merged to form Qorvo Inc. and Dr. Peachey continued his ESD and management responsibilities in the new company. Also, in 2015 Dr. Peachey added the responsibility of Corporate ESD Program Manager to his responsibilities. In this capacity, he is responsible to guide the ESD control program for Qorvo as well as oversee annual audits of assembly facilities. Dr. Peachey has authored and coauthored over 30 technical journal submissions. He has also submitted 14 patents that have either been granted or are pending. He was also asked to author a chapter on ESD and EOS failure mechanisms and reliability for the 2015 textbook "Electrostatic Discharge Protection: Advances and Applications" edited by Professor Juin J. Liou. Dr. Peachey is also a Senior Member of the IEEE. In 2009 Dr. Peachey was elected to the Board of Directors for the ESD Association. He has been involved in various activities within ESDA. From 2011 to 2017, he was the Manager for the Standards Business Unit for the ESD Association. He currently serves on the ESDA Executive Committee.

Heinrich Wolf received his diploma degree in electrical engineering from the Technical University of Munich (TUM) and his PhD from the Technical University of Berlin, Germany. He joined the chair of integrated circuits at TUM as a member of the scientific staff working on electrostatic discharge related issues. This involved modeling of ESD-protection elements, parameter extraction techniques, and test chip design. In 1999, he joined the Munich branch of the Fraunhofer Institute for Reliability and Microintegration (IZM) which became the Fraunhofer Institution for Microsystems and Solid State Technologies EMFT in 2010. He was involved in the investigation of ESD protections for CMOS and smart power technologies. Furthermore, he worked on the simulation and development of ESD protections and on the development of ESD test methods and tester characterization. He is also coordinating the ESD related activities at the EMFT including the development of ESD test systems and the design of protection structures for deep sub-micron technologies. Furthermore, he works in the field of RF simulation and characterization in the frequency range up to 110 GHz. Currently he is also representing the German ESD-Forum in the ESDA standards working groups.