2020

International Electrostatic Discharge Workshop

May 4 - 8, 2020

IEW

Setting the Global Standards for Static Control!
EOS/ESD Association, Inc. 7900 Turin Rd., Bldg. 3 Rome, NY 13440-2069, USA
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Experience IEW

Greetings from the 14th annual International ESD Workshop (IEW) Management Team! This event presents a unique opportunity for attendees to participate in in-depth discussions and learning on EOS and ESD topics in a highly interactive environment. Part of the interactive environment comes from the event location itself. This event will be held at the Tagungshotel Jesteburg, Germany.

Located just outside the center of the small town of Jesteburg the meeting hotel is surrounded by a wood. The quiet surrounding encourages stimulating discussions and immersive interaction. Focused discussion groups, held in the evenings, are a unique part of our interactive workshop. While each EOS/ESD topic discussion is facilitated by an expert on the subject, the main discussion will take place among the participants. The discussion groups will address topics of the focus issues and include ESD soft failures, challenges for advanced CMOS ESD protection, System level test for IOT and wearable devices, latch-up, on-chip health monitoring strategies and the possible impact of reducing CDM limits to 150V.

Scheduled poster sessions are the core of the technical program. These poster sessions begin with a brief summary of their contribution by each author. These teasers encourage the participants to visit each poster and its author in the subsequent interactive poster discussion session. To compliment the offering, attendees are also encouraged to bring open posters. This format provides an ideal forum for learning and the interchange of new ideas. Topics covered in the poster sessions include CDM effects and failures, Test cases, ESD verification with EDA tools, ESD devices for advanced CMOS technology, models for SEED simulations, on-chip ESD protection devices, latch-up and interconnect investigations.

The IEW also provides a forum for interactive special interest groups (SIGs), on selected subjects that may extend beyond the IEW time frame. Some SIGs have been successfully meeting for several years.

A number of stimulating state-of-the-art EOS/ESD seminars, as well as invited talks are scheduled. Come and listen to presentations, and later meet with the presenters, discussing ESD protection for brain implantable electronics, FD-SOI technology, fast transients of CDM, side channel attacks on chips with security functions, Challenges for System Technology Co-Optimization approach, EMC design and soft failures, electrical overstress and new IEC testing results.

An afternoon is allocated for recreational activities with fellow attendees, allowing Jesteberg and its surroundings to be enjoyed, perhaps taking advantage of its proximity to the city of Hamburg. This is a great way to get to know your EOS/ ESD colleagues better.

Come and meet experts, share your views, ask questions, and extend your network with EOS/ ESD experts from industry and academia. Above all, learn how to efficiently deal with today's EOS/ESD challenges and prepare for tomorrow in an informal and interactive atmosphere. Register for this event early. This will help us in the final planning and preparation for a highly successful event. We sincerely hope that you will join us in Jesteburg, Germany for the 2020 IEW.

Tutorial Monday 2:30 - 4:30 PM

Advanced TLP Applications
Instructor: Heinrich Wolf, Fraunhofer EMFT

The tutorial covers accuracy aspects of transmission line testing and explains how to do characterization and parameter extraction for compact modelling including switching behavior and electro-thermal aspects. Furthermore, it discusses SOA measurements and the application of CC-TLP as a CDM like stress method.

Heinrich Wolf received his diploma degree in electrical engineering from the Technical University of Munich (TUM) and his PhD from the Technical University of Berlin, Germany. He joined the chair of integrated circuits at TUM as a member of the scientific staff working on electrostatic discharge related issues. This involved modeling of ESD-protection elements, parameter extraction techniques, and test chip design. In 1999, he joined the Munich branch of the Fraunhofer Institute for Reliability and Microintegration (IZM) which became the Fraunhofer Institution for Microsystems and Solid State Technologies EMFT in 2010. He was involved in the investigation of ESD protections for CMOS and smart power technologies. Furthermore, he worked on the simulation and development of ESD protections and on the development of ESD test methods and tester characterization. He is also coordinating the ESD related activities at the EMFT including the development of ESD test systems and the design of protection structures for deep submicron technologies. Furthermore, he works in the field of RF simulation and characterization in the frequency range up to 110 GHz. Currently he also represents the german ESD-Forum in the standards working groups.

Monday Entertainment 7:30 PM

Keynote

ESD Protection for Medical Implants

Wolfgang Krautschneider, Hamburg University of Technology

Scaling-down of CMOS circuits is accompanied by a huge performance increase of integrated circuits that opens up much potential of electronics for medical implants. There are already some electronic implants in use, e.g., pace makers, cochlear implants and implants for deep brain stimulation. Implants for other medical applications are in an early state or under development.

Biological signal sources show in most cases a very high impedance and provide signals with a very low amplitude. This requires amplifiers with very high input impedance provided by MOS transistors. For handling the electronic circuits during assembly, all the pads connected to gates of MOS transistors have to be protected by ESD devices that may degrade the input resistance resulting in worse signal to noise ratios. An appropriate trade-off has to be found that will be illustrated by demonstrators for medical implants.

Another challenge for medical implants are the very high magnetic fields of MRI which may generate high voltages that have to be handled by protection structures.

One out of four persons in western countries gets the diagnosis cancer with metastases. They are treated by systemic therapy (chemotherapy etc.) combined with radiotherapy applying comparably high radiation doses. When these patients carry medical implants, the radiation can degrade the characteristics of ESD protection devices, so that design measures have to be taken to adjust their radiation robustness accordingly.

Wolfgang H. Krautschneider (M'85) received the M.Sc., Ph.D., and Habilitation degrees from the Berlin University of Technology, Berlin, Germany.,He was with Central Research Laboratories, IBM, Yorktown Heights, NY, USA, the Siemens Research Center, Munich, Germany, and the DRAM Project of IBM and Siemens, Essex Junction, VT, USA. He is currently the Head of the Institute of Nanoelectronics at the Hamburg University of Technology, Hamburg, Germany.

Invited Talks

Invited Speaker Co-Chairs:
Shih-Hung Chen, imec
Yiqun Cao, Infineon Technologies AG

Invited talks always give good opportunities to broaden workshop attendees' exposure to expertise in different focused areas of interests. This year, three invited talks are included with wide-range aspects from process technology, chip security, to system qualification. The talk from Dr. Philippe Galy, STMicroelectronics, is one of the focus topics of this year. It is dedicated on ESD/LU challenges for ultra-thin body and box (UTBB) fully depleted SOI (FD SOI) CMOS technology for 2D and 3D innovative solutions. Dr. Galy will give an introduction of this UTBB FD SOI technology and will also discuss innovative ESD solutions. The talk from Alexander Schlösser, NXP, will focus on side channel attacks for high security automotive chips. In this talk, Alexander will look at how hardware security analysis uses soft failures and will explore the differences and similarities to ESD-related failures. The talk from Dimitri Linten, imec, will focus on the scaling technology with system technology co-optimization (STCO) approach toward node N5 and beyond. Dr. Linten will give an introduction of the novel STCO approach and will discuss the ESD reliability challenges in this technology.

Invited Talk 1

UTBB FD-SOI and ESD/Latch-up: Challenges and Solutions

Philippe Galy, STMicroelectronics

This talk is dedicated to ESD/LU challenges for Fully Depleted SOI (FD-SOI) Ultra Thin Body and Box (UTBB) CMOS technology nodes for 2D and 3D innovative solutions. After an introduction on the UTBB FD_SOI technology provided by STmicrolectronics, especially in 28nm High k metal gate, the ESD protection challenges in this technology will be discussed along with solutions. Preliminary silicon results with 2D/3D innovative solutions are introduced according to performance and integration. Moreover, radiation effects are also addressed.

Philippe Galy born 1965, received the Ph.D. from University of Bordeaux and H.D.R from LAAS CNRS University of Toulouse. He is a fellow, technical director at STmicrolectronics Research and Development France. He has proposed a full CDM protection and several new ESD compact devices for mature & advanced CMOS technologies. He supports several teams for research focused on new innovative solutions: Memory + silicon Qubit and cryo-design, Neuromorphic, 3D ultimate integration. He has authored or coauthored several publications (+100), books (3), and patents (+100). He serves in TPC and is a reviewer for many symposiums and journals. He is also involved in National (3) and European projects (4). Also he joins the QuEng CDP team from Grenoble and also adjunct professor at " Université de Sherbrooke (UdS)".

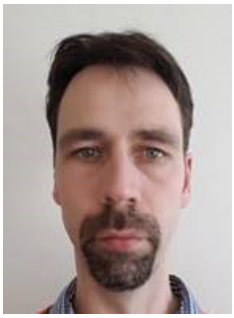
Invited Talk 2

Reliability Challenges in Scaling Era with System Technology Co-Optimization (STCO) Approach

Dimitri Linten, imec

From the 10 nm technology generation onward, traditional scaling has been complemented by design-technology co-optimization (DTCO), combining expertise from technology as well as from design. But, as the technology moving forward, the benefits of DTCO in system-on-chip (SoC) applications are expected a certain saturation. For 3 nm and beyond technology nodes, the focus will shift from scaling at logic cell level towards scaling at system level. Hence, DTCO is evolving into an system technology co-optimization (STCO)-oriented approach. More and more (sub-)system functions will be integrated in one chip with a special 3D vertically stacked or 2.5D interposer architecture. However, a chip-level or even a system-level electrical reliability becomes necessary to evaluate at the early stage of the technology/circuit/system development period.

In this talk, we will look at the technology features of the STCO approach, including different 3D integration technologies applied in different levels of interconnect hierarchy. In addition, the emerging reliability challenges will be also discussed from different aspects in the STCO framework. .



Dimitri Linten received PhD degrees in electrical engineering from the Vrije Universiteit Brussel (VUB), Brussels, Belgium in 2006. Since 2015, he is the R&D manager of the Device Reliability and Electrical characterization group at imec. He is a senior member of the IEEE (SM13). His main research interests are ESD reliability, Memory and logic device reliability physics, radiation, biosensors and security. He has served as a technical program committee member of several international scientific conferences, among which the International Reliability Physics Symposium (IRPS), the EOS/ESD Symposium, the International ESD Workshop (IEW) and International Electron Devices Meeting (IEDM).

Invited Talk 3

Soft Fails as a Tool in Hardware Security Analysis

Alexander Schlösser, NXP Semiconductors

While soft fails are to be avoided from an ESD point of view they can be quite useful in another domain. Hardware Security Analysis is a specific field in the wide world of hacking and penetration testing. It focuses largely on so-called implementation attacks, targeting the unintended imperfections and compromises in the physical realization of a digital design. The methods for these attacks are often derived from failure analysis and include the use of lasers, micro- and nano-probes as well as small-scale antennas and field generators.

A specific group of methods are Fault Injection Attacks. These are active but non-invasive efforts to intentionally cause soft fails, with the aim to compromise the secure handling of to-be-protected data. This talk will introduce the systems and methods used in fault injection attacks and the physical effects and interactions that are exploited. It will show how hardware security analysis uses these fails and discuss differences and similarities to ESD-related fails.

Alexander Schlösser is a Senior Security Analyst with NXP Semiconductors. As a member of NXP's internal hacking team he conducts hardware security analyses of Smart Cards and Secure Elements as well as automotive and application processors. Alexander has a background in photonics and received a PhD in physics from TU Berlin before he joined NXP in 2014. Since then he develops systems and methods to identify and root-cause vulnerabilities and weaknesses in digital designs with a security focus.

Seminars

Seminar Co-Chairs:
Shih-Hung Chen, imec
Yiqun Cao, Infineon Technologies AG

Four recognized experts from university, research institute, and industry will give seminar talks on some of the highly interesting topics at this year's IEW. These seminar talks are covered with the main ESD challenges in system-level, component-level, and even manufacturing perspectives. The seminar from Dr. Wolfgang Stadler, Intel, will focus on non-standard overstress in manufacturing phase and will show the (mis)correlation between IC ESD qualification waveforms and real world risks in handling ICs, boards, and systems. The seminar from Professor David Pommerenke, ESDEMC, will focus on system-level ESD testing and will discuss the reasons for large uncertainty of the test results even when carefully following the procedures in IEC 61000-4-2, as well as give suggestions to the test implementation. The seminar from Professor Franco Fiori, Politecnico di Torino, will focus on circuit-level EMC/EMI design and will discuss recent progresses on the EMI immune designs of MEMS readout circuits. Finally, the seminar from Johannes Weber, Fraunhofer EMFT, will focus on fast transient of CDM ESD event and will cover wide-range perspectives of the fast rise time (or fast slew rate) from the fundamental theory to the testing methodologies.

Seminar 1

Achieving Meaningful and Repeatable Results in ESD System Level Testing

David Pommerenke, Technical University of Graz.

The vast majority of system level ESD testing follows the specifications defined in IEC 61000-4-2. Unfortunately, even when carefully following the procedures in IEC 61000-4-2 there is a high level of uncertainty in the test results, and successful passing of the test requirements is often not a good prediction of ESD robustness in the field. The talk, which is based on a white paper by the Industry Council on ESD Target Levels explains deficiencies of the standard and problems within the generally applied test procedures. Based on this analysis the talk suggests improvements to both the standard, and the test implementation.
This includes
- better ESD gun specifications
- Full wave and SPICE models for ESD generators
- Simulation of ESD robustness following the SEED concept (System Efficient ESD Design)
- Improved documentation, such as measuring the ESD current during testing
- Improved test produced e.g., number of discharges, methods of stabilizing the arc in air discharge etc.
- Robotic ESD testing

The goal of the talk is to explain the reasons for the large test result uncertainty, to give suggestions to the standard committee for improvements and to enable engineers to implement the test in such a way that results are meaningful, repeat well and give indications for the root cause of a failure.

Dr. David Pommerenke received his diploma and PhD from the Technical University Berlin, Germany. His research interests are system level ESD, electronics, numerical simulations, EMC measurement methods and instrumentation. He worked at Hewlett Packard for 5 years before joining the electromagnetic compatibility laboratory at the Missouri University of S&T in 2001. Dr. Pommerenke became the CTO of ESDEMC in July 2019 before joining the ESD/EMC group at the Technical University of Graz in Austria in January 2020. His new focus is on ESD, EMC, harmonics, and PIM. He has published more than 200 papers and is inventor on 13 patents. His main research interests are measurement/instrumentation ESD, electronic design and EMC. He is IEEE fellow and associated editor for the IEEE Transactions on EMC.

Seminar 2

Correlation of Qualification ESD Robustness and Handling Threats

Wolfgang Stadler, Intel Deutschland GmbH

Today, almost all integrated circuits (ICs) are qualified with respect to Human Body Model (HBM) and Charged Device Model (CDM). Current international standards on ESD Control Programs require a minimum ESD robustness of 100 V according to HBM and 200 V of CDM for ICs to ensure safe handling. However, there is no clear correlation between qualification waveforms and waveforms of reel ESD events even on IC level, therefore, the qualification might not necessarily cover all problems.
The situation is even worse if ESD events on system level are considered. Such events mainly occur during board and system assembly or during testing, like Charged Board Events, Cable Discharge Events, or transient latch-up. Today, there are no widely accepted ESD qualification standards on most of these ESD system level events, this is one reason why the ESD control standards refer to IC level robustness only.
In this presentation, we will assess the (mis)correlation between IC ESD qualification waveforms and real world risks in handling ICs, boards, and systems. We will also discuss which ESD system level characterization methods could help to improve the ESD process assessment methodologies of boards or system handling processes.

Wolfgang Stadler received his diploma degree in physics in 1991 and in 1995 the PhD degree from the Physics Department of the Technical University Munich. 1995 he joined the semiconductor division of Siemens, which became Infineon Technologies in 1999. His focus was on development of ESD-protection concepts in CMOS technologies and on innovative ESD topics. In this role he was coordinator of several European and German ESD funding projects. Since 2003, he was also been responsible for the measurement characterization of I/O cells and PHYs. In 2011, he joined Intel Mobile Communications which is now Intel Deutschland GmbH. Within the corporate quality network, he is currently responsible for the ESD control program of Intel and for ESD risk assessment. Furthermore, he supports ESD/latch-up testing and qualification of products. Wolfgang holds several patents in ESD-related topics. He is author or co-author of more than 120 technical papers and has co-authored a book on ESD simulation. He has received several best paper awards and teaches courses on ESD device testing, ESD qualification, and ESD control measures (for example, TR53 ESD Technician Certification).

Seminar 3

Recent Advances on the Design of MEMS Readout Circuits Immune to EMI

Franco Fiori, Politecnico di Torino

Among the circuit topologies available in the open literature for the design of MEMS readout circuits, those based on the current feedback differential difference amplifier (DDA) are usually preferred because they feature a wider differential input range (DMIR), rail-to-rail common mode input range (CMIR), high power supply rejection (PSR) as well as high noise figure. These are valuable features for low voltage applications. In addition, such a topology lends itself well to implement auxiliary circuits such as those needed for input biasing or DC offset cancellation or AC calibration.

Franco Fiori(M'02) received the Laurea and Ph.D. degrees in electronic engineering from the Polytechnic University of Turin, Turin, Italy, in 1993 and 1997,respectively. From 1997 to 1998, he was an R&D Leader ofST-Microelectronics, Milan, Italy. In 1999, he joined the Electronics and Telecommunication Department, Polytechnic University of Turin, where he is currently an Associate Professor of Electronics. From 2006 to 2010, he was the Scientific Leader of a joint ST-Microelectronics-Politecnico di Torino Research Laboratory aimed to investigate chip-level EMC issues. He has authored and coauthored more than 170 papers published in international journals and conference proceedings. His research interests include analog circuit design, macro-modeling of active nonlinear circuits, smart power devices, and electromagnetic compatibility.

Seminar 4

Stress Current Rise Time Evaluation in the Single-Digit Picosecond-Domain

Johannes Weber, Fraunhofer EMFT

This seminar will cover theory including the definition of rise time/slew rate, relation to bandwidth oft the test system, and voltage overshoot of typical ESD protection schemes; as well as dependency of ESD robustness (peak current failure thresholds) on rise time (slew rate). Examples of discharges with ultra-fast rise times in the manufacturing line will be given. The seminar will also include discussion on current rise time evaluation of CDM testing and alternative contact-based test method CC-TLP as a method to repeatably control rise time of stress pulses. During the seminar, the speaker will challenge the limits of today's test methods and methodologies in the single-digit picosecond domain and discuss critical parameters that may influence the slew rate (rise time) sensitivity of high-speed devices (high-speed design, DC-blocking capacitor etc.).

Johannes Weber received his Master's degree in physics from the Technical University Munich (TUM) in 2015. He wrote his Master's thesis in the research area of Nuclear, Particle and Astrophysics at the Max Planck Institute for Extraterrestrial Physics (MPE). Afterward, he joined the Team of Analysis & Test at the Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT in Munich, Germany as a research associate. He works in the field of Electrostatic Discharges (ESD) and focuses on the development of ESD test methods and ultra-fast ESD events in the picosecond domain. His research mainly deals with the influences of critical stress parameters like the rise time or the energy content of the stress pulse on the failure level of advanced semiconductor technologies. Supported by the ERC Grant 2016 of the ESD-Association, he finished his PhD thesis with the title "Pulsed High Current Characterization of Highly Integrated Circuits and Systems" at the Bundes-wehr University of Munich in 2019.

Discussion Groups

Discussion Groups Chair:
Fabrice Caignet, LAAS/CNRS

The discussion groups are an integral part of the workshop. There will be six discussion groups offered, with three parallel sessions on Tuesday evening and three parallel sessions on Wednesday evening. The topics include ESD soft failures; ESD challenges for advanced CMOS (FD-SOI, beyond FINFETS); discussions on health monitoring, the appropriateness of system level testing for IoT devices/wearables; latch-up; and testing devices for CDM below 150 volts. Each discussion group has a moderator with extensive expertise on the topic to help guide and inspire the discussion. The success of these sessions depends on your active participation. We encourage you to bring along data, ideas, and other items of interest to share.

Session A
Parallel Groups–Tuesday 7:00–8:30 PM

DG A.1

ESD Challenges for Advanced CMOS (FD-SOI, Beyond FINFETS)

Co-Moderators: Shih Hung Chen, imec; Philippe Galy, STMicroelectronics

While Bulk FinFET and Fully-Depleted (FD) SOI technologies have become the mainstream in the advanced CMOS IC industry, what are the next technology options or next device architectures after FinFET and FD SOI? Several promising candidates have been proposed; however, only very few prior works discussed ESD reliability in these promising future technologies. In addition, the challenges might not only from technology options but also from more realistic aspects, such as design verification and product qualification. This discussion group aims to look at the ESD challenges in advanced CMOS technologies with varied perspectives. With your ideas and sharing experience, this discussion group will be able to bring some clarity to those emerging ESD challenges.

DG A.2

System Level Test: is it Appropriate for IOT Devices/Wearables?

Co-Moderators: Adrijan Barić, University of Zagreb Faculty of Electrical Engineering and Computing; Harald Gossner, Intel Deutschland GmbH

System level testing using IEC 61000-4-2 is like an elephant in a glass shop; it seems to be widely applicable and it produces sound results. However, the question is, is it really useful and relevant for real world events or is there any better approach? Also, what are the most appropriate test levels for tiny IoT devices. Are the size of the IoT device and the technology node critical for the energy that can be dissipated on the device? What are the ultimate sustainable testing levels for the down scaled technology nodes that will inevitably penetrate into the IoT market? Finally, when we do system level testing, do we look only for the functionality of the device or we also have to worry about safety of the system. Is it possible to disturb the operation in such a way that the data sent from IoT device can generate a twisted image of the reality?

DG A.3

Is Latch-up Testing Still Relevant?

Moderator: Guido Quax, NXP Semiconductors

The category of low voltage IC products has experienced an ever decreasing operating voltage, such that a setup according to the latchup standard (JEDEC78E) does not lead to any current injection stress. On the other hand, the number of products with a severe system level stress requirement (like IEC61000-4-2 or IEC61000-4-5) is increasing. The risk for 'soft failures' (latchup) would, in this case, not be covered by passing the JEDEC78E test.

This leads to a question: does the standard need to get better 'aligned' with the modern product portfolio? And if so, how should that be done? One can think of product categories, each with their own stress. How should the reference stress for a product category be determined? Next to these possible improvements to the standard, we would like to reflect with you on the cause of current injection stresses in 'the real world'. In which situations do you think the +/- 100 mA stress could still occur, and are there actual field returns related to situations beyond this current stress level? How can the standard capture these situations? With this discussion we aim to get a better insight in the limitations of the current JEDEC78E standard.

Session B
Parallel Groups- Wednesday 7:00-8:30 PM

DG B.1
ESD Induced Soft Failures
Moderator: David Pommerenke, ESDEMC

This discussion group will try to answer the root cause of soft-failures, methods for modeling, and countermeasures. The root-cause includes, the discharge, the system level coupling path, and the internal reasons of the IC which lead to a soft-failure. Modeling of soft-failures can be successful using circuit information if the region inside the IC is well defined. However, in most cases behavioral models will be needed. Here behavioral models for USB 3.x will be presented and compared to measurements. A variety of countermeasures exist, obviously in software, but it is also possible to use TVS diodes such that they not only prevent damage, but reduce soft failures strongly. This will be explained based on a USB 3.x example to start an open discussion on all aspects of soft failures.

DG B.2
Health Monitoring: Can we use Transient Event Detection of EOS/ESD to Build More Resilient Systems?
Moderatos: Franz Dietz, Henning Lohmeyer, Robert Bosch GmbH; Patrice Besse, NXP Semiconductors

Over the last years there has been significant attention within reliability engineering to the so called third generation of reliability. Such resilient systems are designed to be aware of their health status by recognition of critical stress-strength combinations. This enables the system to react to changed situations or even to compensate errors prior to failure. On a hardware level it is proposed to introduce detectors for aging, mission profile logging and impeding failure of SoC. Additionally, detectors for events exceeding normal operation region were proposed which arguable could include EOS/ESD. Specifically for ESD threads, transient event detectors have been discussed that monitor exposure of the systems to ESD-stress during assembly and field usage. Furthermore such detectors have been proposed to support analysis of ESD soft failures and enable containment of such events on system-level. By sorting through the different approaches and targets of implementing transient event detectors, the discussion group aims to identify the potential benefits and limits of such an approach in the context of resilient systems for different applications. What can we learn from detecting and even measuring strength of ESD/EOS events in assembly and field and how do we use such information for more resilient and safe systems?

DG B.3
Testing Devices for CDM Below 150 Volts
Moderator: Marko Simicic, imec

The CDM device testing levels are dropping below 150 volts. One of the reasons for that is the technology advancement. However, the zap-to-zap variability of the standard Field-Induced CDM (FI-CDM) tester used today drops significantly for low voltages. Alternative CDM testers such as the capacitively-coupled TLP or the low-impedance contact CDM (LICCDM) do not have issues with variability. However, their relay-based testing mechanism is significantly different to the current standard. In this discussion group, we will discuss questions as:

What are the reasons for lowering the CDM testing level?

Is the pulse rise time an issue for LICCDM/CC-TLP?

What are the concerns with testing CDM on non-packaged dies and wafers?

Should we be reporting the CDM currents instead of the voltages?

Technical Sessions

Technical Session Chair: Heinrich Wolf, Fraunhofer EFMT

This year's IEW technical program consists of three sessions, where peer-reviewed poster presentations are discussed together with the authors and interested colleagues. The authors will introduce their work in a short podium "teaser" presentation before the extended interactive discussion with the workshop participants at the poster sessions. This format allows an in-depth exchange of ideas among a diverse audience in a very informal setting. A wide variety of ESD subjects will be covered, including ESD simulation/verification of full chips and single elements, system related and general measurements aspects and device physics covering the behavior of single elements, and also latch-up.

Technical Session A: Simulation Related Topics

A.1 CDM Failures at Internal Nodes— Challenges for Future CDM Simulation and Understanding of Test Results

James Karp, Xilinx, Inc.

This poster will share case studies of CDM failures observed at internal nodes 100 microns away from I/O pads. The author will propose a device physics model that explains CDM failures that cannot be characterized with VFTLP and simulated with available current density tools.

A.2 X-FAB ESD Design Checker an Automated Tool for Full Chip ESD Simulation

Vadim Kuznetsov, X-FAB Dresden GmbH & Co. KG; Lars Bergmann, X-FAB Global Services GmbH

X-FAB ESD Design Checker (XESDC) is the tool for full chip ESD analysis. It performs a virtual TLP test and finds ESD weaknesses of IC design using the CDL or SPICE extracted netlist and technology-specific ESD model library. XESDC works independently from EDA platforms using the built-in simulation core.

A.3 ESD Charaterization and TCAD Simulation of Reversed ggNMOS in Advanced Bulk FinFET Technology

W-C. Chen, S-H. Chen, G. Hellings, Y-K. Siew, J. Chen, G. Groeseneken, D. Linten, imec

In this work, the ESD performance of reversed GG-NMOS in the advanced bulk FinFET are investigated. The impact of the layout parameters, such as gate length (Lg) and the distance of the gate and the drain contact (Lgd) are demonstrated by the TLP measurement and studied by the 3D TCAD simulation.

A.4 Chip-Level ESD Verification Using Graph-Theory Based Approach

Vlatko Galić, Adrijan Barić, University of Zagreb; Aarnout Wieers, Renaud Gillon, ON Semiconductor

A new Electrostatic Discharge (ESD) verification flow is proposed. The presented methodology uses piecewise linear models based on transmission line pulsing (TLP) measurements to ascertain the level of ESD robustness of integrated circuits (IC) and to detect ESD current paths. This flow is based on graph-theory Floyd-Warshall algorithm.

A.5 Full-Chip CDM Analysis: Is Static Simulation Enough?

Jordan Davis, Chanhee Jeon, Sung-Jun Song, Samsung Electronics; Yuri Feinburg, Simon Young, Silicon Frontline

To improve understanding and verification of ICs before manufacturing, a static approach to CDM verification and analysis is explored. In the absence of full-chip transient circuit simulation, considered computationally prohibitive, enhancements to the static approach have been made. These enhancements are able to find potential failures regardless of technology or design.

Technical Sessions continued

Technical Session B: System-Level and General Testing Aspects

B.1 Display Driver IC`s System Level ESD Failure Case Study with Component Level ESD Test & Analysis

Sung-Joon Song, Young-Min Kim, Chang-Su Kim, Chan-Hee Jeon, Samsung Electronics Co., Ltd

A display driver IC's EOS/ESD failure case observed in TV assembly line. The root cause of IC failures is identified to be the gate oxide rupture. In this case study, the effectiveness of the resistance analysis tool is demonstrated through the component level ESD test to identify the IC failure.

B.2 Generalization of Modelling Concept for Common Mode Choke (CMC)

Sergej Bub, Nexperia Germany GmbH

In this poster, a generalized modeling concept for Common Mode Choke (CMC) is presented. The S-Parameters based small-signal model of CMC is extended with dynamic and saturation working regions evaluated using the Transmission Line Pulse (TLP) test method. The developed CMC model is verified on the different types of CMC.

B.3 Using Fast Transient Characterization (FTC) for EOS Risk Mitigation

Dietmar Walther, Raj Sankaralingam, Texas Instruments

The introduced method applies fast transient pulses (residual IEC 61000-4-2 pulses) with high energy to a powered device.

Besides soft failures also electrical induced physical damages (EIPD) are observed which were undetected during HBM/CDM.

Once fails are identified, simulation is used identifying circuit weaknesses to comprehend powered ESD fail modes.

B.4 A Discussion on ESD Data in IC Datasheets

Bart Huitsing, Theo Smedes, NXP Semiconductors

Despite the publication of a Standard Practice and consolidated Joint ESD Standards, it remains challenging to specify a correct and exhaustive ESD robustness of application specific components. We will discuss suggestions how to deal with e.g. IC's with mixed pin specific robustness requirements or IC's with non-standard pin-to-pin discharge requirements.

B.5 Influence of Parasitic Impedances on LICCDM Testers

Marko Simicic, Wei-Min Wu, Shih-Hung Chen, Dimitri Linten, imec; Shinichi Tamura, Yohei Shimada, Masanori Sawada, Hanwa Electronic Ind. Co., Ltd.

It is expected that CDM testing on wafer level and with pre-charge voltages below 150 V will soon become necessary for new technologies. Low-Impedance Contact CDM (LICCDM) is one of the candidates that could satisfy these requirements. In this work we study the parasitic impedances that affect the LICCDM tester.

B.6 De-Embedding of VF-TLP/CC-TLP Systems

Johannes Weber, Ellen Jirutková, Heinrich Wolf, Horst Gieser, Fraunhofer EMFT

This poster presents a De-/Embedding technique for TDR-based test methods like VF-TLP or CC-TLP. It replaces the manual determination of the time shift parameter between the incident and reflected pulse by fully reconstructing the signals at the DUT considering dispersion effects. Instead of S-parameters of the test fixture which should be de-embedded, its calibration requires only three pulses in time domain.

Technical Sessions continued

Technical Session C: Device Physics and Design

C.1 Evaluating Latchup (LU) Risk in Advanced CMOS Technologies

Guido Groeseneken, Kateryna Serbulova, KULeuven ESAT, imec; Shih-Hung Chen, Geert Hellings; imec

In advanced CMOS technologies, LU risk becomes one of the major reliability concerns because of the shrinking layout dimensions. LU originates from parasitic BJTs forming SCR path. The beta gain of these parasitic BJTs is essential characteristic for LU prevention that is evaluated for different layout configurations in this work.

C.2 Single Event Latchup or Multi Event Latchup - How Far Can You Push it?

Geert Hellings, Brecht Truijen, Marko Simicic, Shih-Hung Chen, imec

During SEL robustness tests, a chip is exposed to a high flux of radiation. We investigated the probability of Multi Event Latchup (MEL) during such accelerated tests. Based on TCAD and theoretical derivations, we find that MEL can occur, although it highly depends on the test specifics (# of DUT, test flux, layout, etc.).

C.3 Triggering of Multi-Finger and Multi-Segment SCRs Near the Holding Voltage Studied by Emission Microscopy Under DC Conditions

Hasan Karaca, Dionyz Pogany, TU Wien; Clement Fleury, CTR Carinthian Tech Research AG; Steffen Holland, Hans-Martin Ritter, Guido Notermans, Nexperia

Emission microscopy under DC current controlled mode has been used to study current flow distribution in multi-finger and multi-segment SCRs. The elements trigger at nearly the same current density indicating the substrate-coupled triggering mechanism found previously under TLP regime. On-resistance and holding current aspects are also discussed.

C.4 Influencing SCR Holding Current by Segmentation Topology

Vasantha Kumar, Steffen Holland, Hans-Martin Ritter, Nexperia

A segmented layout topology on a novel SCR is used to obtain a higher holding current (Ihold). The SCR Ihold has been increased by reducing the emitter area of the PNP, which reduces the injection efficiency of the PNP. The increased ability to collect free carries results in higher Ihold.

C.5 Interconnect Capacitance Investigation and Optimization Under I/O Pad for ESD Protection of RF/High-Speed Circuits in Micro-& Nano-scale CMOS Technology

Wei-Min Wu, imec; NCTU; KU Leuven, Shih-Hung Chen, Dimitri Linten, imec; Guido Groeseneken,imec-Leuven; KU Leuven

Recently, new distributed network to put ESD devices under I/O pad was proposed. However, parasitic capacitance gets more critical to RF degradation. In this work, investigation of capacitance, technique of BEOL capacitance reduction, S-parameter and TLP measurement, and optimization between RF and ESD are compared, fabricated, and proposed.

C.6 Effects of Current Density and Geometry on Parasitic NPN Transistors in CMOS

Guido Quax, NXP Semiconductors

This work investigates the behavior of parasitic npn bipolars in an advanced CMOS and a submicron power technology as a function of current injection level and multiple geometric parameters. We intend to create an integral empirical model, which can be easily applied during the design practice.

Schedule

start	end	Monday
12:00	14:30	Optional Lunch
13:00	16:00	Registration
14:00	14:30	Free Time
14:30	16:30	Tutorial: Advanced TLP Applications Heinrich Wolf, Fraunhofer EMFT
16:30	17:00	Break
17:00	18:00	**Seminar 1: Achieving Meaningful and Repeatable Results in ESD System Level Testing** David Pommerenke, ESDEMC
18:00	19:30	Dinner
19:30	20:30	Welcome entertainment
20:30	21:30	Networking/ Social Gathering

start	end	Tuesday
7:30	9:00	Breakfast
9:00	9:30	Welcome (open poster question)
9:30	10:30	Keynote: ESD Protection for Medical Implants Wolfgang Krautschneider, Hamburg University of Technology
10:30	11:00	Break
11:00	12:00	**Invited talk 1: UTBB FD-SOI and ESD/Latch-up: Challenges and Solutions** Philippe Galy, STMicroelectronics
12:00	13:00	Lunch
13:00	14:00	**Seminar 2: Correlation of Qualification ESD Robustness and Handling Threats** Wolfgang Stadler, Intel Deutschland GmbH
14:00	15:00	Technical session A: Simulation Related Topics
15:00	16:30	Poster discussion session A
16:30	17:00	Break
17:00	18:00	**Invited talk 2: Reliability Challenges in Scaling Era with System Technology Co-Optimization (STCO) Approach** Dimitri Linten, imec
18:00	19:00	Dinner
19:00	20:30	Discussion Group Session A A.1 ESD Challenges for Advanced CMOS (FD-SOI, Beyond FINFETS) Co-Moderators: Shih Hung Chen, imec; Philippe Galy, STMicroelectronics A.2 System Level Test: is it Appropriate for IOT Devices/ Wearables? Co-Moderators: Adrijan Barić, University of Zagreb Faculty of Electrical Engineering and Computing; Harald Gossner, Intel Deutschland GmbH A.3 Is Latch-up Testing Still Relevant? Moderator: Guido Quax, NXP Semiconductors
20:30	21:30	Networking/ Social Gathering

Schedule continued

start	end	Wednesday
7:30	9:00	Breakfast
9:00	9:10	Announcements
9:10	10:10	**Seminar 3: Recent Advances on the Design of MEMS Readout Circuits Immune to EMI** Franco Fiori, Politecnico di Torino
10:10	10:30	Break
10:30	11:30	**Invited talk 3: Soft Fails as a Tool in Hardware Security Analysis** **Alexander Schlösser, NXP Semiconductors**
11:30	12:10	Report on DG Session A
12:10	13:30	Lunch
13:30	18:00	Open Time
18:00	19:00	Dinner
19:00	20:30	Discussion Group Session B B.1 ESD Induced Soft Failures Moderator: David Pommerenke, ESDEMC B.2 Health monitoring: Can we use Transient Event Detection of EOS/ESD to Build More Resilient Systems? Co-Moderators: Franz Dietz, Henning Lohmeyer, Robert Bosch GmbH; Patrice Besse, NXP Semiconductors B.3 Testing Devices for CDM Below 150 Volts Moderator: Marko Simicic, imec
20:30	21:30	Networking/ Social Gathering

start	end	Thursday
7:30	9:00	Breakfast
9:00	9:10	Announcements
9:10	10:10	**Seminar 4: Stress Current Rise Time Evaluation in the Single-Digit Picosecond-Domain** Johannes Weber, Fraunhofer EMFT
10:10	10:30	Break/Picture
10:30	11:10	Report on DG Session B
11:10	12:00	Technical Session B: System-Level and General Testing Aspects
12:00	13:00	Lunch
13:00	14:20	Poster Discussion Session B
14:20	14:50	Break
14:50	15:50	Technical Session C: Device Physics and Design
15:50	17:15	Poster Discussion Session C
17:15	17:45	Industry Council Report
17:45	18:00	Closing
18:00	19:00	Dinner
19:00	20:00	Hosted reception

start	end	Friday
7:30	9:00	Breakfast
9:00	11:00	Check Out

TRAVEL ARRANGEMENTS & ACCOMMODATION

IEW ACCOMMODATION:

The IEW will take place in a meeting hotel in Jesteburg, Germany. Jesteburg with a first record in 1202 is located just south of Hamburg, in the middle of a wood. In the morning you only hear the rustling of leaves and the bird chirps in the trees. On the first floor there are standard rooms, each equipped with private bathroom facilities, telephone and internet access.
The physical isolation of the location and the absence of distractions encourage extensive interaction among the workshop attendees. Lodging and all meals are included in the registration costs for the workshop.
● Arrangements can be made for those with special dietary or physical requirements. Please send your re¬quirements with your registration or call +1 315-339-6937.

GUESTS AND SPOUSES:

You are welcome to bring a guest to IEW. Double rooms are available for spouses and guests in the same room for 20 Euro per night, which includes breakfast. Lunch and dinner is offered for an additional cost of 18 Euros and 14 Euros, respectively. Guest fees will be charged separately and must be paid directly to the hotel. Attendees must list guests with their initial registration to allow for room arrangements as the number of double rooms are limited

RESPONSIBILITIES OF ATTENDEES:

Please come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees. Enjoy IEW!
In keeping with the relaxed and informal atmosphere of the Workshop, we ask that attendees not overtly solicit, promote, or attempt to sell a commercial product or service at the Tagungshotel Jesteburg. On the other hand, we strongly encourage making business acquaintances and arranging meetings to be held after the workshop.

SURROUNDING AREA:

The meeting hotel is located within walking distance of the center of Jesteburg. The surrounding invites for walks inside the wood. The city of Hamburg is located 30km away. It can easily reached by car and public transport in about 40 minutes.
The city of Hamburg, with 1.8 Mio inhabitants is the second largest city in Germany. It offers a wide range of cultural experiences, from art museums, concert halls to the “Miniatur Wunderland”, the world largest model railroad exhibition. You can visit the second largest port in Europe by boat as well as the old storage district, the Speicherstadt, which became a UNESCO world heritage in 2015. You can also make a trip on the lake Alster in the city center or explore the various channels which pass through the city.
Enjoy your “Free time” and explore the Hansestadt Hamburg!

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Fax: +49 4183 93 91 00
E-Mail: info@tagungshotel-jesteburg.de
Internet: http://www.tagungshotel-jesteburg.de

The Tagungshotel Jesteburg is located about 30km from the city center of Hamburg and 50 km from the International Airport of Hamburg (HAM).
From the airport

Public transport:
There are subways to the main train station (Hamburg Hbf) every 10 minutes. From here, a regional train (RE4) to Bremen and stopping at Buchholz is going ever hour. A bus or a taxi takes you to the Tagungshotel Jesteburg.
For further information please visit: https://www.hvv.de/en
The travel takes about 1 hour 20 minutes.
By Car:
The travel from the airport takes about 1 hour by rental car.
From the main train station (Hamburg Hbf)

Public transport:
a regional train (RE4) to Bremen and stopping at Buchholz is going ever hour. A bus or a taxi takes you to the Tagungshotel Jesteburg.
For further information visit: https://www.hvv.de/en
The travel takes about 45 minutes.
By Car:
The travel from the main train station (Hamburg Hbf) takes about 40 hour by rental car.

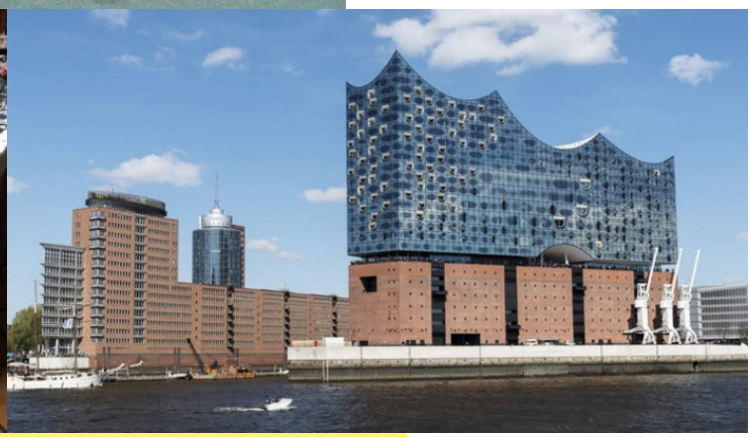
SIGHTSEEING TIPS FOR HAMBURG

1. Hamburg Parliament/City Hall
2. Speicherstadt
3. Miniatur Wunderland
4. ElbPhilharmonie
5. St. Michael‘s Church
6. Landungsbrücken Piers and Old Elbe tunnel
7. Port of Hamburg
8. Reeperbahn
9. Alster lakes

For further information:

https://www.hamburg.com/must-sees/
https://www.hamburg.com/shopping/
https://www.hamburg.com/dine-and-drink/restaurants/



International ESD Workshop Registration Form

May 4-8, 2020 Tagungshotel Jesteburg Hamburg, Germany

Workshop registration includes a room reservation and provided meals

Attendee: _____

Company: _____

Address: _____

City: _____ State: _____ Zip: _____ Country: _____

Phone: (____) _____ E-mail: _____

Address is: *(Please check one)* ☐ home or ☐ office

☐ Please check here if you would like a printed set of notes. ☐ Check if, under the Americans with Disabilities Act, you require any auxiliary aids or services.

•Please List Your Guests: Adults (Name) _____

Guests staying in the room of a registered attendee will be charged 30 EUR per person. Guest fees are payable directly to the Priory

•Please indicate any special dietary needs. _____

Arrival: Date _____ Time _____ • Departure: Date _____ Time _____

☐ Monday Lunch $30 additional fee

Registration Fee $2,195

Discount before March 2nd: members $1,795 / non-members $1,995

The registration fee includes full workshop attendance and handout materials, four nights' lodging* (Mon-Thurs), plus 12 meals* (Monday Dinner-Friday Breakfast), as well as morning and afternoon snacks and drinks.
*Lodging and meals valued at $900

Cancellation & refund requests will be considered if received in writing no later than March 2, 2020, and are subject to a $50 fee. Any other approved dispositions will also be assessed a $50 fee.

Register 5 or more people from one company at the same time and save $100 per person. Please contact EOS/ESD Association, Inc. prior to registering.
Students wishing to apply for a 50% discount on their registration must contact EOS/ESD Association, Inc. prior to registering. No refunds will be issued if discount is not applied at time of original registration.

The German ESD FORUM e.V. supports the attendance of up to five students from Austria, Germany, or Switzerland. Students from these countries may apply for a $1,000 USD grant for IEW attendance from the German ESD FORUM e.V. (info@esdforum.de) until February 24, 2020.

Method of Payment

☐ Check — Only U.S. currency, checks drawn on a U.S. bank that is a member of the U.S. Federal Reserve will be accepted.

☐ Wire transfer — $15 fee

To pay by credit card, register online at http://www.cvent.com/d/phq356

Discussion Groups

I am interested in the following discussion group(s)

Choose one from group A	Choose one from group B
☐ DG A.1	☐ DG B.1
☐ DG A.2	☐ DG B.2
☐ DG A.3	☐ DG B.3

Total Enclosed $ _____

Make checks payable to: ESD Association
Purchase orders not accepted for registration

Posters

Will you be bringing a poster to the open poster session? ☐ Yes ☐ No

If yes, what is the title of your poster? _____

Special Interest Groups

Would you like to form a new SIG? ☐ Yes ☐ No

If yes, what is the proposed topic for your group? _____

Setting the Global Standards for Static Control!

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42nd Annual ELECTRICAL OVERSTRESS/ ELECTROSTATIC DISCHARGE SYMPOSIUM

Sept 14-18, 2020 Peppermill Resort and Casino Reno, NV, USA

CALL FOR PAPERS

TRACK 1: EOS/ESD in Manufacturing – Control Materials, Technologies, and Techniques

Parallel TRACK 2: On-Chip ESD Design, including System Level ESD, Testing, and ESD Case Studies

Submission Deadline: February 10, 2020

About the "EOS/ESD in Manufacturing" Track

For the fourth year, "EOS/ESD in Manufacturing" offers a full track of activities dedicated to EOS/ESD in manufacturing – control materials, technologies and techniques. This manufacturing track focuses on a combination of full and short technical papers, poster presentations, invited papers, discussion groups, workshops, hands-on demonstration sessions, short tutorials, and practical demonstrations of equipment by exhibitors.

The call for papers describes the offerings and submission requirements. Each abstract submission selects the track, format, and suggested area using the abstract toolkit available on the EOS/ESD Association, Inc. website www.esda.org.

Parallel Track Options are:

☐ 1. EOS/ESD IN MANUFACTURING - CONTROL MATERIALS, TECHNOLOGIES, AND TECHNIQUES	☐ 2. ON-CHIP ESD DESIGN, INCLUDING SYSTEM LEVEL ESD, TESTING, AND ESD CASE STUDIES
SUGGESTED SUBMISSION AREA FROM PAGE 3:	SUGGESTED SUBMISSION AREA FROM PAGE 4:
□ STUDENT PAPER	□ STUDENT PAPER
□ FULL TECHNICAL PAPER □ CONSIDER THIS SUBMISSION FOR POSTER SESSION □ SHORT TECHNICAL PAPER OR CASE STUDIES □ CONSIDER THIS SUBMISSION FOR POSTER SESSION □ POSTER SESSION □ DISCUSSION GROUP □ WORKSHOP □ HANDS-ON DEMONSTRATION	□ FULL TECHNICAL PAPER □ DISCUSSION GROUP □ POSTER SESSION

EOS/ESD Symposium CALL FOR PAPERS

TRACK 1: EOS/ESD in Manufacturing – Control Materials, Technologies, and Techniques

Parallel TRACK 2: On-Chip ESD Design, including System Level ESD, Testing, and ESD Case Studies

Submission Deadline: February 10, 2020

About the EOS/ESD Symposium

EOS/ESD Association, Inc. is sponsoring the 42nd Annual Symposium on Electrical Overstress (EOS) and Electrostatic Discharge (ESD) effects. The Symposium is dedicated to the understanding of issues related to electrostatic discharge and electrical transients / overstress, and the application of this knowledge to the solution of problems in consumer, industrial, and automotive applications, including electronic components and manufacturing, as well as in systems, subsystems, and equipment.

Papers/Contributions

The Technical Program Committee solicits symposium contributions, including data and analysis that advance the state-of-the-art knowledge, enhance or review the general knowledge, or discuss new topics related to EOS/ESD.

Special attention will be dedicated this year to "Relationships and Interactions between ESD and EMC". The technical program committee would like to highlight this focus area and requests submission of various contributions (e.g., full papers, workshop & short tutorial proposals…). Topics such as ESD/EMI interaction, design and testing issues, robust and innovative solutions to address ESD & EMC requirements, ESD/EMC modelling approaches are encouraged.

Electronic Submissions

Abstract submissions shall be made electronically via an emailed PDF file to **info@esda.org**. One file for each submission is required.

Deadlines

The abstract submission deadline is Monday, February 10, 2020. Abstracts not meeting guidelines may not be accepted. The final submission deadline for the finished papers is Friday, June 1, 2020. **ESDA reserves the right to withdraw any paper or presentation that does not meet the guidelines, including deadlines. Your paper MUST be submitted by the deadline.** Final full technical papers will be limited to a maximum of 10 pages - guidelines will be provided after acceptance of the paper.

Paper Acceptance

The Technical Program Committee accepts unpublished papers for peer review with the understanding that the author will not publish the work elsewhere prior to presentation at the Symposium. Presentation of your work at the earlier International ESD Workshop (IEW) or the Symposium for Manufacturing Issues will not preclude your Annual Symposium abstract submission. The submission must follow guidelines and be expanded significantly in the abstract submission for the EOS/ESD Symposium. Publication of accepted papers in any form prior to presentation at the Symposium may result in the paper being withdrawn from the Symposium Proceedings. Authors must obtain appropriate company and government clearances prior to submitting their abstracts.

Paper Awards and Recognition

Awards are presented annually for the Symposium Outstanding Paper (selected by Symposium attendees), the Best Paper (selected by the Technical Program Committee), and the Best Student Paper. The Best Paper is considered for presentation at the RCJ EOS/ESD Symposium in Japan. The Outstanding Paper is considered for presentation at the ESD Forum in Germany. Eligible student contributions for the Best Student Paper Award should be marked as such by the authors at the time of abstract submission.

Accepted full technical papers covering selected topics may be considered for review for invited publications in IEEE Transactions on Device and Materials Reliability (TDMR), IEEE Transactions on Electron Devices, the Microelectronics Reliability Journal, the Journal of Electrostatics, or other appropriate publications.

Sponsored by EOS/ESD Association, Inc. in cooperation with IEEE.
Technically co-sponsored by the Electron Devices Society.

Papers / Presentations / Discussion / Hands-on Demonstration Sessions in Track 1. EOS/ESD in Manufacturing – Control Materials, Technologies, and Techniques are solicited in the following areas and formats:

A. Full Technical Paper

Authors must submit a maximum 50-word abstract and 4-page maximum summary of their work. The summary must clearly state the purpose, results (e.g., data, diagrams, photographs, etc.), and conclusions of the work. Summaries must also include references to prior publications and state how the work enhances existing knowledge. Authors suggest the appropriate technical area related to their submission. Authors are required to use the abstract submission toolkit available on the EOS/ESD Association, Inc. website www.esda.org.

B. Short Technical Paper or White Paper with Presentation of Case Studies

Authors must submit a maximum 50-word abstract and 2-page maximum summary of their work. The summary must clearly state the purpose, results (e.g., data, diagrams, photographs, etc.), and conclusions of the work. Summaries must also include references to prior publications and state how the work enhances existing knowledge. Authors suggest the appropriate technical area related to their submission. Authors are required to use the abstract submission toolkit available on the EOS/ESD Association, Inc. website www.esda.org.

C. Poster Session

Authors must submit abstracts in the form of a short PowerPoint presentation. After the title slide, the second slide of the presentation should describe the objective and significance in a maximum 200-word summary. The abstract presentation should not exceed 5 additional slides; with representative data and figures that will be the foundation for the longer poster maximum of 24 slides that you plan to present. A formal five-minute presentation is given by each author followed by the poster session. Authors are required to use the abstract submission toolkit available on the EOS/ESD Association, Inc. website www.esda.org.

D. Workshop or Discussion Group

Proposals for workshops and discussion groups must be submitted with an abstract describing the proposal. The abstract toolkit is used to indicate participation as a workshop moderator or committee participant. **Workshop** topics address fundamentals, generally accepted techniques, and consider present and future challenges and solutions to problems. **Discussion Group** topics address EOS/ESD novel ideas and consider new developments or common myths dispelled. The discussion should encompass some provocative points of view.

E. Hands-on Demonstration

Proposals for hands-on demonstrations of measurement techniques must be submitted with an abstract defining the presentation and measurement. Authors complete a presentation describing the measurement technique followed by a hands-on station for attendees to perform the measurement as described. Application, limitations, and common pitfalls should be discussed. Authors are required to use the abstract submission toolkit available on the EOS/ESD Association, Inc. website www.esda.org. (Note: ESDA does not provide equipment).

Track 1 Suggested Submission Areas:

- ESD Packaging and Handling Procedures
- EOS/ESD Detection and Measurement Techniques
- ESD Facility Design, Mitigation in Test and Manufacturing; Ionization
- Manufacturing EOS/ESD Case Studies, Reviews and Analysis
- EOS/ESD Process Assessment
- ESD Control in Industry 4.0
- ESD Control Materials and Use of Antistatic Materials
- ESD Issues in 2.5D & 3D Stacking and TSV
- Control Program Topics (Cost/Benefit Analysis, training, etc.)
- ESD control in Explosives & Pyrotechnics, Oil/Petroleum/Biomedical/Chemical Industry
- Standards – Comparison and Analysis
- ESD Control with IoT Technology

Contact information for questions or further information:

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E-mail: souvick.mitra@globalfoundries.com

EOS/ESD in Manufacturing Chair: Michelle Lam, IBM
EOS/ESD in Manufacturing Co-Chair: Dale Parkin, Seagate Technology

Papers / Presentations for Track 2. On-Chip ESD Design track, including System Level ESD, ESD Testing, ESD Case Studies are solicited in the following areas:

A. Full Technical Paper

Authors must submit a maximum 50-word abstract and 4-page maximum summary of their work. The summary must clearly state the purpose, results (e.g., data, diagrams, photographs, etc.), and conclusions of the work. Summaries must also include references to prior publications and state how the work enhances existing knowledge. Authors suggest the appropriate technical area related to their submission. Authors are required to use the abstract submission toolkit available on the EOS/ESD Association, Inc. website, www.esda.org.

B. Workshops and Discussion Groups

Proposals for workshops and discussion groups must be submitted with an abstract describing the proposal. The abstract toolkit is used to indicate participation as a moderator or committee participant. **Workshops** address fundamentals and generally accepted techniques. Topics consider present and future challenges and solutions to problems. **Discussion Groups** address EOS/ESD novel ideas. Ideas consider new developments or common myths dispelled. The discussion should encompass some provocative points of view.

C. Poster Session

Authors must submit abstracts in the form of a short PowerPoint presentation. After the title slide, the second slide of the presentation should describe the objective and significance in a 200-word maximum summary. The abstract presentation should not exceed 5 additional slides; with representative data and figures that will be the foundation for the longer poster maximum of 24 slides that you plan to present. A formal five-minute presentation is given by each author followed by the poster session. Authors are required to use the abstract submission toolkit available on the EOS/ESD Association, Inc. website, www.esda.org.

Track 2 Suggested Submission Areas:

I. Advanced CMOS (Analog/Digital) EOS/ESD and Latch-up

- ESD Issues in Advanced Technologies (Multi-gate, FinFET, SOI, SiGe, Compound, Graphene, nanowire, etc.)
- On-Chip ESD Protection Devices & Techniques in Advanced CMOS Technologies
- IC Design and Layout Issues
- Circuit Simulation of EOS/ESD Events in Advanced CMOS Technologies
- DC/Transient Latch-up Issues and Solutions, Troubleshooting, Simulation
- ESD Issues in 2.5D & 3D Stacking and TSV

II. ESD Protection in Bipolar, RF, High Voltage and BCD Technologies

- ESD Issues in Bipolar, RF, High Voltage, and BCD Technologies and power Technologies (SiC, GaN, etc.)
- On-Chip ESD Protection Devices & Techniques in Bipolar, RF, High Voltage and BCD Technologies
- IC Design and Layout Issues
- Circuit Simulation of EOS/ESD Events in Bipolar, RF, High Voltage, and BCD Technologies
- DC/Transient Latch-up Issues and Solutions, Troubleshooting, Simulation
- ESD Circuit Simulation and Co-Design

III. Numerical Modeling and Simulation for On-Chip ESD Protection

- ESD Device TCAD Simulation
- Simulation Tool and Methodology
- Numerical Modeling and Physics of EOS/ESD Events
- TCAD/Circuit Co-simulation

IV. EOS/ESD Failure Analysis, Troubleshooting and Case Studies

- EOS/ESD Case Studies, Reviews and Analysis
- EOS/ESD Phenomena in MEMS (Microelectromechanical Systems)
- Failure Analysis Techniques and Interpretations
- EOS/ESD Component Failure Analysis
- Testing of MR/TMR Heads and Ultra-Sensitive Devices
- EOS/ESD Protection for Aircraft, Spacecraft, and Avionics

V. Device Testing: Testers, Methods and Correlation Issues

- Transmission Line Pulse Testing Systems
- Novel EOS/ESD Test Methods
- Novel TLP Measurement Results
- HBM, CDM Tester Issues and Solutions
- Tester Correlation Issues
- Standards – Round-Robin Testing, Results and Analysis

VI. System Level EOS/ESD/EMC, HMM

- System Level EOS/ESD/EMC Test Methods
- System Level EOS/ESD Modeling and Simulation
- EOS/ESD Simulators, Calibration and Correlation
- Transient ESD/EMI Induced Upset
- Case Studies, Reviews and Analysis
- Standard Test Boards as an Early Measure of Robustness

VII. Chip/Module/Package EOS/ESD Electronic Design Automation

- Novel EOS/ESD EDA Tools
- ESD Checking and Verification Methodology
- Application of EDA tools for EOS/ESD Failure Analysis, Design and Verification

Contact information for questions or further information:

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Phone: 802-769-2642
E-mail: souvick.mitra@globalfoundries.com

EOS/ESD Manufacturing Symposium in China

Anthea Hotel, Shenzhen, China
October 19-24, 2020

The EOS/ESD Association is organizing the EOS/ESD Manufacturing Symposium China. The EOS /ESD Manufacturing Symposium in China is focused on discussing issues and providing answers to electrostatic discharge in electronic production and assembly.

Call For Presentations

Abstract Submission Deadline May 8, 2020

Submission Instructions

Your presentation abstract (two slides including reasonably sized figures) must clearly present the data and the significance of the results. Please e-mail your presentation abstract including title, author affiliation, and e-mail address to info@esda.org by May 8, 2020 (Friday) deadline. Notification of acceptance will occur by August 3, 2020. Final, full presentations for EOS/ESD Manufacturing Symposium in MS PowerPoint® format must be received by October 9, 2020. These MS PowerPoint® slides will be included in the presentation handout that will be distributed during the Symposium. There will be no published proceedings of the Symposium. Technical papers that have been previously published may be considered.

For more information and registration please visit the ESDA website at www.esda.org/manufacturingsymposium/

Please visit the web page at http://www.esda.org/manufacturingsymposium / for regular updates on the Symposium. As it becomes available, we will post information on the full technical program including tutorials, seminars, technical sessions,discussions, workshops, and exhibits.

EOS/ESD Manufacturing Symposium would like you to consider presentation abstract submission topics such as:

I. EOS/ESD Factory Level and Materials Technology

- Packaging and Handling
- Case Studies, Reviews and Analysis
- Test Methods and Procedures
- Troubleshooting Techniques
- Air Ionization and Uses
- Facility Design
- ESD Shunting Packaging Technology
- ESD Control Materials
- ESD Detection and Measurement Techniques
- Management Issues (cost/benefit analysis etc.)

II. EOS/ESD Standards – Components, System, Factory, & Materials

- Test Methods and Procedures
- Standards - Comparisons and Analysis
- ESD Control Program Development
- Case Studies
- Round-Robin Testing, Results, and Analysis

Events Director:
Nate Peachey, Qorvo

Local Chair:
Tay, Chin Siang, Canmax

Mark Your Calendar!

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If you are interested in sponsoring this event please contact: EOS/ESD Association Inc., Phone +1-315-339-6937, info@esda.org

Setting the Global Standards for Static Control!

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December 23, 2019 3:23 PM

EOS/ESD Association, Inc. Tutorial Bundle in Chicag

June 16 - 17, 2020

DoubleTree by Hilton O'Hare – Rosemont 5460 North River Road Rosemont, IL 6001

June 18, 2020 Professional Program Manager Exam (Optional)

FC340: ESD Program Development and Assessment (ANSI/ESD S20.20)

JUNE 16 - 17, 2020 8:00 AM - 5:00 PM

John T. Kinnear, IBM Corporation; Dave Swenson, Affinity Static Control Consulting

Certification: PrM

This seminar provides instruction on designing and implementing an ESD control program based on ANSI/ESD S20.20. The cours provides participants with the tools and techniques to prepare for an ESD facility audit. This two-day course is an ESDA certificatio requirement for in-plant auditors and program managers who are working toward professional ESD certification.

The following topics are covered in this course:

- Overview of ANSI/ESD S20.20
- How to approach an assessment
- Administrative elements
- ESD program assessment
- ESD program techniques for different applications
- Technical elements
- Overview of the assessment process
- The audit checklist and follow-up questions

It is recommended that the ESD Program Development and Assessment (ANSI S20.20) be taken after the certification candidat has taken most of the other program manager related tutorials.

JUNE 18, 2020 8:00 AM - 5:00 PM

Optional Program Manager Exam

EOS/ESD Association, Inc. Tutorial Bundle in Chicago

April 20 - 21, 2020

DoubleTree Hotel Chicago - Oakbrook 1909 Spring Road, Oak Brook, Illinois, 60523, USA

June 16 - 17, 2020

DoubleTree by Hilton O'Hare – Rosemont 5460 North River Road Rosemont, IL 60018

June 18, 2020 Professional Program Manager Exam (Optional)

First Name: _____ Last Name: _____

Company Name: _____

Street: _____ City: _____

State/Province: _____ Country _____ Zip/Postal Code:_____

Address is (please circle the one that applies) Home or Company

Phone: _____ E-mail: _____

Tutorial Selection

☐ **April 20 ESD Basics for the Program Manager**	**$510 USD/ non-member $610 USD**
☐ **April 21 How To's of In-Plant ESD Auditing and Evaluation Measurements**	**$510 USD/ non-member $610 USD**
☐ **June 16-17 ESD Program Development & Assessment (ANSI/ESD S20.20)**	**$1,510 USD/ non-member $1,610USD**
☐ **Professional Program Manager Certification Exam (Optional)**	**$60 USD**

NOTE: You must initiate an official file in your name at EOS/ESD Association, Inc., pay the $50 USD filing fee, and complete all pre-requisite courses to be eligable to take the exam.

Exclusive 10 course bundle
Certified Program Manger Certification

☐ **3 face to face courses: ESD Basics, How To's and S20.20** — **$5,000 USD**

7 Online courses: (Class links provided upon payment)

- Cleanroom Considerations for the Program Manager
- Ionization Issues and Answers for the Program Manager
- System Level for the Program Manager
- Packaging Principles for the Program Manager
- ESD Association Standards Overview
- Device Technology and FA Overview
- Electrostatic Calculations for the Program Manager

Register Online for April at: http://www.cvent.com/d/nhq0s2

Register Online for June at: http://www.cvent.com/d/phq0x6

To register for the bundle, please use the April link.

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