2020

International Electrostatic Discharge Workshop
March 29 - April 2, 2020

IEW

Setting the Global Standards for Static Control!
EOS/ESD Association, Inc. 7900 Turin Rd., Bldg. 3 Rome, NY 13440-2069, USA
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ESD ASSOCIATION

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The IEW Experience

On behalf of the IEW Management Committee and EOS/ESD Association, Inc., welcome to the 14th annual International ESD Workshop!
IEW is an informal workshop that attracts some of the most recognized experts in the field, by virtue of its unique format: focus is on key themes, which are addressed through a multitude of events, with a strong emphasis on attendees' interaction.

This year's edition is centered around Latchup, EOS vs ESD, and ESD vs EMC. These topics will be tackled through ad-hoc tutorials, high-profile keynote speakers, technical sessions, and discussion groups.

Additionally, there will be an informal evening program, where the most "hard-core" ESD experts can continue their discussions.

Every attendee has something to share and to learn, and that is why the social aspect is so prevalent. For this reason, as is the IEW tradition, fun will not be forgotten with Tuesday afternoon devoted to a multiple-options social event. This is a great opportunity to get to know your EOS/ESD colleagues better and expand your network.

Furthermore, following last year's successful model, IEW will continue to be fully embedded into IRPS, which provides additional value to our attendees:

- As an IEW registered attendee, you can attend **every event**, including tutorials and high-profile keynote speakers, at IRPS
- IRPS and IEW programs are synced to maximize events attendance flexibility

Bottom line: by registering to IEW, you are going to get the best of the IEW and IRPS worlds.

We are looking forward to meeting you all in Dallas!

Tutorial Sunday 1:30 – 3:00 PM

Electronic Design Automation (EDA) Solutions for Latch-up Verification in CMOS and HV Technologies

Instructor: Michael Khazhinsky, Silicon Labs

The verification of latch-up protection networks in CMOS and HV technologies is a difficult challenge. There are several factors including increasing design and process complexity, higher-pin counts, wide operating voltage ranges, and the overall computational difficulties in dealing with large data sets. Traditional latch-up geometrical rule checks using DRC tools can only provide limited verification. These checks are typically focused on layout topology. However electrical information for latch-up risk areas throughout the chip is not readily available. While DRC checks are still useful at early design stages, relying on conventional DRC latch-up checking exclusively, poses a significant risk of missing hidden latch-up pitfalls. Consequently, a fully automated latch-up rule checking approach analyzing electrical information is highly desired.

In this tutorial we will review the essential requirements of the latch-up electronic design automation (EDA) verification flow. Then an overview of existing latch-up EDA solutions across the industry will be given. We will introduce generic rules that can be used as basis for a typical latch-up EDA verification flow in CMOS and HV technologies. Finally, recommendations for future EDA tool development and standardization will be provided.

Michael G. Khazhinsky is currently a Principal ESD engineer/designer at Silicon Labs in Austin, Texas. Prior to joining Silicon Labs, he worked at Motorola and Freescale Semiconductors where he was in charge of the TCAD development and ESD/latch-up protection solutions for emerging process technologies, with a focus on ESD-EDA. Michael has M.S.E.E. and M.S. Physics from the Moscow State Institute of Electronic Engineering, and Ph.D. in Physics from Western Michigan University. Michael is the Chair of ESDA Working Group 18 on EDA. Michael has served as a member of the IRPS, IEW, ESREF, EMC and EOS/ESD Symposium Technical Program Committees, as well as a Workshop Chair, Technical Program Chair, Vice General Chair and General Chair of EOS/ESD Symposium. He currently serves on the Technical Program Committees of 2020 International Reliability Physics Symposium, 2020 International ESD Workshop, and 2020 EOS/ESD Symposium. Michael co-authored over 30 papers and gave a number of invited talks on ESD, EDA, process/device TCAD, and photonic crystals. He was a recipient of seven EOS/ESD Symposium and SOI Symposium “Best Paper” and “Best Presentation” awards as well as Industry Pioneer Recognition Award. Michael currently holds eighteen patents on ESD design, with additional patents pending. Michael is a Senior Member of IEEE and the Director of the ESD Association.

Tutorial Sunday 3:30 – 5:00 PM

EOS, ESD, Transient, AMR, EIPD, Robustness, Aging - Do All of These Pieces go to the Same Puzzle?

Instructor: Hans Kunz, Texas Instruments

Electrical Over-Stress (EOS) continues to be one of the largest categories of Customer Returns of Integrated Circuits (ICs). In recent years, there has been resurgence in interest in EOS, including recent attempts by the Industry to better define terms and concepts related to EOS, in hopes of helping suppliers and customers better address the issues. This presentation will examine EOS in relationship to Absolute Maximum Ratings (AMR) and the newly defined term Electrically Induced Physical Damage (EIPD), with an ultimate goal of continuing a conversation about the state of EOS trouble-shooting and how more precise terms and concepts can be harnessed in the process of root-cause analysis. The presentation will also explore relationships between EOS and ESD and contemplate whether combining or separating these categories is ultimately helpful in addressing the EOS problem. Similarly, the relationship between EOS and device Aging will be explored. The complexity of specifying limits for transient events and the complexity of attempting to define or measure EOS robustness will also be discussed.

Hans Kunz joined Texas Instruments as an ESD specialist in 2003, after nine years at Dallas Semiconductor/Maxim. He was elected Distinguished Member of Technical Staff at Texas Instruments in 2017. His past responsibilities include the design, development, and implementation of ESD protection circuits for analog CMOS and high-voltage BiCMOS technologies; he is currently focused on the development of ESD verification tools and methodologies. Hans has been active in the workshop process at both the EOS/ESD Symposium and IEW, serving as both panelist and moderator at various workshops and serving as the EOS/ESD Symposium Workshop Chair in 2010. He has been a frequent member of the EOS/ESD Symposium technical program committee, served as the IEW TPC chair in 2016, and the IEW Management Committee chair in 2017. Hans has also been active in the educational tutorial process of the EOS/ESD Symposium, serving as an instructor since 2007. Hans is co-author of multiple publications related to ESD and received the *Best Presentation Award* for the 2006 EOS/ESD Symposium. He holds 13 patents in the area of ESD protection. Hans received his BS degree in physics from *The University of the South* and his BS in electrical engineering from *The Georgia Institute of Technology*.

Tutorial Monday 8:00 – 9:30 AM

Exploring Relation of ESD and EMC: Tests, Events to Damage, Failure Types, and Co-Design Approaches

Instructor: Alan Righter, Analog Devices

This tutorial will explore the events of EMC and ESD as they relate to test methods, damage signatures from the different tests in ICs, and co-design approaches addressing EMC and ESD. First, the various tests will be described and compared to one another. Next common damage signatures for each type of event will be described. With this information, the concept of co-design can be explored to relate to the type of event and the damage signature the co-design is designed to protect. Some co-design tradeoffs may be needed in the consideration of what events are most likely / important in a particular application, but could conflict in co-design, and these will be described.

Alan Righter has been with Analog Devices since 1997 and currently a Senior Staff ESD Engineer in Santa Clara, CA, involved in customer ESD and EOS (EIPD) return resolution, manufacturing ESD control, and IC design / consulting. From 1984 to 1997, Alan worked at Sandia National Laboratories, Albuquerque, NM and received his PhD in Electrical Engineering from the University of New Mexico in 1996. Alan has been with the EOS/ESD Association also since 1997 and currently is their 2020-21 Association President, and also is ESDA co-chair of the Joint ESDA/JEDEC CDM (Charged Device Model) Standard Working Group responsible for the ANSI/ESDA/JEDEC JS-002 CDM testing standard.

Tutorial Monday 10:00 – 11:30 AM

Full chip CDM ESD Verification
Instructor: Melanie Etherton, NXP

While the basic principle of protecting integrated circuits (ICs) from damage caused by electrostatic discharge (ESD) events is pretty simple, the details of implementing a full chip protection strategy that has minimal impact on area and leakage, does not limit the functionality or performance of the circuit it is protecting, and prevents any damage from ESD events that ICs are exposed to can be very challenging. The nature of Charged Device Model (CDM) ESD events, where charges are distributed over the complete IC and package and discharge currents flows through internal circuitry, significantly increases the challenge for designing an ESD robust product. For CDM ESD, every aspect of the IC integration can have an impact on the overall product robustness, including the placement of local CDM protection for domain crossings, the primary ESD protection for power and ground domains and seemingly small details in the power and ground grid implementation. This tutorial provides insight to a complete set of verification strategies that will ensure predictive capabilities for CDM ESD robustness, including complex products with billions of transistors, sensitive analog circuitry and multiple power and ground domains.

Melanie Etherton is a principal engineer at NXP Semiconductors in Austin, Texas where she designs ESD protection for automotive products in advanced CMOS technologies and develops methodologies to ensure full-chip ESD robustness, including new EDA tools. She has almost 20 years of experience in the field of ESD, including her doctoral research work at Robert Bosch GmbH, Germany for her PhD from the Swiss Federal Institute of Technology (ETH Zurich). She has authored and co-authored numerous papers in the field of ESD and holds several patents in that area. Dr. Melanie Etherton has served as TPC Chair, Vice and General Chair of the EOS/ESD Symposium from 2014 through 2016.

IRPS Keynote

Tuesday 9:05-9:40 AM

The Future of Compute: Reliability and Resiliency in the Era of Data Transformation

Michael C. Mayberry, Intel

The digital transformation continues to gain momentum and is changing the shape of business, industry and consumers around the world. This transformation is characterized by continued strong demand for compute at all points in the network – at the core, the edge, and at the endpoints. Data continues to grow at an exponential rate and not only drives the compute requirements, but also requires efficient solutions for movement and storage of data that is critical for overall performance. From device to cloud, new applications and use cases are continuously emerging. This transformation demands that we adapt our thinking and move from a hardware/program centric to a data/information centric approach, and to embrace new ways to compute. To keep pace in this dynamic environment, Moore's Law and its impact have become more relevant than ever. The continued dimensional, materials and device scaling drives a renewed focus on the fundamental reliability physics of devices and materials, while novel architecture integration schemes and large-scale system design innovation motivates a more comprehensive understanding of resiliency at all levels of the system.

Dr. Michael (Mike) C. Mayberry is the chief technology officer at Intel Corporation. He is a senior vice president and general manager of Technology Development, where he is responsible for the research, development and deployment of next-generation silicon logic, packaging and test technologies that will produce future Intel products.

Since joining Intel in 1984 as a process integration engineer, Mayberry has held a variety of positions. As part of the California Technology Development team, he developed EPROM, flash and logic wafer fabrication processes. In 1994, he moved to Sort Test Technology Development, responsible for roadmaps and development of test processes for Intel microprocessors. In 2005, he moved to Components Research and was responsible for research to enable future process options for Intel's technology development organizations. In 2015, he moved to Intel Labs and became responsible for Intel's product-driven research. In 2018, he moved to the Technology Development group at Intel.

Mayberry received his bachelor's degree in chemistry and mathematics from Midland College and his Ph.D. in physical chemistry from the University of California, Berkeley.

IRPS Keynote

Tuesday 9:40-10:15 AM

Power Semiconductor Reliability – An Industry Perspective on Status and Challenges

Oliver Häberlen, Infineon Technologies Austria AG

Power transistors are an inevitable key component of nearly every power electronic system enabling the path to a greener environment through increased conversion efficiency. Silicon based power transistors are established on the market since more than half a century and the reliability and quality of those devices has matured to failure levels in the sub ppm range. The base for this achievement was a deep understanding of all the failure modes and their corresponding lifetime models.
The new wide band gap power semiconductor materials SiC and GaN that have entered the market during the past respective this decade are on much earlier points along a similar learning curve. It will be shown that the methodology how to qualify a power semiconductor technology remains essentially unchanged for the new devices, but of course all the new material and device specific failure modes need to be understood and modelled. The most important past learnings will be shown in this talk. So everything is solved for the established silicon technologies? Also, here we face new challenges due to the ever-continuing pressure for cheaper devices mostly addressed by device shrinks. Pushing the devices closer and closer to their physical limits of course also requires refining and improving the established models in order to tailor the exactly right amount of safety margin. Additionally, increasing power and current densities on die level require new package concepts leading to potential new failure modes. Finally, we will conclude with some examples on a general trend observed: Fitting the devices as good as possible to the target applications and their respective requirements is leading to the need for an increased focus on application reliability testing

Dr. Oliver Häberlen received his M.S. and Ph.D. degree in physics from the University of Munich and Technical University of Munich respectively.

He is currently employed with Infineon Technologies Austria AG as a Senior Principal for Power Transistor Technology and heading the group for advanced technology concepts evaluating future silicon and wide band gap (SiC, GaN) power device concepts for improved energy conversion solutions. His research areas include low and medium voltage trench power MOSFETs, high voltage super junction devices, GaN power devices and power device reliability. He is a senior member of IEEE and member of the IEEE EDS Power Devices and ICs Technical Committee. He also served as Technical Committee member for IEDM (International Electron Devices Meeting) and ISPSD (International Symposium on Power Semiconductor Devices and ICs) and is the General Chair of the ISPSD conference in 2020. He is author and co-author of over 100 international patents and patent applications in the field of power semiconductors.

IEW Keynote

Tuesday 10:15-11:00 AM

IoT End-node Device: Built to Last
Alessandro Piovaccari, Silicon Labs

End-node IoT devices are aimed to ubiquitous adoption, with projections of over a trillion installed devices within the next 5-10 years. This translates to requirements such as low-energy consumption and long product life cycles while meeting demanding low-cost constraints. From the engineering point of view, upgradeability, security and reliability are among the main issues to solve. Traditional design techniques based on worst case analysis do not provide the required level of optimization in this case which in turn provides ample opportunities for more innovation.
In this keynote, we will show how knowledge of the usage context and application must be used to achieve this complex and multi-faceted goal. Moreover, the fact that these devices are almost always wirelessly connected to the cloud, can be used to our advantage for monitoring and improving their lifetime in the field via methods such as machine learning.

As Silicon Labs' Chief Technology Officer, **Alessandro Piovaccari** is responsible for the company's product and technology research and development. Alessandro joined Silicon Labs in 2003 to design the company's single-chip FM radio products, which have surpassed 1.5 billion device shipments. He co-architected Silicon Labs' single-chip TV tuner IC, used by nine of the world's top ten TV makers, with more than 70 percent market share and 1.25 billion unit shipped. Previously, Alessandro worked as a research scientist at Tanner Research, joining the company in 1997 to develop CMOS neuro-inspired image processors.
From 1998 to 2003, he was a member of the design services team at Cadence Design Systems, focusing on CMOS RFICs and high-speed SerDes IP development.
Alessandro holds 38 patents and is a Senior Member of IEEE, a Full Member of AES, and a Member of the Forbes Technology Council. Alessandro received Laurea and PhD degrees in electronic engineering and computer science from the University of Bologna in Italy and a Post-Master's Certificate with Honors in electrical

engineering from Johns Hopkins University. He also serves as a board member for the Skillpoint Alliance, a member of the advisory council of UTeach Natural Sciences at The University of Texas at Austin, College of Natural Sciences, an advisor for the Center for Leadership Education, G. W. Whiting School at John's Hopkins University, and he is an IEEE CICC Conference steering committee member.

IRPS Keynote

Wednesday 11:00-11:35 AM

Reliability Drives Semiconductor Industry Evolution

Dr. Walden Rhines – Mentor

Attention to reliability issues has evolved from a focus on burn-in and rigorous testing to designed-in reliability and evolving methods for modeling physical failure mechanisms, intelligent verification of layouts and machine learning. Dr. Rhines has participated in much of this evolution as a semiconductor executive at Texas Instruments and CEO of Mentor Graphics. He will highlight some of the lesser known history of reliability improvements and propose a roadmap for the future.

WALDEN C. RHINES is CEO Emeritus of Mentor, a Siemens business, focusing on external communications and customer relations. He was previously CEO of Mentor Graphics for 25 years and Chairman of the Board for 17 years. During his tenure at Mentor, revenue nearly quadrupled and market value of the company increased 10X. Prior to joining Mentor Graphics, Dr. Rhines was Executive Vice President, Semiconductor Group, responsible for TI's worldwide semiconductor business. During his 21 years at TI, he was President of the Data Systems Group and held numerous other semiconductor executive management positions. Dr. Rhines has served on the boards of Cirrus Logic, QORVO, TriQuint Semiconductor, Global Logic and as Chairman of the Electronic Design Automation Consortium (five two-year terms) and is currently a director. He is also a board member of the Semiconductor Research Corporation and First Growth Children & Family Charities. He is a Lifetime Fellow of the IEEE and has served on the Board of Trustees of Lewis and Clark College, the National Advisory Board of the University of Michigan and Industrial Committees advising Stanford University and the University of Florida. Dr. Rhines holds a Bachelor of Science degree in engineering from the University of Michigan, a Master of Science and PhD in materials science and engineering from Stanford University, a Master of Business Administration from Southern Methodist University and Honorary Doctor of Technology degrees from the University of Florida and Nottingham Trent University.

Seminars

Three recognized experts from industry will give seminars on critical topics at this year's IEW. The first two seminars (by Rajkumar Sankaralingam, Texas Instruments, and Michi Stockinger, NXP) will focus on different angles of the IEC On-chip ESD protection design challenges. The topic, a main theme through the entire IEW program, is becoming especially critical following the requirements from the Automotive Industry. A third seminar (by Charvaka Duvvury, ESD Consulting) will update the audience on the Roadmap of the ESD Industry Council on the ESD target levels.

Seminar 1

On-Chip HV Transient IEC Design Challenges

Rajkumar Sankaralingam, Texas Instruments, Dallas, Texas

The criticality of Analog Technologies has significantly increased over the last decade, due to the phenomenal success of portable consumer electronics, which require multiple analog functions to be implemented in the same chip. The relatively recent push towards society "electrification" (electric cars, smart power grids, IoT) is driving the need for higher and higher voltage applications together with a plethora of functional and safety requirements, which pose significant challenges in terms of ESD Design. This seminar discusses these challenges.

Raj Sankaralingam has a PhD in Electrical Engineering from University of Notre Dame. Raj joined TI in 2005 to support ESD design and development for CMOS Analog products. Since 2009 he has been managing ESD design team where he oversees ESD support for all TI product lines. Raj has enabled first-pass ESD success in hundreds of products in various technologies over the years and made significant contributions to ESD development and ESD tool infrastructure within TI.

Seminar 2

On-chip Protection from System-Level Fast Transient Stress Event

Michi Stockinger, NXP, Austin, Texas

Harsh electrical environments often require microcontroller chips to have built-in system-level protection against fast transient stress events like powered ESD (PESD) or other IEC61000-4 type events. With ultra-low system cost requirements, additional discrete protection components like TVS diodes must be avoided. This talk describes area-efficient on-chip protection design methods suitable for I/O port protection in CMOS technologies without board-level ESD components. The main goal is to prevent chip damage and major disturbance of the IO supply during system-level stress, and to also meet component-level ESD requirements (HBM and CDM).

Michael "Michi" Stockinger received his PhD in electrical engineering with highest honors from Vienna University, Austria, in 2000. His doctoral research focused on the optimization of ultra-low-power CMOS transistors. In 2000, he moved to Austin, Texas to join Motorola's semiconductor sector, which became Freescale Semiconductor in 2004 and then NXP Semiconductors in 2016. Michael's focus has been on ESD protection and LU prevention for advanced CMOS products. He is a Technical Director of ESD design in NXP's MCU/MPU Engineering division. Michael's on-chip ESD solutions have been implemented in the Kinetis, i.MX, and ColdFire product lines. His latest research interests are in the field of on-chip protection solutions for system-level transient immunity. Michael was awarded the 2001 EOS/ESD Symposium Best Paper award, the 2003 EOS/ESD Symposium Best Paper and Best Presentation awards, and the 2013 EOS/ESD Symposium Best Paper and Outstanding Paper awards. He has authored over 35 technical papers and holds more than 25 patents. He has served in the TPC of several EOS/ESD Symposia, International Reliability and Physics Symposia and International ESD Workshops, and he teaches an ESDA tutorial.

Seminar 3

Industry Council on ESD Target Levels: Review of Achievements, Activities, and Initiatives

Co-chairs: Charvaka Duvvury, ESD Consultant / Harald Gossner, Intel Corporation

The Industry Council on ESD Target Levels, founded during 2006, has been active with the mission to recommend realistic specifications and test methods for ESD to be compatible with advanced technologies and the prevailing demand for high speed circuit performance. While the recommended changes to spec target levels consider component level HBM and CDM, the proposed test methods involve new understanding of more efficient system-level ESD design and evaluation. This review will first briefly cover the key accomplishments of the Council that changed the industry qualification processes for ESD reliability, followed by overview of the recent technical initiatives to understand electrical overstress (EOS) and the corresponding myriad of root causes, the recommended methods to mitigate EOS damages, as well as the notion of Absolute Maximum Rating (AMR) as it relates to probability of EOS during applications. Finally, there is currently an industry survey in preparation to collect input for recommendations for Latchup reliability testing that will be briefly discussed.

Charvaka Duvvury received his PhD in Engineering Science from the University of Toledo and worked as a post-doctoral fellow in Physics at the University of Alberta before joining Texas Instruments in the Advanced DRAM Development Group. His experience at TI spanned for 35 years in semiconductor device physics with development work in ESD design. He was elected as TI Fellow in 1997 and as IEEE Fellow during 2008. He has contributed to the industry by offering tutorials at various IEEE sponsored conferences and is an active participant in the EDS DL Program. He is currently working as a technical consultant on ESD design. He is a recipient of the IEEE Electron Devices Society's Education Award (2013), Outstanding Contributions Award from the EOS/ESD Symposium (1990), and Outstanding Industry Mentor Award from the Semiconductor Research Council (1994 and 2012). From 2004-2006 he served on the IEDM CMOS Reliability Sub-committee. He has published over 150 papers in technical journals and conferences and holds US 75 patents. He co-authored and contributed to 5 books. Charvaka has been serving on Board of Directors of the ESD Association (ESDA) since 1997 promoting ESD education and research at academic institutes. He served twice as General Chairman of the ESD Symposium. He is co-founder and co-chair of the Industry Council on ESD since 2006. During 2015 he became a co-founder of the iT2 Technologies that utilizes software engine for rapid ESD data analysis.

Discussion Groups

Discussion groups are an integral part of the workshop. There will be four discussion groups offered, with two parallel sessions on Monday (3:30PM-5:00PM) and on Wednesday (3:30PM-5:00PM). The topics offered will be the natural continuation of the IEW main themes. Each discussion group has a moderator with extensive expertise on the topic to help guide and inspire the discussion. The success of these sessions depends on your active participation. We encourage you to bring along data, ideas, and other items of interest to share.

DG A.1

EOS versus ESD Robustness

Co-Moderators: tbd

Semiconductor components are designed to withstand appropriate levels of ESD, typically for the Human Body Model (HBM) and the Charged Device Model (CDM). Electrical Over-Stress (EOS), on the other hand, does not have any explicit test method by which one could judge the robustness. Does latch-up testing according to JESD78 ensure some level of EOS robustness? What about transient latch-up? Does a high level of ESD robustness automatically translate to EOS-robust components? Is there any relationship?

DG A.2

40 Year of ESD: Are we Doing Anything Fundamentally Different?

Co-Moderators: tbd

ESD has been a relevant reliability threat for 40+ years. Comparing ESD practices today with that of 1980, have the fundamentals of the problem changed? Are we performing the same analysis but with increasing efficiency and automation? Has there been revolutionary changes in the 40 years or has this been an incremental development process? Do we foresee any revolutionary ideas on the horizon? Come share your perspective on retrospective and forward-looking discussion

DG A.3

Cost of ESD versus Benefit: the perception factor

Co-Moderators: tbd

Technology
scaling has increased the cost of manufacturing semiconductor components to the point that only a few players in the industry can afford to continue down this path. This scaling has produced increasingly fragile devices and integration complexity, requiring significant investments to ensure that ESD levels are met at each node. At the same time, the loading by ESD protection on high-speed data links is increasingly performance-limiting. Are our ESD targets too conservative? Is the roadmap for target-level reduction aggressive enough? How is the industry moving compared to the published target level reduction roadmap? Should more of the emphasis be placed on ESD factory control and less for on-chip protection in order to minimize the cost of semiconductor components?

DG A.4

Challenges of On-Chip Powered ESD Protection in Ultra-Low-Cost Systems

Co-Moderators:
Michi Stockinger, NXP
Raj Sankaralingam, Texas Instruments

The SEED methodology describes how co-designing the IC ESD protection with PCB components can yield cost-efficient system ESD solutions. This discussion group will address the question whether ultra-low-cost systems can truly benefit from the SEED approach, or whether the IC alone could handle the system-level ESD stress without added board components.

Technical Program

The Technical Program consists of three parts:

1. **IEW Technical Poster Sessions**, where posters submitted to IEW are displayed and used as starting point for discussion with the authors
2. **IRPS Platform Session**, where accepted oral papers by IRPS/IEW committee are presented
3. **IRPS Wednesday night Poster Session & Reception**, where all Posters (IRPS + IEW) are displayed in a casual environment, with food and entertainment

IEW Technical Poster Session #1

Monday 1:00PM-3:00PM

Program definition in progress

IEW Technical Poster Session #2

Tuesday 11:10AM-12:40PM

Program definition in progress

IRPS ESD/Latchup Platform Session

Wednesday 12:35PM-3:10PM

6A.1 "How to Achieve Moving Current Filament in High Voltage LDMOS Devices: Physical Insights & Design Guidelines for Self-Protected Concepts", Kranthi Nagothu (1), Sampath Kumar Boeila (1), Chirag Garg (1), Akram Salman (2), Gianluca Boselli (2), Mayank Shrivastava (1) (1. Indian Institute of Science, 2. Texas Instruments)

6A.2 "Over-Voltage Protection on the CC Pin of USB Type-C Interface against Electrical Overstress Events", Chao-Yang Ke, Ming-Dou Ker (Institute of Electronics, National Chiao-Tung University)

6A.3 "Design Insights to Address Low Current ESD Failure and Power Scalability Issues in High Voltage LDMOS-SCR Devices", kranthi Nagothu (1), Sampath Kumar Boeila (1), Gianluca Boselli (2), Akram Salman (2), Mayank Shrivastava (1) (1. Indian Institute of Science, 2. Texas Instruments)

6A.4 "Threshold Voltage Shift in a-Si:H Thin film Transistors under ESD stress Conditions", Rajat Sinha, Prasenjit Bhattacharya, Sanjiv Sambandan, Mayank Shrivastava (Indian Institute of Science)

6A.5 "Sub-nanosecond Reverse Recovery Measurement for ESD Devices", Alex Ayling, Shudong Huang, Elyse Rosenbaum (University of Illinois - Urbana Champaign)

6A.6 "Improved Turn-on Uniformity & Failure Current Density by n- & p-Tap Engineering in Fin Based SCRs", Monishmurali M, Milova Paul, Mayank Shrivastava (Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore, Karnataka, 560012, India)

IRPS Reception and Poster

Wednesday 6:00PM-9:00PM

Program definition in progress

Schedule

Start	End	Sunday
8:30am	12:00pm	Registration
12:00pm	1:30pm	Lunch
1:30pm	3:00pm	Tutorial: Latchup
3:00pm	3:30pm	Break
3:30pm	5:00pm	Tutorial: EOS vs ESD
5:00pm	8:00pm	Group Dinner

Start	End	Monday
8:00am	9:30am	Tutorial: ESD-EMC
9:30am	10:00am	Break
10:00am	11:30am	Tutorial: CDM Verification
11:30am	12:30pm	Lunch
1:00pm	3:00pm	Technical Sessions/Posters I
3:00pm	3:30pm	Break
3:30pm	5:00pm	Discussion Group 1A/B
5:00pm	5:30pm	Break
5:30pm	6:30pm	Seminar: Industry Council Roadmap
6:30pm	9:00pm	Group Dinner

Start	End	Tuesday
8:30am	10:50am	IRPS/IEW Keynote
10:50am	11:10am	Break
11:10am	12:40pm	Technical Session/Posters II
12:40pm	1:40pm	Lunch
1:40pm	9:00pm	Free Time and Group Dinner

Start	End	Wednesday
8:30am	9:30am	Invited Talk: On-Chip HV Transient Design Challenges
9:30am	10:30am	Invited Talk: On-Chip Protection From System-Level Fast Transient Stress Event
10:30am	10:50am	Break
10:50am	11:35am	Keynote
11:35am	12:35pm	Lunch
12:35pm	3:10pm	IRPS ESD/Latchup Technical Session
3:10pm	3:30pm	Break
3:30pm	5:00pm	Discussion Group 2A/B
5:00pm	5:15pm	IEW Closing
6:00pm	9:00pm	IRPS Reception and Posters

Start	End	Thursday
8:00am	1:25pm	IRPS Technical Sessions

IRPS - IEW Bundle Registration Includes: Access to the IRPS Technical Program, Sunday and Monday Tutorials, and Year in Review. Also includes access to food and beverage at all breaks and Wednesday Poster Reception. Additionally, access to the Full IEW Program (IEW Tutorials, Technical Program, Discussion Groups, Social Events).

NOTE: There is no IEW only registration option.

Registration Options

Registration Type	Up to March 1, 2020	After March 1, 2020
IRPS - IEW Bundle – IEEE Member	$1,300	$1,500
IRPS - IEW Bundle – non-IEEE Member	$1,580	$1,780

To complete your registration in several easy steps, please visit http://www.cvent.com/events/2020-ieee-international-reliability-physics-symposium-irps-/event-summary-99311b8bbc554a38ade05acfd966a2c4.aspx to be redirected to a secure partner website, containing information about registration fees and registration options.