2023

US- International Electrostatic Discharge Workshop
March 28 - March 30, 2023

US-IEW

Setting the Global Standards for Static Control!

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The IEW Experience

On behalf of the IEW Management Committee and EOS/ESD Association, Inc., welcome to the 16th annual International ESD Workshop!
IEW is an informal workshop that attracts some of the most recognized experts in the field, by virtue of its unique format: focus is on key themes, which are addressed through a multitude of events, with a strong emphasis on attendees' interaction.

This year's edition is centered around Latchup, Advanced CMOS design challenges, and ESD vs EMC. These topics will be tackled through ad-hoc tutorials, high-profile keynote speakers, and technical sessions.

Additionally, there will be an informal evening program, where the most "hard-core" ESD experts can continue their discussions.

Every attendee has something to share and to learn, and that is why the social aspect is so prevalent. For this reason, as is the IEW tradition, fun will not be forgotten with Tuesday afternoon devoted to a multiple-options social event. This is a great opportunity to get to know your EOS/ESD colleagues better and expand your network.

Furthermore, IEW will be fully embedded into IRPS, with fully synced programs, to maximize events attendance flexibility.

Bottom line: by registering to IEW, you are going to get the best of the IEW and IRPS worlds.

We are looking forward to meeting you all in Monterey!

IEW Keynote

Tuesday 10:40-11:30 AM

High-performance electronics using wide bandgap technology

Prof. Srabanti Chowdhury, Stanford University

We live in a very exciting time where the world is championing electrification at every level. We are witnessing the most significant transformation of transportation since the internal combustion engine. Smart devices, including appliances, equipment, and machinery, supported by the IoT, are becoming more intelligent and affordable. Robotics and autonomous vehicles promise to transform our lifestyles. Among all these new waves of technology, the idea of achieving a carbon-free energy system by 2050 is now more than a commitment and requires energy efficient electronics at every level.

Wide-bandgap (WBG) semiconductors present a pathway to enable much of these electronics with higher frequencies, higher power densities, and at higher temperatures, enabling newer functionalities. WBG devices with higher power density have unprecedented value in both power and high frequency electronics. The roadmap looks promising if GaN and other WBGs can be successfully integrated into circuit boards to drive applications. However so far, GaN transistors have not been a plug-n-play experience. To extract the anticipated efficiencies from a WBG driven system, sometimes the power module needed a change, while at other times, the whole circuit topology had to be re-invented. Under those operating conditions, where WBG devices perform their best, parasitic devices in integrated circuits can risk the desired function of a component. Latch-up and electrostatic discharge (ESD), among other high field phenomena (avalanche), and their roles in circuit design are therefore critical to understand and deliver the functional security of the system, even under extreme operating and environmental conditions. The success of gallium nitride has opened the door to other ultra-wide bandgap materials (e.g., Diamond, Aluminum Nitride and Gallium Oxide), presenting new area of research covering a wide spectrum from materials, physics, devices, and applications.

Prof. Srabanti Chowdhury is the Willard and Inez Kerr Bell Faculty Scholar associate professor of Electrical Engineering (EE) at Stanford and materials Science and Engineering (by courtesy). She is a senior fellow at the Precourt Institute of Energy at Stanford. Her research focuses on wideband gap (WBG) and ultra-wide bandgap (UWBG) materials and device engineering for energy efficient and compact system architecture for power electronics, and RF applications. Besides Gallium Nitride, her group is exploring Diamond for various active, and passive electronic applications, particularly thermal management. She received her M.S and PhD in Electrical Engineering from University of California, Santa Barbara.

She received several early career awards including DARPA Young Faculty Award, NSF CAREER and AFOSR Young Investigator Program (YIP) in 2015. In 2016 she received the Young Scientist award at the International Symposium on Compound Semiconductors (ISCS). She is a senior member of IEEE and alumni of NAE Frontiers of Engineering.

She received the Alfred P. Sloan fellowship in Physics in 2020. To date, her work has produced over 6 book chapters, 100 journal papers, 110 conference presentations, and 26 issued patents. She serves the program committee of several IEEE conferences including IRPS and VLSI Symposium, and the executive committee of IEDM.

IEW Keynote

Tuesday 11:30-12:20 PM

A Roadmap for Disruptive Applications and Heterogeneous Integration Using Two-Dimensional Materials: State-of-the-Art and Technological Challenges *Prof. Mayank Shrivastava, Indian Institute of Science, Bangalore, India*

This talk will attempt to establish a roadmap for 2-Dimensional (2D) material-based Nanoelectronic technologies for beyond Si and other future/disruptive applications with a vision for the semiconductor industry to enable a universal technology platform for heterogeneous integration. The heterogeneous integration would involve integrating orthogonal capabilities such as different forms of computing (classical, neuromorphic and quantum), all forms of sensing, digital and analog memories, energy harvesting, etc. – all in a single chip using a universal technology platform. This talk will also cover the technological and fundamental challenges in pushing the 2D technology to the market, where the world stands today, and what gaps are required to be filled. Talking about the gaps, I will particularly touch base on the Metal (3D) to graphene/TMD (2D) contact engineering challenges, which has been considered as one of the most fundamental challenges towards harnessing the full potential of 2-dimensional materials. And, how the fundamental understanding of the contact's quantum chemistry resulted in unique ways to engineer it, resulting into record transistor performance. Besides, I will talk about some of the fundamental process challenges which can unintentionally perturb the 2D channel's electrical, optical and mechanical properties. In the end, I will talk about some of the reliability gaps, which are urgently required to be addressed and the fundamental understanding we have developed so far.

Prof. Mayank Shrivastava is a faculty member at the Indian Institute of Science, Bangalore, and co-founder of AGNIT Semiconductors Pvt. Ltd. He is also instrumental in setting up a 300 Crore worth GaN prototyping Fab and leading a national effort on 2D material's technology hub. He received his Ph.D. degree from the Indian Institute of Technology Bombay (2010). For his Ph.D. work, he received Excellence in Research award and the Industrial Impact award from IIT Bombay in 2010. He is among the first recipients of the Indian section of the American TR35 award (2010) and the first Indian to receive IEEE EDS Early Career Award (2015). He is also an Editor of IEEE Transactions on Electron

Devices. Besides, he is an IEEE Electron Device's Society (EDS) Distinguished Lecturer and an elected member of the IEEE EDS Board of Governors. He is the recipient of the prestigious DST Swarnjayanti Fellowship (2021), Abdul Kalam Technology Innovation National Fellowship from INAE-SERB (2021), and the VASVIK award (2021). He has received several other national awards and honors of high repute, like the National Academy of Sciences, India, (NASI) Young Scientist Platinum Jubilee Award – 2018; Indian National Academy of Science (INSA) Young Scientist Award - 2018; Indian National Academy of Engineering (INAE) Innovator Entrepreneur Award 2018 (Special commendation); Indian National Academy of Engineering (INAE) Young Engineer Award - 2017; INAE Young Associate (since 2017); Indian Academy of Sciences (IASc), Young Associate, 2018 – 2023; Ministry of Electronics & Information Technology (MeitY), Young Faculty Fellowship. Besides, he received best paper awards from several international conferences like Intel Corporation Asia academic forum, VLSI design Conference and EOSESD Symposium. Prof Shrivastava broadly works on applications of emerging materials like Gallium Nitride (GaN), atomically thin two-dimensional materials like Graphene and TMDCs, in electronic and electro-optic devices working closer to its fundamental limits (like the ability to handle extreme powers, ability to work at THz like ultra-high frequencies, or ability to compute information in unconventional ways). Currently, his group is developing few-atom thick devices & circuits, GaN-based ultra-high-power devices with high reliability, and devices/circuits for operation at THz frequencies. Besides, his group also works on developing novel ESD and High Voltage device concepts in advanced CMOS nodes. He held visiting positions in Infineon Technologies, Munich, Germany, from April 2008 to October 2008 and again from May 2010 to July 2010. He worked for Infineon Technologies, East Fishkill, NY, USA; IBM Microelectronics, Burlington, VT, USA; Intel Mobile Communications, Hopewell Junction, NY, USA; Intel Corp, Mobile and Communications Group, Munich, Germany between 2010 and 2013. He joined the Indian Institute of Science as a faculty member in the year 2013. Prof Shrivastava's work has resulted in over 190 peer-reviewed publications (47 of these papers are in IRPS and IEDM, the two most prestigious conferences of IEEE EDS, and around 100 are in journals such as IEEE T-ED) and 47 patents. Most of these patents are either licensed by semiconductor companies or are in use in their products.

Seminary/Workshop #1

Wed. 10:55 – 12:35 PM

ESD for High-Speed IO Circuits
Presenter: Glasney Asada, AMD

High speed IO (input / output) circuits need to minimize capacitance on signal bumps to achieve their desired performance targets. ESD protection is needed to prevent damage to these circuits during handling or assembly. There are several techniques that attempt to solve these mostly mutually exclusive problems. This seminar presents the solution space from the perspective of the high-speed IO designer.

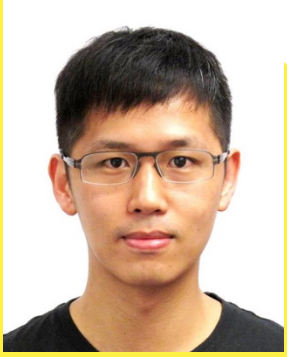
Glasney Asada received his B.S. in Electrical Engineering from the University of California at Los Angeles in 1997. He initially started working on high-speed wireline SerDes at Agilent Technologies in 2000. In 2003, Gladney joined AMD and became the technical lead for high-speed receivers such as Hypertransport, PCIE, SATA, USB, and Display Port. He was also the GDDR transmitter owner for one technology node. In 2014, Gladney became the overall ESD design owner for all AMD products. He leads the team that oversees the implementation of circuit topologies to guarantee that AMD solutions meet customer ESD manufacturing requirements and achieve the IO speed targets.

Seminary/Workshop #2

Wed. 1:45 – 3:20 PM

Advanced FinFET ESD Design Challenges
Presenter: Wun-Jie Lin, TSMC

ESD design becomes more challenging as technologies advance. While novel device structures such as FinFET's and Nanosheet have better gate-control, those devices feature lower junction and GOX breakdowns, which restrict the ESD design window, making in turn ESD device development even more challenging.
In this presentation, we introduce the ESD design challenges in advanced technologies, and then demonstrate ESD device optimization including rotated ESD diodes with low-capacitance BEOL, snapback-ESD and low-capacitance SCR, that provides competitive ESD devices for ESD network design.



Wun-Jie Lin received the B.S. degree from the Department of Engineering and System Science, Tung-Hai University, Taiwan, in 2008, and the M.S. degree from the Department of Electronics Engineering, National Tsing-Hua University, Taiwan, in 2010. He joined Taiwan Semiconductor Manufacturing Company (TSMC) in 2010 as an Engineer worked on ESD/EOS solution in advanced technologies and in 2019 as a Manager of ESD/EOS Device Technology Section.

Seminary/Workshop #3

Wed. 3:25 – 5:40 PM

Do you really know how to do JESD78 latch-up testing? Preview our new user guide

Presenter: Marty Johnson, Texas Instruments (ret)

Over time, the JESD78 latch-up test standard has grown in size and complexity to address a variety of real-life challenges. A proper interpretation and execution of the test standard has become difficult. A recent survey on latch-up testing practices and recommendations for improvements, which was performed by the Industry Council on ESD Target Levels and summarized in JEDEC publication JEP193, has highlighted the need for a latch-up testing user guide with practical explanations, hints, and examples. The JESD78 working group has taken up this task and created an outline of the user guide. This seminar will preview the various user guide topics with the hope to receive valuable feedback from the audience that will help to further improve the user guide.

Martin (Marty) Johnson received his B.S. Physics from Midland Lutheran College now Midland University (Fremont, Nebraska) in 1973, his M.S. Physics from the University of Tennessee Space Institute (Tullahoma) in 1975 and his M.S. in Electrical Engineering from the University of Nebraska (Lincoln) in 1978. He worked at National Semiconductor from 1978 to 2001, Philips Electronics from 2001 to 2006 and returned to National Semiconductor in 2006 which is now part of Texas Instruments (2011). He retired from Texas Instruments in May 2019. His interests have spanned the semiconductor reliability spectrum from basic reliability qualification through wafer level reliability to ESD and Latch-up. He last worked in the Semiconductor Reliability Services Group in Santa Clara, California and was the corporate Subject Matter Expert (SME) for Latch-up. He is also active on the ESDA/JEDEC Joint HBM & CDM standards teams and the JEDEC Latch-up standard team. He’s co-authored papers in package-level reliability, wafer-level reliability, ESD and Latch-up.

Seminar/Workshop #4

Thu. 9:15 – 10:50 AM

Transient Absolute Maximum Ratings (AMR) – The missing link between customer and supplier

Presenter: Andrea Boroni, STMicroelectronics

White Paper number 4 of Industry Council on ESD Target Level gave a clear definition of absolute maximum ratings (AMR) as the dividing line between allowed operation and the realm of electrical overstress, which has to be fully acknowledged by system design since its first publication more than five years ago. The Industry Council Working Group is working on extending the specification of transient stress to transient AMR as a generalized approach other than a limit number of specific standardized stress tests. Clear definition of Transient AMR (tAMR), real world examples and proposal of a new method to describe the safe operating area profile of tAMR will be discussed.

Andrea Boroni received the degree in electronic engineering from Politecnico di Milano, Milan, Italy, in 2004 with a thesis on “Apparatus development for trapping level characterization in PN junction”. After two years of research developing SPAD characterization equipment, he joined the R&D Equipment Development Team for Product Validation and ESD Qualification in STMicroelectronics. He led the ESD Qualification Team for few years and currently he is responsible for ESD, Metrology and Reliability laboratories in STMicroelectronics in Agrate.

Seminar/Workshop #5

Thu. 1:40 – 4:20 PM

Automotive On-Chip System-Level Design Challenges
Presenter: Gianluca Boselli, Texas Instruments

The trend towards society's "smart-electrification" is driving the need for ESD immunity at system-level. IEC 61000-4-2 defines how to perform the Electrostatic discharge immunity test at system level. To protect against these events, until fifteen years ago, ad-hoc ESD protections (TVS – Transient Voltage Suppressors) were implemented at board/system-level in proximity of the connectors interfacing with the "external world". However, a new trend of implementing system-level robustness at component-level is quickly becoming standard practice, mainly stemming from the desire to reduce system/board design cost. While on paper this may sound as a logical step, it poses enormous challenges to the component ESD Designer. In the automotive world, situation is even more challenging. In addition to ESD immunity at system-level, there is a plethora of other requirements against immunity to Electrical Disturbances and immunity to RF disturbances that must be met. This Seminar will review all the aforementioned challenges and will propose solutions to tackle them.

Dr. Gianluca Boselli (Master in EE at the University of Parma-Italy, 1996, PhD at the University of Twente-The Netherlands, 2001) is with Texas Instruments, Inc., Dallas, Texas, since 2001. He is currently the manager of the corporate ESD Team. He authored many papers about ESD and latch-up, which were presented at major conferences/journals. Dr. Boselli has been the first recipient of multiple best paper awards on behalf of Microelectronics Reliability Journal and EOS/ESD Symposium. He served multiple times as sub-committee chair for technical program committees (TPC) of EOS/ESD Symposium, IEDM, IRPS, IEW, and ESREF. Dr. Boselli has served as TPC chair at the EOS/ESD Symposium 2006, vice-general chair at the EOS/ESD Symposium 2007, and general chair at the EOS/ESD Symposium 2008. He is currently a member of the board of directors of EOS/ESD Association, where he served as President in 2018-2019. He is the recipient of the ESDA Outstanding Contribution Award. Dr. Boselli is an IEEE senior member and holds over thirty patents with several pending. Dr. Boselli serves in the editorial board of the IEEE Transactions on Device and Materials Reliability (T-DMR).

IRPS + IEW Poster Session

Thu. 10:55 – 12:55 PM

1. **Multi-finger Turn-on: A potential cause of premature failure in Drain Extended HV Nanosheet Devices,** Jatin Jatin, Monishmurali M, Mayank Shrivastava, IISc, Bangalore, India
2. **Extremely Large Breakdown to Snapback Voltage Offset (Vt1>>VBD): Another Way to Improve ESD Resilience of LDMOS Devices**, Aakanksha Mishra, B. Sampath Kumar, Monishmurali M, Shaik Ahamed Suzaad, Shubham Kumar, Kiran Pote Sanjay, Amit Kumar Singh, Ankur Gupta, Mayank Shrivastava, Indian Institute of Technology Delhi/ Indian Institute of Science Bangalore/Semiconductor Laboratory Mohali
3. **Current Scalability Issues in Multi-Bank 5V PMOS ESD structures: Root cause and Design Guidelines**, Kranthi Nagothu, Yang Xiu, Yang Xiao, Raj Sankaralingam, Texas Instruments
4. **Engineering Custom TLP I-V Characteristic Using a SCR-Diode Series ESD Protection Concept**, Harsha B Variar, Satendra Kumar Gautam, Ashita Kumar, Amogh K M, Juan Luo, Ning Shi, David Marreiro, Shekar Mallikarjunaswamy, Mayank Shrivastava, Indian Institute of Science Bangalore/ Alpha and Omega Semiconductor
5. **3D Approaches to Engineer Holding Voltage of SCR**, Satendra Kumar Gautam, Harsha B Variar, Juan Luo, Ning Shi, David Marreiro, Shekar Mallikarjunaswamy, Mayank Shrivastava, Indian Institute of Science Bangalore/ Alpha and Omega Semiconductor
6. **Current Injection Effect on ESD Behaviors of the Parasitic Bipolar Transistors inside P+/N-well diode**, Hui Wang, Pengyu Lai, Zhong Chen, University of Arkansas
7. **TCAD study of the Holding-Voltage Modulation in Irradiated SCR-LDMOS for HV ESD Protection**, Laura Zunarelli, Luigi Balestra, Susanna Reggiani, Raj Sankaralingam, Mariano Dissegna, Gianluca Boselli, University of Bologna/Texas Instruments
8. **Role of LDD on the Current Filamentation behavior in ggNMOS**, Monishmurali M, N K Kranthi, Raj Sankaralingam, Gianluca Boselli and Mayank Shrivastava, IISc Bangalore/Texas Instruments
9. **Case Study of Non-permanent Failure in High-Speed Interface IP during Component CDM Test**, Sukjin Kim, Mijin Lee, Woojin Seo, Eonguk Kim, and Chanhee Jeon, Samsung Electronics
10. **Multiphysics Simulation of Non-contact ESD in Electronic Devices**, Tim McDonald and Kevin Merenda, Electro Magnetic Applications, Inc

IEW Schedule

Start	End	Tuesday
8:00am	10:15am	IRPS Welcome and Keynotes
10:15am	10:35am	Break
10:35am	12:20pm	IEW Keynotes
12:00pm	1:40pm	Lunch
1:40pm	6:00pm	Outdoor Networking Activities

Start	End	Wednesday
8:00am	8:50am	IRPS Keynote
8:50am	9:10am	Break
9:10am	10:30am	IRPS EL Session
10:30am	10:50am	Break
10:50am	12:35pm	Seminar/Workshop #1: High-speed I/O design
12:00pm	1:40pm	Lunch
1:40pm	3:20pm	Seminar/Workshop #2: FinFET ESD Design
3:25pm	5:40pm	Seminar/Workshop #3: JESD78 LU User guide updates
6:00pm	9:00pm	IRPS Reception and Posters

Start	End	Thursday
8:00am	8:50am	IRPS Keynote
8:50am	9:10am	Break
9:10am	10:30am	Seminar/Workshop #4: Transient AMR
10:55am	12:35pm	IEW+IRPS Poster session
12:00pm	1:40pm	Lunch
1:40pm	4:00pm	Seminar/Workshop #5: Automotive System-Level ESD Design