IEEE Advancing Technology for Humanity

7th ICEE 2025 IEEE

7th International Conference on Emerging Electronics (ICEE 2025)

December 13 - 16, 2025, Hilton Bengaluru Embassy Manyata Business Park

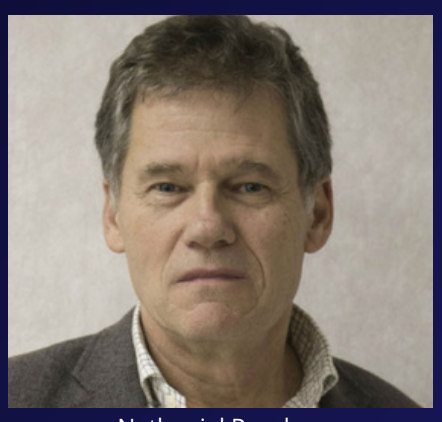
ESD Devices and Circuits at ICEE 2025

Tutorial – 13 December 2025 (Saturday)

Tutorial 6:

On-Chip ESD Design: From Device Physics to Practical Application

Time: 02:00 PM – 05:30 PM



Nathaniel Peachey
President for EOS/ESD Association, Inc,
Sr. Eng. Manager, Qorvo, USA

Souvick Mitra
International Partner Chair for EOS/ESD Association, Inc,
Micron Technology, USA

Invited Talks - 15th December 2025 (Monday)

Session 1: ESD Design

11:40-12:05 PM : Unified ESD Protection Methodologies for Heterogeneous 3.5D Integration

Abhijat Goyal; Marvell Technology, USA

12:05-12:30PM : 3D Heterogenous Integration and Advanced Packaging: ESD Challenges

Nathaniel Peachey; President for EOS/ESD Association, Inc,
Sr. Eng. Manager, Qorvo, USA

Session 2: ESD EDA & System Design

02:00–02:25 PM : ESD Electronic Design Automation Challenges - New Revision of ESDA Technical Report ESD TR18.0-01

Subhadeep Ghosh; Texas Instruments, India

02:25–02:50 PM : From Complexity to Confidence: Comprehensive ESD Signoff for 3DICs

Vinayakam Subramaniam; Ansys, India

02:50–03:15 PM : SoC ESD Design and Verification - Trend and Challenges

Nitesh Trivedi; Intel, India

03:15–03:40PM : Improving the fidelity of ESD margins with context-aware ESD simulation

Sreekumar Kuriyedath; Siemens EDA, USA

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Oral Presentations

- **NIPIN Diode with Designable Asymmetry for Low Voltage and Low Capacitance System Level ESD Protection [P_162]**
  Navin Maheshwari, Krish Patel, Kshitij Agarwal, Hasan Ali, Ritesh Kumar and Sandip Lashkare; IIT Gandhinagar
- **Managing higher ESD CDM target using optimized I/Os [P_341]**
  Bhawana Adhikari, Hemant Ahire, Siddharth Singh and Anurag Mittal ; Synopsys
- **A Modified RC and Delay based ESD Clamp Circuit with False-trigger Immunity during normal supply operation [P_210]**
  Naresh Kumar, Divya Agarwal and Rajesh Narwal ; ST Microelectronics
- **Analysis and Solution to Slew-Rate-Detection NAND ESD Clamp Failure in RF Front-End Module [P_6]**
  Jian Liu, Nathaniel Peachey, Calvin Weichert and Jeffrey Zhijian Yang ; Qorvo Inc.
- **Analyzing the Low-Capacitance ESD Diode for System-level ESD Protection of High-Speed Interfaces [P_192]**
  G Yashan Kumar, Gosike Raviteja, Sachin Kumar and Sandip Lashkare; IIT Gandhinagar

Poster Presentations

- **Optimizing Well Tap Placement in CMOS for Latch-Up Immunity: A TCAD Perspective [P_108]**
  Pallabi Das, James Davis and Radhakrishnan Sithanandam ; Micron Technology
- **TCAD-Guided Design of a Compact ESD Protection Circuit for Neurostimulators in CMOS 65nm Technology [P_149]**
  Navin Maheshwari, Tanay Das, Siddhesh Kadam, Laxmeesha Somappa and Sandip Lashkare ; IIT Gandhinagar, IIT Bombay
- **Verification of ESD Protection Network Robustness on Optimized Design Database for SoC in TSMC Technology [P_151]**
  Aditya Poal and Nitesh Trivedi ; Intel
- **Area Efficient Latch-up prevention layout design technique for Fail-safe or cross supply domain IOs [P_185]**
  Meenakshi Didharia and Sarath Lal K P ; Synopsys
- **Early PERC Signoff through IO Integration Rules [P_216]**
  Annu Kumari, Avinash Gupta and Anurag Mittal; Synopsys
- **Best Practices with AI-Assisted Robust Analog Layout for Mixed-Signal ICs with ESD Protection [P_240]**
  Amitabh Jain, Prateek Asthana, Krishna Thakur and Deependra Jain; LTSCT
- **Design of ESD Protection with on-chip diodes for 65nm CMOS High Voltage Neurostimulators [P_357]**
  Tanay Das, Laxmeesha Somappa and Sandip Lashkare; IIT Gandhinagar, IIT Bombay

ESD Devices and Circuits Track

Track Chairs/Co-Chair

Radhakrishnan Sithanandam
Micron Technology

Sandip Lashkare
IIT Gandhinagar

Committee Members

- ***Souvick Mitra;*** *Micron, USA*
- ***Michael Khazhinsky;*** *SiLabs, USA*
- ***Kranthi Nagothu;*** *TI, India*
- ***Dattatreya Prabhu Rachakonda;*** *GlobalFoundries, India*
- ***Harshit Dhakad;*** *Intel, India*

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