EOS/ESD Association, Inc.
Asia Online Forum
Circuit Design Engineers Certification (ECEC 1)

Virtual Event November 9–10, 2026

Cost $680 USD • Certification online $250 USD

Discounted Price with a savings of over $1,100 USD!

DON'T miss it!

The EOS/ESD Association's ESD for Circuit Design Engineers Certification provides the circuit design engineer with the knowledge and the skills to implement ESD protection circuits and latch-up mitigation on their integrated circuit (IC) designs using industry-proven best practices.

Learning Objectives:

Upon completion of this training, engineers will be able to:

- Understand basic ESD circuits and how to implement them successfully into their product designs.
- Knowledge of basic ESD physics and how this can impact other circuit components.

Target Audience:

Circuit designers who implement ESD circuits into the product padrings and architecture.

Unlock the expertise that sets top circuit designers apart with the EOS/ESD Association's ESD for Circuit Design Engineers Certification. This industry-recognized program gives you the practical skills to design stronger, more reliable ICs by mastering proven ESD protection and latch-up mitigation techniques. From essential ESD circuits to the physics that drive them, you'll learn how to build smarter padrings and architectures that reduce failures and speed up development. Elevate your credibility, boost your team's confidence in your designs, and stand out in the semiconductor industry with a certification backed by the world's leading authority in ESD.

- **Elevate your IC design expertise with the industry's most trusted certification in ESD protection and latch-up mitigation.**

Gain the knowledge top semiconductor companies expect from today's circuit design engineers.

- **Master the essential ESD protection circuits every high-reliability product depends on.**

Learn to implement robust protection structures that safeguard performance, reduce field failures, and improve product longevity.

- **Build confidence in your ability to design ESD-safe padrings and architectures using proven, standards-aligned techniques.**

Develop skills grounded in real-world best practices recognized across the electronics industry.

- **Understand the physics behind ESD—and how it impacts critical circuit behavior.**

Move beyond "cookbook" design and make informed engineering decisions that prevent unintended interactions within your IC.

- **Reduce costly design iterations by getting ESD protection right the first time.**

Apply techniques that minimize rework, shorten development cycles, and help avoid expensive qualification failures.

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• **Stand out in a competitive engineering field with a credential backed by the EOS/ESD Association, the global authority on ESD.**
Show employers and teams that you bring certified, specialized expertise to every project.

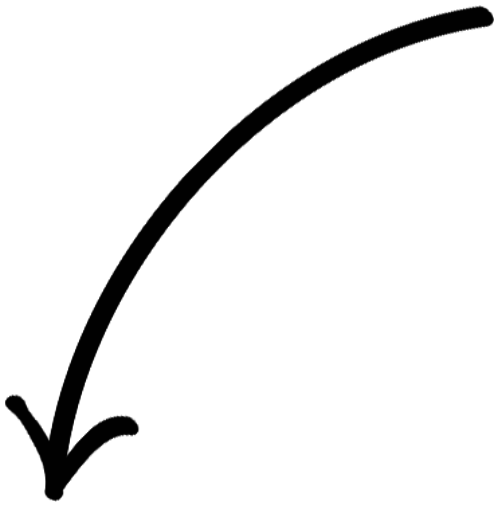
• **Strengthen collaboration across design, reliability, and verification teams.**
Speak the shared language of ESD design requirements, enabling smoother reviews, clearer communication, and higher-quality outcomes.

• **Designed specifically for circuit designers integrating ESD into product padrings and overall IC architectures.**
Training that is practical, focused, and directly applicable to day-to-day design responsibilities.

Event Times Both Days:

Timezone	Start Time	End Time
India (IST)	11:00–11:05 AM	4:10–4:25 PM
Vietnam/Thailand (ICT)	12:30–12:35 PM	5:40–5:55 PM
Singapore/China/TPaiwan/H/MY (SGT/CST/PST/MYT)	1:30–1:35 PM	6:40–6:55 PM
Eastern USA (EST)	12:30–1:35 AM	5:40–5:55 AM

Detailed Agenda on Next Page



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Detailed Agenda — Day 1: November 9, 2026

Session	India (IST)	Vietnam/ Thailand (ICT)	Singapore/ China/ Taiwan/ PH/ MY (SGT/ CST/PST/MYT)	Eastern USA (EST)	Description
Welcome & Opening	11:00–11:05 AM	12:30–12:35 PM	1:30–1:35 PM	12:30–12:35 AM	Brief introduction and overview
Session 1 (45 min)	11:05–11:50 AM	12:35–1:20 PM	1:35–2:20 PM	12:35–1:20 AM	Background of ESD Basics and Models
Q&A 1 (10 min)	11:50–12:00 PM	1:20–1:30 PM	2:20–2:30 PM	1:20–1:30 AM	Question and answer session
Session 2 (45 min)	12:00–12:45 PM	1:30–2:15 PM	2:30–3:15 PM	1:30–2:15 AM	ESD Factory Basics for Design Engineers
Q&A 2 (10 min)	12:45–12:55 PM	2:15–2:25 PM	3:15–3:25 PM	2:15–2:25 AM	Question and answer session
Open Discussion Breakout 1 (15 min)	12:55–1:10 PM	2:25–2:40 PM	3:25–3:40 PM	2:25–2:40 AM	Interactive breakout
Full Break (15 min)	*1:10–1:25 PM*	*2:40–2:55 PM*	*3:40–3:55 PM*	*2:40–2:55 AM*	*Standard rest and refresh break*
Session 3 (45 min)	1:25–2:10 PM	2:55–3:40 PM	3:55–4:40 PM	2:55–3:40 AM	ESD System Level Basics
Q&A 3 (10 min)	2:10–2:20 PM	3:40–3:50 PM	4:40–4:50 PM	3:40–3:50 AM	Question and answer session
Session 4 (45 min)	2:20–3:05 PM	3:50–4:35 PM	4:50–5:35 PM	3:50–4:35 AM	ESD EDA Verification Tools
Q&A 4 (10 min)	3:05–3:15 PM	4:35–4:45 PM	5:35–5:45 PM	4:35–4:45 AM	Question and answer session
Session 5 (45 min)	3:15–4:00 PM	4:45–5:30 PM	5:45–6:30 PM	4:45–5:30 AM	ESD Compact Models and Simulation
Q&A 5 (10 min)	4:00–4:10 PM	5:30–5:40 PM	6:30–6:40 PM	5:30–5:40 AM	Question and answer session
Open Discussion Breakout 2 (15 min)	4:10–4:25 PM	5:40–5:55 PM	6:40–6:55 PM	5:40–5:55 AM	Final interactive discussion and reflections

Day 2 on next page

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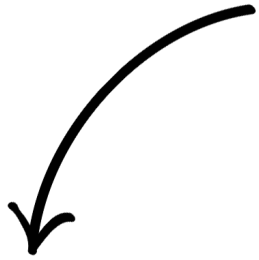
Detailed Agenda — Day 2: November 10, 2026

Session	India (IST)	Vietnam/ Thailand (ICT)	Singapore/China/PH/ Taiwan/ MY (SGT/ CST/PST/MYT)	Eastern USA (EST)	Description
Welcome & Opening	11:00–11:05 AM	12:30–12:35 PM	1:30–1:35 PM	12:30–12:35 AM	Brief introduction and overview
Session 1 (45 min)	11:05–11:50 AM	12:35–1:20 PM	1:35–2:20 PM	12:35–1:20 AM	Basics of ESD and Latch-up Device Physics
Q&A 1 (10 min)	11:50–12:00 PM	1:20–1:30 PM	2:20–2:30 PM	1:20–1:30 AM	Question and answer session
Session 2 (45 min)	12:00–12:45 PM	1:30–2:15 PM	2:30–3:15 PM	1:30–2:15 AM	ESD Circuit-Chip Design Implementation (with Layout Principles) CMOS
Q&A 2 (10 min)	12:45–12:55 PM	2:15–2:25 PM	3:15–3:25 PM	2:15–2:25 AM	Question and answer session
Open Discussion Breakout 1 (15 min)	12:55–1:10 PM	2:25–2:40 PM	3:25–3:40 PM	2:25–2:40 AM	Interactive breakout
Full Break (15 min)	*1:10–1:25 PM*	*2:40–2:55 PM*	*3:40–3:55 PM*	*2:40–2:55 AM*	*Standard rest and refresh break*
Session 3 (45 min)	1:25–2:10 PM	2:55–3:40 PM	3:55–4:40 PM	2:55–3:40 AM	ESD Circuit-Chip Design Implementation (with Layout Principles) Mixed-Signal High-Voltage
Q&A 3 (10 min)	2:10–2:20 PM	3:40–3:50 PM	4:40–4:50 PM	3:40–3:50 AM	Question and answer session
Session 4 (45 min)	2:20–3:05 PM	3:50–4:35 PM	4:50–5:35 PM	3:50–4:35 AM	ESD Latch-up Product Testing Basics
Q&A 4 (10 min)	3:05–3:15 PM	4:35–4:45 PM	5:35–5:45 PM	4:35–4:45 AM	Question and answer session
Session 5 (45 min)	3:15–4:00 PM	4:45–5:30 PM	5:45–6:30 PM	4:45–5:30 AM	ESD Latchup Failures Troubleshooting Techniques and Case Studies
Q&A 5 (10 min)	4:00–4:10 PM	5:30–5:40 PM	6:30–6:40 PM	5:30–5:40 AM	Question and answer session
Open Discussion Breakout 2 (15 min)	4:10–4:25 PM	5:40–5:55 PM	6:40–6:55 PM	5:40–5:55 AM	Final interactive discussion and reflections

Course descriptions



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Course Descriptions

Background of ESD Basics and Models — *John Kinnear*

This class introduces the basics of ESD: what it is, why it is a problem, and how to test for it. A basic overview of CDM, HBM, HMM, TLP, and system ESD test methods is also presented.

Basics of ESD and Latch-up Device Physics — *Gianluca Boselli*

The primary goal of this class is to determine the ESD Design/Operation window, i.e. the electrical boundary within which an ESD protection will meet both functional and ESD requirements. Relevant electrical parameters leading to the ESD Design Window are specified and reviewed for any class of components. Latch-up basics is also covered.

ESD Circuit-Chip Design Implementation (with Layout Principles): CMOS — *Gianluca Boselli*

This class first provides an overview of prevalent ESD failure modes and the available ESD protection building blocks including diodes and transient-triggered active MOSFET clamps. The concept of an "ideal ESD clamp" is described from the perspective of an IC's operating and failure voltage levels and the expected ESD current level. The next section discusses application scenarios for IO pad protection, distinguishing between rail-based and pad-based protection methods, and showing how the protected circuitry may participate in an ESD event. Preferred rail clamp and busing schemes for IO pad banks, including embedded analog pad domains, are introduced. The CDM response of an IO pad is used as an example for performing ESD network simulations. The concepts of secondary input protection and cross-domain CDM protection are described. The class continues with discussing the potential IC performance impact of added ESD devices and how to minimize it — a GHz LNA receiver is used as an example. The final section describes potential pitfalls of ESD designs and how to avoid them systematically.

ESD Circuit/Chip Design Implementation (with Layout Principles): Mixed-Signal/High-Voltage — *Gianluca Boselli*

The primary goal of this class is to review and provide the fundamental design notions of the ESD protection solutions that will satisfy the ESD Design Window to meet both functional and ESD requirements.

ESD EDA Verification Tools — *Michael Khazhinsky*

The verification of ESD protection networks in modern integrated circuits is a difficult challenge due to increasing design and process complexity, higher pin counts, and the overall computational difficulties in dealing with large data sets. Most chips today are segmented into multiple power domains, where ESD currents must necessarily be shunted from one domain to another, across multiple-layer interconnect paths that span major portions of the chip. Furthermore, circuit blocks that are traditionally not associated with the I/O ring — and which may be far from the I/O circuits themselves — may become damaged as a result of the high voltages and currents produced during an ESD discharge. Relying on manual verification alone poses a significant risk of missing hidden ESD pitfalls; consequently, automated ESD and latch-up rule checking is highly desired. This tutorial outlines the essential requirements of the ESD EDA verification flow, as discussed in ESDA Technical Report TR18.0-01-14, gives an overview of existing ESD EDA solutions across industry (both commercial and in-house), and discusses directions for future ESD EDA tool development.

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ESD Compact Models and Simulation — *Michael Khazhinsky*

Make designers aware of ESD-specific SPICE simulation tasks, including simulation test benches, setup, and model limitations. Aligned with ESDA WG18 recommendations.

ESD/Latch-up Product Testing Basics — *Robert Gauthier*

This course will present a basic overview of ESD/latch-up product testing and debug. Background on the test models/methods, inputs needed for the test lab for job submissions, and some common pitfalls will be reviewed.

ESD/Latch-up Failures: Troubleshooting Techniques and Case Studies — *Robert Gauthier*

This course will give a basic overview of the possible failure analysis techniques to utilize on a product when an ESD or latch-up failure or improvement to the product is needed. A high-level overview of the different types of failure analysis — and which one is typically best for which failure — will be reviewed.

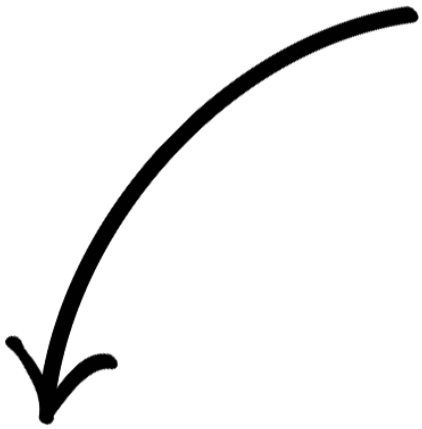
ESD Factory Control Basics — *John Kinnear*

This course will provide the design engineer with the basic understanding of ESD control for safe handling of ESD-sensitive devices. It will give the rationale for the engineer to implement ESD-safe handling practices and controls in the engineering characterization lab.

ESD System Level Basics — *John Kinnear*

Based on the understanding of the interaction between board and IC level protection — also using SEED simulations — the circuit designer will be able to optimize the on-chip protection for interfaces exposed to residual stress of system-level ESD.

Instructor biographies



Instructor Biographies

Gianluca Boselli, Ph.D.

Dr. Boselli completed his Ph.D. at the University of Twente, The Netherlands, in 2001 and joined Texas Instruments, Inc., Dallas, Texas, where he focused on ESD and latch-up development for advanced CMOS technologies. He is currently managing the corporate ESD Team and is the Director of Advanced Technology Development University Research Program. He has authored several papers in the area of ESD and latch-up and was the recipient of the best paper award on behalf of Microelectronics Reliability Journal in 2000. He received the best paper award at the EOS/ESD Symposium 2002, and the Outstanding Symposium award at the EOS/ESD Symposium in 2002, 2006, and 2010. In 2019 he was the recipient of the Outstanding Contribution Award, the most prestigious award granted by ESD Association. Dr. Boselli is an IEEE senior member and holds over twenty patents with several pending.

John T. Kinnear, Jr.

John graduated from the University of Buffalo with a B.S. in Electrical Engineering and a Master's in Electrical Engineering from Syracuse University. He was hired by IBM, where he worked for 46 years. As part of his role, John was the Subject Matter Expert in ESD control for IBM, including developing and implementing ESD control processes at all IBM manufacturing sites and assessing IBM's suppliers for ESD control. The processes spanned wafer fab through to large servers, with all the processes required in between.

John has been a part of the ESD Association for over 30 years. He is currently chair of Working Group 20, which is responsible for ANSI/ESD S20.20, Development of an Electrostatic Discharge Control Program. John is also a member of various other standards working groups and is a founding member of the Technical Advisory Support Committee (TAS), which oversees all the ESD Association standards. He is the chair of the International Electrotechnical Commission (IEC) Technical Committee 101 on electrostatics and is the project leader for IEC 61340-5-1 — Electrostatic Discharge Control Program. Before becoming chair, John was the chief delegate for the United States.

Robert Gauthier

Robert joined IBM in Essex Junction, Vermont in 1995, where he focused on device design and TCAD simulations designing devices in 0.35 µm technologies. In 1998 he expanded his role within IBM to also look at ESD and latch-up devices in 0.25 µm and beyond. From 1998 through 2003 he worked on 0.25 µm–0.13 µm technologies, getting heavily involved in ESD and latch-up. In 2004 he became an R&D manager at IBM with emphasis on ESD/latch-up development and RF modeling. From 2004–2015 he continued to manage the ESD/latch-up team inside IBM along with various other functions such as TCAD. In 2015 he and the majority of his team joined GlobalFoundries during an acquisition; from 2015–2020 he led the worldwide ESD/latch-up team within GlobalFoundries, including teams in the U.S., Dresden, and Singapore. He has over 285 issued patents with many others filed, and more than 50 publications at major conferences and journals. He has served on the ESDA Board of Directors in the past and currently, and is also an active member of the ESDA EXCOM team. He was one of the founders of the International ESD Workshop (IEW) and is a former General Chair of the EOS/ESD Symposium.

Michael G. Khazhinsky, Ph.D.

Dr. Khazhinsky is a Principal ESD engineer at Silicon Labs in Austin, Texas. Prior to joining Silicon Labs, he was employed at Motorola and Freescale Semiconductors, where he managed TCAD development and ESD/latch-up protection solutions for emerging process technologies, with an emphasis on ESD-EDA. Michael holds an M.S.E.E. and M.S. in Physics from the Moscow State Institute of Electronic Engineering, and a Ph.D. in Physics from Western Michigan University. He chairs the ESDA Working Group 18 on EDA and has been involved in several Technical Program Committees including IRPS, IEW, ESREF, EMC, ISTFA, IPFA, and EOS/ESD Symposium. He has chaired the International ESD Workshop and held roles such as Workshop Chair, Technical Program Chair, Vice General Chair, and General Chair of the EOS/ESD Symposium. Michael has co-authored over 60 papers and delivered numerous invited talks on ESD, EDA, process/device TCAD, and photonic crystals. He has received seven "Best Paper" and "Best Presentation" awards from the EOS/ESD Symposium and SOI Symposium, along with the Industry Pioneer Recognition Award for his contributions to ESD EDA verification. He holds eighteen patents related to ESD design, is a Senior Member of IEEE, and serves as Vice President of the ESD Association, responsible for international conferences and events.