EOS/ESD SYMPOSIUM ON DESIGN AND SYSTEM

The Ritz-Carlton
269 Shuncheng Avenue, Qingyang District, Chengdu, Sichuan, 610017 China
November 11-13, 2020

EOS/ESD Association, Inc. is sponsoring the 2020 International EOS/ESD Symposium on Design and System (IEDS). IEDS 2020 is dedicated to the fundamental understanding of issues related to electrostatic discharge on design and system and the application of this knowledge to the solution of problems.

Seminars - Technical Sessions - Keynote - Workshops

Presented papers will be related to the following tracks:

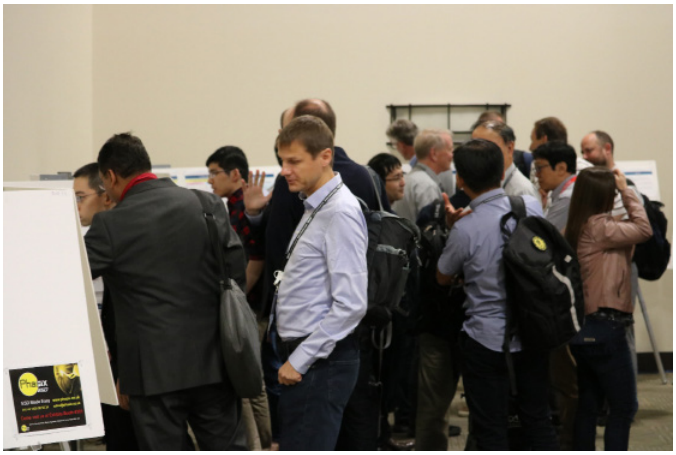
- Advanced CMOS EOS/ESD and Latch-up
- ESD protection in Bipolar, RF, High-voltage, and BCD technologies
- ESD modeling, simulation and design automation
- EOS/ESD Failure analysis and case studies
- ESD and latch-up testing
- System ESD design and troubleshooting issues
- ESD manufacturing control issues and target level discussion

Conference Chair:
李军俊 (Junjun Li) ESDA

Conference co-Chair:
董树荣 (Shurong Dong) 浙江大学 (ZJU)

Technical Program Chair
王源 (Yuan Wang) 北京大学 (PKU)

Conference Site Chair (Chengdu)
刘志伟 (Zhiwei Liu) 电子科技大学(UESTC)



General Chair Welcome

Dear colleagues, friends, and fellow EOS/ESD enthusiasts,

On behalf of EOS/ESD Association, Inc. and the 2020 Management Committee, I would like to personally welcome you to the 1st annual **I**nternational **E**OS/**E**SD Symposium on **D**esign and **S**ystem (**IEDS**)! This year the IEDS will be held at the Ritz-Carlton, in Chengdu, Sichuan, China. With its world famous Sichuan Cuisine, friendly Panda Bears, and endless tea drinking, I encourage you to dive into the hot topics of this year's EOS/ESD presentations, discussions, and exhibitions, and at the same time, take some time off to enjoy the unparallel beauty of what Chengdu offers!

For the first time, the world's leading forum on Electrostatic Discharge and Overstress finds its root in the fast growing greater China region, where technology developers, chip designers, electronics manufacturers and system assembler are all facing the same question: how to mitigate the EOS and ESD challenge whereas at the same time meet the latest application needs, be it mobile, automobile, AI or IoT, to name a few. Continuing the long tradition of the annual EOS/ESD Symposium, the IEDS will address the latest research on EOS and ESD in the rapidly changing world of electronics. To overcome the ever-changing challenges from the sensibility of advanced technologies, progress has to be made in the form of creative ESD design, innovative, comprehensive, and predictive verification of the control standards and methods. The 2020 EOS/ESD Symposium addresses these matters and more with seminars, workshops, technical sessions, invited talks, and through the products and services presented in the industry exhibits.

Technical Program: Our technical program, the heart of the symposium, has introduced two parallel tracks to accommodate your diverse interests. The main technical program includes 42 outstanding presentations, addressing latest innovations in the area of EOS and ESD. These will be presented Thursday through Friday in 8 sessions covering hot topics in the areas of *Advanced CMOS, ESD Modeling and Simulation, ESD Protection in Bipolar, RF and High-voltage Applications, ESD Tester and ESD Testing, System level ESD, and ESD Manufacturing and Factory Control.*

Seminars: World-class experts, in the areas of EOS and ESD, have prepared a unique full-day seminar program to answer questions from today's electronics market. In addition to classics on *Advanced on-chip ESD Protection*, we have organized seminar topics on *ESD design for RF Circuits, System Level ESD Protection, and ESD design for High Voltage Applications*. These talks are arranged into two parallel tracks and will be presented on Wednesday, each with a dedicated Q&A session right after the seminar talk.

Workshops: The four symposium workshops taking place on Thursday and Friday afternoon offer an interactive forum for sharing experiences, exchanging knowledge, and jointly searching for and defining possible solutions. All workshops are centered on relevant and timely technical topics; each workshop allows participants the opportunity to learn about different perspectives from other colleagues in the field and allow the discussion of occasionally controversial topics in an informal environment.

With this many carefully selected options happening in Chengdu it provides an experience both impressive and rewarding, for each member traveling from all around the world. The symposium is a truly international event and I welcome you to this exciting forum to enjoy all the technical achievements from your peers, and continue to form the special life-long bond with people, device, system, and the word of EOS/ESD!

Sincerely,

Dr. Junjun Li
Board of Directors, EOS/ESD Association
2020 IEDS General Chair

IEDS 2020 (Chengdu) Program

Day 1 (Wednesday, November 11, 2020)

Seminar Session A

9:00 ~ 10:00	S.1	Nate Peachey	ESD Solutions for RF Applications
10:00 ~ 10:15			**Break**
10:15 ~ 11:15	S.1	Nate Peachey	ESD Solutions for RF Applications
11:15 ~ 11:30	S.1	Nate Peachey	Q&A
11:30 ~ 14:00			**Lunch**
14:00 ~ 15:00	S.3	Shih-hung Chen	Towards Optimal ESD Protection Diodes in Advanced Bulk FinFET and GAA Technologies
15:15 ~ 16:15			**Break**
16:15 ~ 17:15	S.3	Shih-hung Chen	Towards Optimal ESD Protection Diodes in Advanced Bulk FinFET and GAA Technologies
17:15 ~ 17:30	S.3	Shih-hung Chen	Q&A

Seminar Session B

9:00 ~ 10:00	S.2	David Pommerenke	Quantifying System Level ESD and Protecting I/O
10:00 ~ 10:15			**Break**
10:15 ~ 11:15	S.2	David Pommerenke	Quantifying System Level ESD and Protecting I/O
11:15 ~ 11:30	S.2	David Pommerenke	Q&A
11:30 ~ 14:00			**Lunch**
14:00 ~ 15:00	S.4	Filippo Magrini	Introduction to ESD Design in High Voltage Technologies
15:15 ~ 16:15			**Break**
16:15 ~ 17:15	S.4	Filippo Magrini	Introduction to ESD Design in High Voltage Technologies
17:15 ~ 17:30	S.4	Filippo Magrini	Q&A

IEDS 2020 (Chengdu) Program

Day 2 (Thursday, November 12, 2020)

Parallel Session

8:00	~	8:30		Opening
8:30	~	9:30		Keynote - Advanced ESD Design Facilitated by Circuit Simulation
9:30	~	10:20		Invited - Symposium Award Presentation
10:20	~	10:50		**Break**

Technical Session A1 (Advanced CMOS, ESD Modeling and Simulation)

10:50	~	11:15	A1.1	Zhong Chen (Invited)	Novel Dual-Diodes for Rail-based On-chip ESD Protections
11:15	~	11:40	A1.2	Lihui Wang (Invited)	Methods for Designing RC-triggered ESD Power Clamp Circuits
11:40	~	12:05	A1.3 (PUB.1)	Wenqiang Song	Design of A New Low Voltage Triggered Silicon Controlled Rectifier(SCR) for ESD Applications
12:05	~	12:30	A1.4 (PUB.2)	Yize Wang	Study of ESD Device Modeling Based on Neural Network
12:30	~	14:00			**Lunch**

Technical Session C1 (ESD Tester and ESD Testing)

14:00	~	14:25	C1.1	Masanori Sawada (Invited)	Consideration on Discharge Waveform of GND Relay Free System of High pin count ESD tester
14:25	~	14:50	C1.2	Yingjie Gan (Invited)	TLP and vf-TLP Test Methods, Applications
14:50	~	15:15	C1.3 (PUB.18)	Yu Lu	Development of a TLP System with a Novel Current Sampling Technique for ESD Protection Application
15:15	~	15:40			**Break**
15:40	~	16:05	C1.4	Teruo Suzuki (Invited)	CDM Measurement for Bare Dies and Wafers
16:05	~	16:30	C1.5	Kimi Lai (Invited)	Investigation on ESD trend and event of automotive electronics
16:30	~	17:00			**Break**
17:00	~	18:00			**Workshop A.1 - ESD Protection for RF Applications**

Technical Session B1 (ESD Protection in Bipolar, RF and High-voltage Applications)

10:50	~	11:15	B1.1	Chun-Yu Lin (Invited)	Compact ESD Protection Cell for 5G Applications
11:15	~	11:40	B1.2 (PUB.10)	Raunak Kumar	Design Optimization of High Voltage NPN ESD Protection Device in 130nm Power SOI Technology
11:40	~	12:05	B1.3 (PUB.11)	Prantik Mahajan	Optimization of GGNMOS Devices for High-Voltage ESD Protection in BCDLite Technology
12:05	~	12:30	B1.4 (PUB.12)	Xiangliang Jin	DDSCR Device Structure Fabricated on 0.5μm CMOS Process
12:30	~	14:00			**Lunch**

Technical Session D1 (System Level ESD)

14:00	~	14:25	D1.1	Beiping Yan (Invited)	Low Capacitance Transient Voltage Suppressor (TVS) for High Speed Data Line Protection
14:25	~	14:50	D1.2 (PUB.19)	Guanghui Liu	Module and System Level ESD Co-Design and Simulation of Mobile Phone Antenna Systems
14:50	~	15:15	D1.3	Xing Wu (Invited)	In situ TEM study on ESD FA
15:15	~	15:40			**Break**
15:40	~	16:05	D1.4	Hiroyasu Ishizuka (Invited)	Discharge current analysis of charge board event and consideration the design concept
16:05	~	16:30	D1.5 (PUB.20)	Yanlin Nie	Pulse Frequency Effects on Probability of ESD Soft Failures
16:30	~	17:00			
17:00	~	18:00			**Workshop A.2 - Can Robust ESD Design be Achieved and Verified Using IEC 61000-4-2 Testing?**

18:30	~	20:30	**Banquet**

IEDS 2020 (Chengdu) Program

Day 3 (Friday, November 13, 2020)

				Technical Session A2 (Advanced CMOS, ESD Modeling and Simulation)
9:00	~ 9:25	A2.1 (PUB.22)	Meng Miao (Invited)	Design and Optimization of Diode Triggered Silicon Controlled Rectifier in FinFET Technology
9:25	~ 9:50	A2.2 (PUB.3)	Guangyi Lu	Investigation on Fabrication-Induced High-Leakage Issue of an Overdrive ESD Power Clamp in Advanced FinFET Technology
9:50	~ 10:15	A2.3 (PUB.4)	Yunhao Li	ESD Diode Devices Simulation and Analysis in a FinFET Technology
10:15	~ 10:45			**Break**
10:45	~ 11:10	A2.4	Yuanzhong Zhou (Invited)	Unexpected ESD Weakness Revealed by Circuit Level ESD Simulation with SPICE
11:10	~ 11:35	A2.5	Mingliang Li (Invited)	General Purpose I/O Circuits and Full-chip ESD Protection Design
11:35	~ 12:00	A2.6 (PUB.5)	Zhenghui Kong	A Study of the Electrical and Mechanical Reliability Properties of Suspended Graphene NEMS Devices for ESD Protection Applications
12:00	~ 14:00			**Lunch**
				Technical Session A3 (Advanced CMOS, ESD Modeling and Simulation)
14:00	~ 14:25	A3.1	Sukjin Kim (Invited)	ESD Design Challenges and Solutions in FinFET Technologies
14:25	~ 14:50	A3.2	Xiaozong Huang (Invited)	ESD Protection Strategy for a Mixed-signal ASIC with Multiple Power Domains
14:50	~ 15:15	A3.3 (PUB.6)	Xiaoyun Li	A Novel Area-Efficient ESD Power Clamp with Enhanced Noise Immunity
15:15	~ 15:40			**Break**
15:40	~ 16:05	A3.4 (PUB.7)	Xiaotian Chen	Experimental Investigation of ESD Protection for a 22-nm FD-SOI Process
16:05	~ 16:30	A3.5 (PUB.8)	Zhaonian Yang	A Modified RC and Diode Co-Triggered ESD Clamp Circuit
16:30	~ 16:55	A3.6 (PUB.9)	Xinyu Zhu	ESD Pulse Width Effect on RC-Triggered NMOS With Power On or Off
16:55	~ 17:30			**Break**
17:30	~ 18:30			**Workshop B.1 - High Voltage ESD Protection Effectiveness and Efficiency - From Component Level to Whole Chip Solutions**
				Technical Session B2 (ESD Protection in Bipolar, RF and High-voltage Applications)
9:00	~ 9:25	B2.1 (PUB.13)	Jie (Jack) Zeng	Optimization of NPN ESD Protection Device for Improved Failure Current
9:25	~ 9:50	B2.2 (PUB.14)	Johan Van der Borght	Optimized Local I/O ESD Protection for SerDes Interfaces In Advanced SOI, BiCMOS and FinFET Technology
9:50	~ 10:15	B2.3 (PUB.15)	Zhuojun Chen	Design and Characterization of a SCR with separate bipolar transistors for ESD Protection
10:15	~ 10:45			**Break**
10:45	~ 11:10	B2.4	Yonghai Hu (Invited)	A study of the application requirements of the off-chip ESD protection devices
11:10	~ 11:35	B2.5 (PUB.16)	Zeyu Zhong	Verification of an Equivalent Circuit Model for LDMOS-SCR Based on 0.5μm CMOS Process
11:35	~ 12:00	B2.6 (PUB.17)	Danye Liang	Optimized Structures of Dual-directional Silicon-Controlled Rectifier with Segments Technology
12:00	~ 14:00			**Lunch**
				Technical Session E1 (ESD Manufacturing and Factory Control)
14:00	~ 14:25	E1.1	Shengzong He (Invited)	Factory static PCBA failure, control and solution case study
14:25	~ 14:50	E1.2	Bernard Chin (Invited)	How do I get my manufacturing site ANSI/ESD S20.20 certified?
14:50	~ 15:15	E1.3 (PUB.23)	Marcus Koh (Invited)	EOS/ESD Manufacturing Mitigation Review
15:15	~ 15:40			**Break**
15:40	~ 16:05	E1.4	Haibei (Invited)	Electronic manufacturing process ESD system upgrade
16:05	~ 16:30	E1.5	Figo Lu (Invited)	The impact of ESD on PCBA and protection
16:30	~ 16:55	E1.6 (PUB.21)	Zhiyi Bao	High Temperature Resistant ESD Mats for PCB Bake Tray Usage
16:55	~ 17:30			**Break**
17:30	~ 18:30			**Workshop B.2 - Challenges and Opportunities in Manufacturing ESD Control**

Seminar 1
ESD Solutions for RF Applications

Nathaniel Peachey, Qorvo

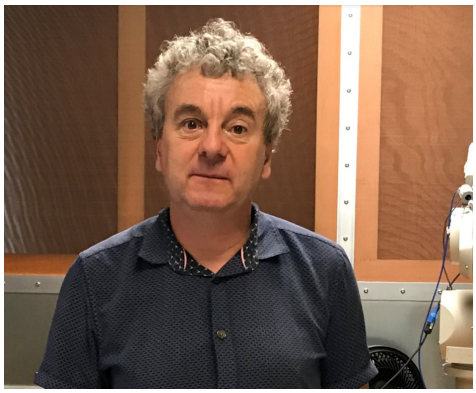
Abstract
While designing circuits for complex applications can be challenging, RF circuits present additional requirements on the designer. Not only are these circuits very sensitive to ESD threats, but adding ESD protection will invariably compromise performance. Thus, in most cases, the design of functionality and ESD protection must be done as co-design. This seminar will address the various aspects of advanced ESD design. This will then be extended to RF applications and ESD co-design. Finally, this seminar will discuss various case studies to illustrate the principles presented.

Biography
Nathaniel Peachey received his PhD in physical chemistry in 1994 from the University of Nebraska–Lincoln and then was awarded a director's funded postdoctoral fellowship at the Los Alamos National Laboratory; where he studied thin-film membranes for gas separation. In 1996, he joined Atmel Corporation in Colorado Springs as a thin-films process engineer. Over the next several years Dr. Peachey held various positions at Atmel including process engineer, technology development engineer, device engineer, and circuit design engineer. In 2003, he began focusing exclusively on ESD protection and I/O design issues. In 2005, Dr. Peachey accepted the position of engineering manager for the newly formed ESD design group at RF Micro Devices (currently Qorvo, Inc.). In this capacity, he was responsible for the development of ESD protection for all the technologies that Qorvo designed including both silicon and GaAs. Besides on-chip protection he led the development and improvement of the RF antenna ESD protection. Dr. Peachey has authored and coauthored over 30 technical journal submissions. He has also submitted 14 patents that have either been granted or are pending. Dr. Peachey is also a senior member of the IEEE. In 2009, Dr. Peachey was elected to the board of directors for EOS/ESD Association, Inc. He has been involved in various activities within EOS/ESD Association, Inc. Currently, he is serving as the Vice President.

Seminar 2
Quantifying System Level ESD and Protecting I/O

David Pommerenke, IEEE Fellow

Abstract
This seminar will describe the different entry paths of ESD into a system, such as the breakdown through gaps in the plastic, the corona induced currents from discharges to displays, and the discharges into I/O such as USB. This will enable engineers to quantify the threat for the different entry paths, and base design guidelines on this information. In the second, part this seminar will explain the System Efficient ESD Design strategy that allows to design efficient protection even for 10 GHz+ I/O based on simulation. The simulation needs transient models for the TVS diodes and models for the ICs. It is shown how these models are obtained and how the simulation is performed. The last part of the seminar will show how to even reduce the likelihood of soft-failure on I/O, such as USB by selecting protection elements based on simulation.



Biography
Dr. David Pommerenke received his diploma and PhD from the Technical University Berlin, Germany. His research interests are system level ESD, electronics, numerical simulations, EMC measurement methods and instrumentation. He worked at Hewlett Packard for 5 years before joining the electromagnetic compatibility laboratory at the Missouri University of S&T in 2001. Dr. Pommerenke became the CTO of ESDEMC in July 2019 before joining the ESD/EMC group at the Technical University of Graz in Austria in January 2020. His new focus is on ESD, EMC, harmonics, and PIM. He has published more than 200 papers and is inventor on 13 patents. His main research interests are measurement/instrumentation ESD, electronic design and EMC. He is IEEE fellow and associated editor for the IEEE Transactions on EMC.
He can be reached at david.pommerenke@ieee.org

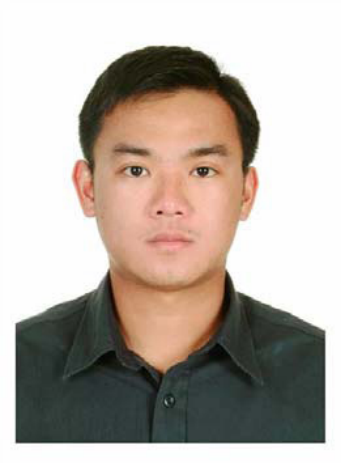
Seminar 3

Towards Optimal ESD Protection Diodes in Advanced Bulk FinFET and GAA Technologies

Shih-Hung Chen, imec

Abstract

As CMOS technology nodes scaling beyond 20nm, bulk FinFET (FF) has become the mainstream technology in mobile and computing applications. ESD reliability is strongly impacted by not only the geometry scaling, but also by newly introduced process options in the advanced bulk FinFET technologies. To further enhance function transistor performance, a gate-all-around (GAA) architecture has been proposed as a promising candidate in sub-5nm CMOS technology nodes. This new device architecture with new process options can bring further challenges of ESD reliability. In this seminar, we will look at the influence of the device architectures and the corresponding process options on ESD device characteristics in the FinFET/GAA NW technologies. 3D TCAD simulations bring an in-depth physical understanding of the ESD current conduction and failure mechanism in the ESD protection diodes.



Biography

Shih-Hung Chen received the PhD degree from the Institute of Electronics, National Chiao Tung University, in 2009. In 2002, he joined the ITRI, Hsinchu, as an ESD Engineer. Since 2010, he has been with Device Reliability and Electric Characterization (DRE) Group at imec, as a senior ESD researcher. He authored or co-authored more than 100 conference and journal publications. He has served as a TPC member in IEEE IRPS since 2016, and in EOS/ESD Symposium since 2014. His current research interests include ESD protections in sub-10nm technologies, in 3D/2.5D IC applications, and in STCO with the integrations of III-V materials.

Seminar 4
Introduction to ESD Design in High Voltage Technologies

Filippo Magrini, Infineon

Abstract
This seminar gives an introduction to ESD design in high voltage technologies for integrated circuits with pin voltages from 12 volts upwards. After a short introduction of typical applications and requirements, an overview of different technologies and the typical device portfolios in these technologies will be given. Different ESD protection concepts are introduced, analyzing advantages and disadvantages of the various possible approaches to implement ESD networks (diodes, snapback, active clamps…). Finally, HV-technology and design related challenges regarding ESD protection are discussed, with a special focus on relevant case studies.

Biography
Filippo Magrini was born in Parma, Italy. He received his M. Sc. degree in electronic engineering from the “Universitá degli Studi di Parma” in 2007, discussing a thesis on numeric simulations of power PiN diodes. In 2008, he joined the automotive power technology development department of Infineon Technologies where, since then, he has been responsible for the development of ESD protection devices and concepts in advanced Smart Power technologies. In the latest years, his focus has addressed reverse engineering topics, the development of HV-SCRs and the investigation of discrete MOSFETs’ dynamic behavior. His responsibilities also cover the support of design teams with respect to the implementation of robust on-chip ESD protection design. Filippo has authored and co-authored several papers published at international ESD and EMC conferences. He received the EOS/ESD Symposium best paper award in 2011.

KEYNOTE

Thursday, November 12
8:30 - 9:30

Advanced ESD Design Facilitated by Circuit Simulation

Elyse Rosenbaum, Melvin and Anne Louise Hassebrock Professor in Electrical and Computer Engineering, University of Illinois at Urbana-Champaign

Technology scaling has made integrated circuits more vulnerable to ESD-induced damage, but that same scaling allows CMOS circuits to operate at unprecedentedly high data rates. For example, the IEEE 802.3bs standard for 400 Gb/s Ethernet specifies a per-lane bit rate of 53.125 Gb/s. Providing the necessary on-chip protection without compromising the circuit performance is more difficult than ever before. It can be assumed that there is only a small design window in which both performance and reliability specifications can be met, and circuit simulation will be a critical tool for executing the challenging circuit design. The simulation netlist must include the ESD protection devices, and those devices must be represented by models that are accurate under both normal operating conditions and high-current ESD conditions. This talk will start with an overview of state-of-the-art ESD protection for high-speed and RF IO pins. Next, the requirements for ESD models will be identified and the shortcomings of current models will be described.

Elyse Rosenbaum is the Melvin and Anne Louise Hassebrock Professor in Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. She received a PhD in electrical engineering from University of California, Berkeley. She is the director of the NSF-supported Center for Advanced Electronics through Machine Learning (CAEML), a joint project of the University of Illinois, Georgia Tech and North Carolina State University. Her current research interests include machine-learning aided behavioral modeling of microelectronic components and systems, compact models, circuit reliability simulation, component and system-level ESD reliability, and ESD-robust high-speed I/O circuit design. Dr. Rosenbaum has authored or co-authored nearly 200 technical papers; she has been an editor for IEEE Transactions on Device and Materials Reliability and IEEE Transactions on Electron Devices. She was the recipient of a Best Student Paper Award from the IEDM, Outstanding and Best Paper Awards from the EOS/ESD Symposium, a Technical Excellence Award from the SRC, an NSF CAREER award, an IBM Faculty Award, and the ESD Association's Industry Pioneer Recognition Award. She is a Fellow of the IEEE.

Feature: EOS/ESD Association, Inc. Symposium Award Paper 9:30 - 10:20

Session A1: 10:50 - 12:30

A1: Advanced CMOS, ESD Modeling and Simulation

Moderator: Yuan Wang, Peking University

A1.1 Novel Dual-Diodes for Rail-Based On-chip ESD Protections

Zhong Chen, Hui Wang, Pengyu Lai, University of Arkansas

Rail-based ESD network has been widely implemented for on-chip ESD protection. Innovative approach will be presented to utilize parasitic components in these dual-diode ESD structures for many applications such as high-speed interface ICs, MCU, RF, etc. Area-efficient dual-diodes can be integrated with different types of primary ESD structures to reduce adverse impacts on the circuit performance and meet specific pin requirements. In addition, this novel structure can alleviate design challenges due to system-level ESD requirements on ICs.

A1.2 Methods for Designing RC-triggered ESD Power Clamp Circuits

Lihui Wang, Guangyi Lu, HiSilicon

RC-triggered power clamp has been widely used in nano-scale CMOS integrated circuits. This approach provides robust and highly efficient ESD protection and allows simulation-based circuit optimization. In this talk, a brief overview on classification of the ESD power clamps, key design parameters and triggering mechanism will first be presented. This is followed by exploring design techniques for improving ESD performance, design window and noise immunity of RC-triggered power clamps.

A1.3 (PUB.1) Design of A New Low Voltage Triggered Silicon Controlled Rectifier(SCR) for ESD Applications

Wenqiang Song, Feibo Du, Fei Hou, Jizhi Liu, Zhiwei Liu, IEEE; Juin J. Liou, IEEE; Shenzhen University

In this paper, a new low-voltage triggered silicon-controlled rectifier (NLVTSCR) with low trigger voltage and higher holding voltage is proposed and implemented in a 28nm CMOS process. The proposed NLVTSCR in the TLP test has a low trigger voltage and an adjustable high hold voltage from 3.44V to 4.93V. In addition, it does not require any additional masks, making it an excellent candidate for 3.3V ESD protection. Compared to conventional low triggered voltage silicon-controlled rectifier (LVTSCR), the proposed NLVTSCR device provides a higher holding voltage than its conventional counterpart.

A1.4 Study of ESD Device Modeling Based on Neural Network

Yize Wang, Yunhao Li, Yuan Wang, Peking University

Modeling method of electro-static discharge (ESD) devices based on neural network is introduced in this work. The new ESD models are scalable and can much reduce the complexity compared with traditional ones. All the modeling process and verification for the neural network model are shown in detail.

Session B2: 10:50 - 12:30

B1: ESD Protection in Bipolar, RF and High-voltage Applications

Moderator: Zhiwei Liu, UESTC

B1.1 Compact ESD Protection Cell for 5G Applications

Chun-Yu Lin, National Taiwan Normal University

Multiple millimeter-wave (MMW) frequency bands are considered for fifth-generation (5G) systems. A compact ESD protection cell by using an inductor with ESD protection devices to achieve the sufficiently small layout area, higher ESD robustness, and lower loss for 5G / multi-band MMW applications is presented in this work.

B1.2 (PUB.10) Design Optimization of High Voltage NPN ESD Protection Device in 130nm Power SOI Technology

Raunak Kumar, Jie (Jack) Zeng, Kyong Jin Hwang, Robert Gauthier Jr, GLOBALFOUNDRIES

A HV NPN ESD devices is evaluated in a 130nm Power SOI technology. Current flow and temperature distribution under ESD stress is investigated by TCAD and a new device architecture without STI is proposed. Non-uniform triggering issue is also investigated. Segment type layout design shows uniform triggering of multi-finger devices.

B1.3 (PUB.11) Optimization of GGNMOS Devices for High-Voltage ESD Protection in BCDLite Technology

Prantik Mahajan, Raunak Kumar, Robert Gauthier, Kyong Jin Hwang, GLOBALFOUNDRIES

Design optimization of Electrostatic Discharge (ESD) GGNMOS for high-voltage applications in low-cost BCDLite technology is presented. Clamp performance optimization through body PWELL engineering and device design techniques are investigated. A comparative analysis between two distinct device architectures (different Poly-LOCOS overlap) showing 100ns TLP measurement and TCAD simulation results is presented.

B1.4 (PUB. 12) DDSCR Device Structure Fabricated on 0.5μm CMOS Process

Xiangliang Jin, Yang Wang, Hunan Normal University

Dual Direction Silicon Controlled Rectifier(DDSCR) are primarily used for ESD protection in high voltage environments. According to the results of the device test, the trigger voltage and the sustain voltage of the DDSCR are 17.62V and 9.54V, respectively. Finally, by changing the important dimensions of the DDSCR, the ESD characteristics of the device can be significantly improved.

Session C1: 14:00 - 16:30

C1: ESD Tester and ESD Testing

Moderator: Shurong Dong, Zhejiang University

C1.1 Consideration on Discharge Waveform of GND Relay Free System of High pin count ESD Tester

Masanori Sawada, Haruki Nakao, Hideaki Miura, Nobuchika Matsui, HANWA ELECTRONIC

Traditional ESD tester at the effect of parasitic capacitor in relay matrix, A-side and B-side waveform difference has been confirmed. To solve this problem, it reconsiders the relay base system and it proposes ESD tester with new structure for GND setting.

C1.2 TLP and vf-TLP Test Methods, Applications

Yingjie Gan, Dong Zhang, Shanghai Will Semiconductor

This report explains the theory of TLP and vf-TLP test methods; the basic implementation of the TDR-O and TDR-S measurement methods; typical applications of the methods; how to do a good measurements in terms of calibration and verification, probing fixture, TLP measurement repeatability; and other frequently asked questions of TLP/vf-TLP measurement.

C1.3 (PUB. 18) Development of a TLP System with a Novel Current Sampling Technique for ESD Protection Application

Yu Lu, Shanghai Xirun Technologies, Co. Ltd; Peking University; Yuhua Cheng, Peking University

This paper presents a a TLP test system with a new current sampling method, which has the advantages of simpler structure, higher theoretical bandwidth and higher upper limit of test current. ESD protection properties of both semiconductor and gNEMS devices were tested with the developed TLP testing machine and good testing results are achieved.

C1.4 CDM Measurement for Bare Dies and Wafers

Teruo Suzuki, Socionext

Resolving frequent ESD failures at an assembly house was time-consuming. Testing the robustness of the CDM in the wafer/bare die state would provide early information about problems with ESD design or electrostatic controls. With our new JS-002-compliant Wafer CDM tester, we tested products as wafers/bare dies to achieve the desired robustness.

C1.5 Investigation on ESD Trend and Event of Automotive Electronics

Kimi Lai, Phil Chen, Russell Huang, Integrated Service Technology CO.,LTD (ISTC)

For automotive designs that require safety and high reliability, ESD test is a key methodology to quantify robustness both of component level and system level. This presentation provides ESD test standards for electronic components of the automotive industry and offers flexibility and completed solutions of ESD testing that meet automotive ESD requirements. In addition, case study of failure analysis is to reveal the typical failure mechanism for ESD test rejects, which helps design improvement of ESD protection circuits.

Session D1: 14:00 - 16:30

D1: System Level ESD

Moderator: Shurong Dong, Zhejiang University

D1.1 Low Capacitance Transient Voltage Suppressor (TVS) for High Speed Data Line Protection

Beiping Yan, Hong Kong Applied Science and Technology Research Institute (ASTRI)

Currently, high-speed USB3.0 and HDMI cable connections are used pervasively. These applications require good ESD/ surge protection and high signal integrity, which limits the available capacitance budget. Therefore, it is important to develop low-capacitance TVS for high speed data line protection. This paper presents the research and development of low capacitance TVS devices.

D1.2 (PUB. 19) Module and System Level ESD Co-Design and Simulation of Mobile Phone Antenna Systems

Guanghui Lui, Vivo; Kathleen Muhonen, Nathan Sechrest, Nathaniel Peachey, Qorvo

Device and system level co-design and co-simulation have been studied for a mobile phone antenna system. TLP data taken with the antenna module both powered off and powered on were used to model its response in the simulation. With this, the mobile phone antenna was built and tested in simulation.

D1.3 In Situ TEM Study on ESD FA

Xing Wu, East China Normal University

Transmission electron microscopy (TEM), with its high spatial resolution and versatile external fields, is undoubtedly a powerful tool for the static characterization and dynamic manipulation of nanomaterials and nanodevices at the atomic scale. The rapid-development of thin-film and precision microelectromechanical systems (MEMS) techniques allows the microstructure during ESD to be probed and engineered inside TEM under external stimuli such as electrical andthermal fields at the nanoscale. Here, taking advantage of advanced in situ transmission electron microscopy, we manipulatedinterfaces of ESD. The progress of the in situ TEM paves the way to future nanodevices.

D1.4 Discharge Current Analysis of Charge Board Event and Consideration the Design Concept

Hiroyasu Ishizuka, Masanori Sawada, Synaptics HANWA ELECTRONIC

Analyzed the discharge current waveform of CBE(Charged Board Event) occurring in the system production line and the field, using mobile phone and panel module.
Main discharged current is characterized by very high speed rise time, narrow width and high current level without high energy, which indicates the need for a new design strategy to remove CBE failure.

D1.5 (PUB.20) Module and System Level ESD Co-Design and Simulation of Mobile Phone Antenna Systems

Yanlin Nie, Qiupei Huang, Zhiwei Liu, Jizhi Liu, University Of Electronic Science and Technology Of China; Xiang Li, Xiaofei Xie, Huawei Technologies Co., LTD.

In this paper the analysis of measurement pulse frequency effects on soft failure probability of DUT is presented. Different pulse intervals are implemented on a camera sub-system of a smartphone prototype. It is found that not only the pulse voltage but also the frequency affects soft failure probabilities.

Session A2: 9:00 - 12:00

A2: Advanced CMOS, ESD Modeling and Simulation

Moderator: Yuan Wang, Peking University

A2.1 (PUB. 22) Design and Optimization of Diode Triggered Silicon Controlled Rectifier in FinFET Technology

Meng Miao, You Li, Robert Gauthier, Globalfoundries

Diode trigger SCR (DTSCR) structure is introduced in FinFET technology for low voltage circuit ESD protection. The current direction is chosen to flow across fins to make full use of the bulk silicon region. Further optimization of DTSCR is investigated to improve layout efficiency

A2.2 Investigation on Fabrication-Induced High-Leakage Issue of an Overdrive ESD Power Clamp in Advanced FinFET Technology

Guangyi Lu, Lihui Wang, Ling Wang, Xin Gao, Mei Li, Hisilicon Technologies Co., LTD

Fabrication-induced high-leakage issue of an overdrive ESD power clamp is presented. With silicon data exhibiting abnormal results, elaborate troubleshooting is performed and disclosed in this paper. Through alignments of silicon data and presumptive simulation results, fabrication-induced root cause is successfully revealed and confirmed by physical failure analysis (PFA) results.

A2.3 (PUB. 4) ESD Diode Devices Simulation and Analysis in a FinFET Technology

Yunhao Li, Yize Wang, Yuan Wang, Peking University

As CMOS scaling down to FinFET technology, the performance of ESD devices degenerate seriously. In this work, two types of ESD protection diodes, Gated Diode and STI Diode, are invested in 14nm FinFET technology. The corresponding 3D TCAD simulation result help to understand the working mechanism of ESD protection diodes.

A2.4 Unexpected ESD Weakness Revealed by Circuit Level ESD Simulation with SPICE

Yuanzhong (Paul) Zhou, Jean-Jacques Hajjar, Analog Devices

The circuit level ESD simulation with SPICE has been adopted by an increasing number of people for ESD protection design and verification. A few case studies will be presented to show the simulation may reveal unexpected effects in ESD qualification testing, such as extremely higher peak current than the one defined by the HBM test standard. Those unusual effects have been validated later by experimental observation, which demonstrates great benefits from ESD simulation and also indicates that physics-based models should be always the first choice whenever it is possible.

A2.5 General Purpose I/O Circuits and Full-Chip ESD Protection Design

Mingliang Li, HiSilicon

Presents an overview on general purpose I/O circuits and full-chip ESD protection for current main-stream integrated circuits. It includes TTL/CMOS interface standard, DC/AC specification, regular GPIO design, mixed-voltage interface circuits design, noise margin, noise isolation□chip I/O floor-plan of different package, and high reliable full-chip ESD network design for HBM/MM/CDM stress.

A2.6 (PUB. 5) A Study of the Electrical and Mechanical Reliability Properties of Suspended Graphene NEMS Devices for ESD Protection Applications

Zhenghui Kong Lele Jiang, Yuhua Cheng, Peking University; Yu Lu, Peking University; Shanghai Xirun Technologies, Co. Ltd ; Qi Chen, Albert Wang, University of California

Recent studies have found that a novel and unique above-IC graphene-based nano-electro-mechanical system (gNEMS) transient switch can be a potential ESD protection. This new ESD switch device is designed by using a suspended graphene membrane structure. In this work, we present experimental investigations and physical insights into the reliability issue and failure mechanism of this graphene ESD device by transient transmission line pulse (TLP) measurement. The mechanical bending evolution and fracture of the graphene membrane via electrostatic actuation assessed with the transient analysis in ESD time scales.

Session B2: 9:00 - 12:00

B2: ESD Protection in Bipolar, RF and High-voltage Applications

Moderator: Zhiwei Liu, UESTC

B2.1 (PUB. 13) Optimization of NPN ESD Protection Device for Improved Failure Current

Jie (Jack) Zeng, Raunak Kumar, Tsung-Che Tsai, Sevashanmugam Marimuthu, Robert Gauthier Jr, GLOBALFOUNDRIES

This paper present a high voltage NPN based ESD protection device with a designed PBL under collector region achieving 2.7X failure current improvement compared to structure without PBL in 130nm advanced BCD Technology. It has a flexible feature of tunable trigger and holding voltage without It2 degradation.

B2.2 (PUB 14) Optimized Local I/O ESD Protection for SerDes Interfaces In Advanced SOI, BiCMOS and FinFET Technology

Johan Van der Borght, Ilse Backers, Olivier Marichal, Bart Keppens, Koen Verhaege, Sofics

Semiconductor companies are developing ever faster interfaces to satisfy the need for higher data throughputs. However, the parasitic capacitance of the traditional ESD solutions limits the signal frequency. This paper demonstrates low-cap Analog I/Os for high speed SerDes (28Gbps to 112Gbps) circuits created in advanced BiCMOS, SOI and FinFET nodes.

B2.3 (PUB. 15) Design and Characterization of a SCR with Separate Bipolar Transistors for ESD Protection

Zhuojun Chen , Ming Wu, Wenzhao Lu, Chenchen Zhang, Wei Peng, Yun Zeng, Hunan University

An optimized segmentation topology is developed to enhance the holding voltage. Compared with the traditional LVTSCR, the holding voltage of the proposed device increases o 5.63 V. Besides, the transmission line pulse tests show the improvement of the holding voltage and the effect of temperature on key ESD parameters.

B2.4 A Study of the Application Requirements of the Off-Chip ESD Protection Devices

Yonghai Hu, Dong Zhang, Shanghai Will Semiconductor

In the last decade, the off-chip ESD protection chips have found various applications in the emerging areas such as mobile phones, high-speed ports interface, portable devices and so on. These applications have many critical requirements, such as extremely low triggering voltage, ultra-low capacitances, high hold voltage, and fast turn-on speed to be fulfilled in one ESD protection chip. These requirements are very challenging for ESD devices design. In this study, we reviewed the requirements for some typical applications and studied the principals for how to design the off-chip ESD protection devices to get favorable device characteristics.

B2.5 (PUB. 16) Verification of an Equivalent Circuit Model for LDMOS-SCR Based on 0.5μm CMOS Process

Zeyu Zhong, Xiangliang Jin, Hunan Normal University

Based on a LDMOS-SCR designed and manufactured in 0.5μm CMOS process, a SCR equivalent circuit model for ESD protection is applied and verified. Simulation results show a high consistency with the TLP I-V curve. It contributes to the simulation methodology of SCR devices for ESD protection.

B2.6 (PUB. 17) Optimized Structures of Dual-Directional Silicon-Controlled Rectifier with Segments Technology

Danye Liang, CSMC Technologies Corporation

Two optimized Dual Directional Silicon-Controlled Rectifier (DDSCR) with segments technology were proposed in this paper with 0.25μm BCD process. TCAD simulation results and transmission line pulse (TLP) measurement results of different structures are compared and discussed. Compared to the original DDSCR with segments technology, two new DDSCR structures can achieve higher failure current and relatively high holding voltage.

Session A3: 14:00 - 16:55

A3: Advanced CMOS, ESD Modeling and Simulation

Moderator: Yuan Wang, Peking University

A3.1 ESD Design Challenges and Solutions in FinFET Technologies

Sukjin Kim, Radhakrishnan Sithanandam, Woojin Seo, Mijin Lee, Sangyoung Cho, Juho Park, Hyukhoon Kwon, Namho Kim, Chanhee Jeon Samsung

Continuous optimization of power performance and area of the CMOS technology lead to development of the FinFET technology. Scaling trend in FinFET technology lead to the invention of extreme ultra violet (EUV) lithography based 7nm FinFET technology. However, there are no literatures available which explains the ESD performance with scaling. This paper is an attempt to present the design choices, challenges and solutions available in these FinFET technologies for robust ESD protection. Components of the general purpose I/O's (N+/Psub, NW/Psub, P+/NW diodes) and failsafe I/Os (GGNMOS and BJTs) are analyzed in 14nm, 10nm and 7nm FinFET technologies. For the first time, a brief note on the new charge based CDM analysis strategy which ensures first time silicon success is also explained. The test structure development, fabrication, testing and results are performed in Samsung Foundry.

A3.2 ESD Protection Strategy for a Mixed-Signal ASIC with Multiple Power Domains

Xiaozong Huang, Fan Xiang, Robert Public, Xin Lei, Fan Liu, Lingli Qian, Chongqing Acoustic-optic-electronic Co. Ltd of CETC

ESD protection strategy for a mixed-signal ASIC is presented in this paper. There are multiple power domains with several separated 5V, 4V, 3.3V and 3.3V for different blocks of the circuit. Accordingly, the ground network is divided into digital part, analog part and I/O part for noise isolation performance. For each power domain, the ESD protection network based on the power rail is employed for compact layout size. The protection concerns between different power domains with different power supplies have been considered with predetermined paths.

A3.3 (PUB. 6) A Novel Area-Efficient ESD Power Clamp with Enhanced Noise Immunity

Xiaoyun Li, Lihui Wang, Guangyi Lu, Xin Gao, Mei Li, Hisilicon Technologies Co., LTD

A novel area-efficient ESD power clamp with enhanced noise immunity is proposed. This design can extend on-time of big MOSFET and reuse shutoff NMOS transistor to reduce detection circuit's area. The 29.6% reduction of detection circuit's area is achieved. The verification is done under an advanced FinFET process.

A3.4 (PUB. 7) Experimental Investigation of ESD Protection for a 22-nm FD-SOI Process

Xiaotian Chen, Yize Wang, Yuan Wang, Peking University

To study the electrostatic discharge (ESD) characteristics of the full-depleted silicon-on-isolation (FD-SOI) device, some ESD structures are fabricated in a 22-nm FD-SOI process. The DC and TLP experimental testing have been fulfilled and investigated.

A3.5 (PUB. 8) A Modified RC and Diode Co-Triggered ESD Clamp Circuit

Zhaonian Yang, Pan Mao, XI'an University of Technology

This paper presents a new ESD clamp circuit which is co-triggered by RC and diode. It is immune to the false triggering caused by fast power-up events due to the diode detection mechanism. With the addition of a common source amplifier, the detection signal is enhanced, and the clamp device is turned on more quickly. The proposed circuit is designed in a 0.18 μm 1.8-V CMOS process and verified by numerical simulation. The characteristics and the improvements of the new circuit are discussed.

A3.6 (PUB. 9) ESD Pulse Width Effect on RC-Triggered NMOS With Power On or Off

Xinyu Zhu, Fangjun Yu, Hongyu Shen, Zekun Xu, Shurong Dong, Zhejiang University

The robustness of RC-triggered NMOS clamp in 28nm process is significantly reduced under the condition of long pulse width and power on. The simulation results show that the device faces the risk of turning off in these two cases, and the simulation results are in line with the test results.

Session E1: 14:00 - 16:55

E1: ESD Manufacturing and Factory Control

Moderator: Marcus Koh, Everfeed Technology Pte Ltd

E1.1 Factory Static PCBA Failure, Control and Solution Case Study

Shengzong He, China Saibao Laboratory

This presentation includes the following: 1) implementation requirements of PCBA factory ESD protected area; 2) apply static control grounding, 3) articulate typical non-compliance of EPA operators increasing ESD risk, 4) static control solutions for EPA.

E1.2 How do I get my Manufacturing Site ANSI/ESD S20.20 Certified?

Bernard Chin, Qorvo

The author will articulate the following: 1) Provide challenges and factors to consider when ANS/ESD S20.20 on-site certification is required; 2) Establish an enhanced quality management system beyond ANSI/ESD S20.20 requirements; 3) Review some of the potential improvements to ANSI/ESD S20.20

E1.3 (PUB. 23) EOS/ESD Manufacturing Mitigation Review

L.H. Koh, K.Y. Loh,Everfeed Technology Pte Ltd; Bernard Chin, Qorvo International Pte Ltd

This paper serves to review the typical EOS/ESD manufacturing issues from component level to system level for ESD sensitive devices (ESDS). The automated testing handling equipment impact on ESDS component failure will be articulated. ESDS failure on printed circuit board assembly is included too.

E1.4 Electronic Manufacturing Process ESD System Upgrade

Haibei Zhang, Shenzhen Kaifa Technology Co., Ltd.

Starting from the example of upgrading the organization ESD system control process, it is necessary to have new methods and ideas for static control in the new era. The ESD control system is transformed from manual detection to real-time.

E1.5 The Impact of ESD on PCBA and Protection

Figo Lu, Dell

This invited talk will cover the following areas: 1) ESD basic measuring instruments and methods, 2) ESD measurement standards, 3) ESD impact on PCBA quality, 4) PCBA processes effectively protect ESD, 5) New EE material design enhances ESD protection.

E1.6 (PUB. 21) High Temperature Resistant ESD Mats for PCB Bake Tray Usage

Andrew Mittermiller, Zhiyi Bao, Zeon Chemicals

High temperature resistant materials are required more often in electronic industry, especially for PCB baking tray liners, which are used repeatedly at high temperature as 150C. The paper will explore various polymer choices for ESD mats, and their comparison on heat resistance and other related properties.

Workshop A 17:00 - 18:00

A.1 ESD Protection for RF Applications

Moderator: Nathaniel Peachey, Qorvo

An ever increasing number of consumer products include RF functionality. From an ESD protection and robustness perspective, the RF circuit provides unique challenges for the designer. At the IC level, on-chip ESD protection must be balanced with performance requirements. At times, performance requirements limit the ESD protection level that can be achieved. Furthermore, advanced ESD co-design of ESD protection and RF functionality may be necessary. At the consumer product level, however, ESD protection cannot be compromised. Thus the system level designer has the challenge of designing a high-performance electronic product while still meeting the IEC61000-4-2 requirements for product qualification. This workshop will provide a forum to discuss and debate the various design and performance issues related with robust ESD design for RF IC's and consumer products.

A.2 Can Robust ESD Design be Achieved and Verified Using IEC 61000-4-2 Testing?

Moderator: David Pommerenke, IEEE Fellow

To introduce the topic a brief summary will be given on IEC 61000-4-2 ESD testing, and aspects of robust design. The discussion will be initiated using the following questions:

- Which methods are used in mechanical, electrical and software design to obtain ESD robust design?
- Which methods are used in design review to identify possible flaws in a designs?
- Which problems have been observed with respect to reproducibility of IEC testing?
- Which methods have been applied to improve reproducibility?
- How should the test standard be improved?

Workshop B 17:30 - 18:30

B.1 High Voltage ESD Protection Effectiveness and Efficiency - From Component Level to Whole Chip Solutions

Moderators: Prantik Mahajan, Jack Zeng, GLOBALFOUNDRIES

In the IoT era, High voltage technologies are gaining more and more traction spanning a wide range of market segments, while ESD protection for High voltage applications is becoming more and more challenging – constrained by cost, effectiveness of protection and safety concerns.
In this discussion group, let's come together to find out effective and efficient ESD protection solutions, encompassing device and circuit co-design. What is the specific requirement for High voltage ESD devices from chip to system level (considering SOC design requirements)? Discussions regarding High voltage ESD Design Window and SOA boundary of baseline device are welcome. Some brainstorming pertaining to the need for defining Figure Of Merit (FOM) for High voltage ESD devices and what could be a reasonable FOM for each type of ESD device, is encouraged. What kind of High voltage ESD device library is preferred by ESD circuit designer considering FOM of different types of ESD devices? The discussion will also cover design trade-off between effectiveness and efficiency of High voltage ESD protection – low holding voltage vs high holding voltage, snapback vs non-snapback devices and a plethora of other open issues including, but not restricted to, modeling the snapback region of certain ESD device operation.

B.2 Challenges and Opportunities in Manufacturing ESD Control

Moderator: Marcus Koh, Everfeed Technologies Pte Ltd

China is a big manufacturing country, where export of mobiles, computers, LCD TVs and so on takes a large proportion in their total exports and plays an important role in the global overseas trade. It is predicted that, in the coming years, this proportion will become larger and the export of electronic information products will be near USD 1,000 billion (1). The growth of China's market will be faster than that of the global market, with GAGR of 10% and in 2023, the value of China's electronic manufacturing services (EMS) in the global market is supposed to break USD 500 billion.
However, inappropriate manufacturing electrostatic discharge (ESD) control will inadvertently impact on products' yield and compromise on EMS market value. ANSI/ESD S20.20 and IEC-61340-5-1 are the recognized EMS ESD control best practices, which can help to enhance products' yield and sustain EMS market value. This session attempts to articulate if better understanding and enhanced manufacturing ESD control best practices from back-end semiconductor assembly, printed circuit board assembly to fully assembled system, could mitigate semiconductor devices' on-chip ESD target reduction.

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