# EOS/ESD Association, Inc
# Japan Electronics and Information Technology Industries Association

# China ESD Forum Workshop
# October 21-22, 2019

## Canmax, 99 Shuangma Street, Suzhou Industrial Park, Jiangsu, Suzhou, China

This annual one-of-a-kind workshop/forum to bring forth the realities of ESD requirements in light of the rapidly advancing semiconductor technologies requiring higher speeds of operations while balanced with much improved worldwide ESD factory control at fabs and assembly areas. It is designed to be a two-day event to bring together key customers and IC quality managers to learn and exchange information about the current issues of ESD requirements, and facilitate all to harmonize towards common goals for product cost savings.

The Forum this year will emphasize the continued development of device and system level ESD co-design. The use of TLP characterization for the development of behavioral models will be explored in greater depth than in previous years. Also, models for specific components such as the TVS device will be discussed. After attending these workshops, the attendee should have a better understanding of the development of both quasi-state and dynamic models that are needed for the system level ESD simulation.

Expert panel discussions provide intensive discussion and analysis that leads to valuable problem-solving exchanges.

**The workshop will address:**

- Design Challenges for IC ESD Protection
- HBM/CDM Testing and their correct standards implementation
- Transmission Line Pulsing set-up and test conditions
- Implementation on SOC levels
- RF, HV, and mixed signal concepts
- ESD Control relating to an EPA and specific measurements to control CDM events
- System Design focusing on parameters of soft and hard fasil immunity
- Disconnects between device and system level protection
- Development of TLP models
- System Efficient Design, models and co-design
- System ESD stress related to ports and charged board events

October 21, 2019

- ESD design concepts and testing methods for ICs

October 22, 2019

- System-Level ESD protection and SEED: characterization and protection methods for hard an soft fails

*Instructors + Panel: Harald Gossner, Intel; Nathaniel Peachey, Qorvo, Inc.; David Pommerenke, University of Missouri-Rolla; Bernhard Stein, Joost Willemen, Infineon Technologies; Nobuyuki Wakai, Toshiba; Hiroyasu Ishizuka, Synaptics.*

Co-Sponsored by:

The event is sponsored by JEITA, Industry Council on ESD Target Levels, and EOS/ESD Association, Inc., co-sponosred by JEDEC.

11 July 2019 12:38 pm

**www.esda.org/events**

Setting the Global Standards for Static Control!

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# Meet the Instructors

**Harald Gossner** is Senior Principal Engineer at Intel. He received his degree in physics (Dipl. Phys.) from the Ludwig-Maximilians-University, Munich in 1990 and his Ph. D. in electrical engineering from the Universität der Bundeswehr, Munich in 1995. For 15 years he has worked on the development of ESD protection concepts with Siemens and Infineon Technologies. In 2010 he has joined Intel Mobile Communications overseeing the development of robust mobile systems. Harald has authored and co-authored more than 100 technical papers and two books in the field of ESD and device physics. He holds 50 patents on the same topic. He received the best paper award of EOSESD 2005 and 2012. Regularly he is lecturing tutorials at ESREF, IRPS and EOSESD symposium. He has served in technical program committees of IEDM, EOSESD Symposium and International ESD Workshop and is member of the board of directors of ESD Association. In 2006 he became cofounder and co-chair of the Industry Council on ESD Target Levels.

**Nathaniel Peachey** received his PhD in physical chemistry in 1994 from the University of Nebraska–Lincoln and then was awarded a director's funded postdoctoral fellowship at the Los Alamos National Laboratory; where he studied thin-film membranes for gas separation. In 1996, he joined Atmel Corporation in Colorado Springs as a thin-films process engineer. Over the next several years Dr. Peachey held various positions at Atmel including process engineer, technology development engineer, device engineer, and circuit design engineer. In 2003, he began focusing exclusively on ESD protection and I/O design issues. In 2005, Dr. Peachey accepted the position of engineering manager for the newly formed ESD design group at RF Micro Devices (currently Qorvo, Inc.). In this capacity, he was responsible for the development of ESD protection for all the technologies that Qorvo designed including both silicon and GaAs. Besides on-chip protection he led the development and improvement of the RF antenna ESD protection. Dr. Peachey has authored and coauthored over 30 technical journal submissions. He has also submitted 14 patents that have either been granted or are pending. Dr. Peachey is also a senior member of the IEEE. In 2009, Dr. Peachey was elected to the board of directors for EOS/ESD Association, Inc. He has been involved in various activities within EOS/ESD Association, Inc. Currently, he is serving as the Standards Business Unit Manager.

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**Dr. David Pommerenke**'s research interests are system level ESD, electronics, numerical simulations, EMC measurement methods, and instrumentations. He received a PhD from the Technical University Berlin in Germany in 1996. After working at Hewlett Packard for 5 years he joined the Electromagnetic Compatibility Laboratory at the Missouri University of S&T in 2001; where he is a professor. He has published more than 200 papers and is an inventor on 13 patents. His main research interests are measurement/instrumentation ESD and EMC. He is a senior IEEE member and associated editor for the IEEE Transactions on EMC. He is an IEEE fellow.

**Bernhard Stein** is Principal Engineer at Infineon Technologies. He received his degree in physics (Dipl. Phys.) from the Ludwig-Maximilians-University, Munich in 1999 and received his PhD in Physics also from the Ludwig-Maximilians-University in Munich 2004. He has joined Infineon Technologies in 2005 working on ESD/LU development and application engineering. Since 2011 he was leading the ESD/LU development as well as ESD/LU application engineering at Intel Mobile Communications. In 2016 he moved to product development as director of Analog-RF design for mobile transceivers. Since 2019 he is Principal Engineer for ESD at Infineon Technologies. He received the best paper award of the EOSESD symposium in 2012

**Joost Willemen** received a master's degree and PhD in electrical engineering from DIMES Institute, Delft University of Technology, Delft, The Netherlands, in 1993 and 1998, respectively. In 1998, he joined the automotive electronics division, Robert Bosch GmbH, Reutlingen, Germany; where he developed methodologies for human body model and conventional delay model circuit-level simulation, high-current electrostatic discharge (ESD) device models, and a simulation environment for fully coupled electrothermal circuit simulations. In 2005, he joined smart power technology R&D, Infineon Technologies AG, Munich, Germany. His main tasks are the development of ESD concepts and devices for automotive applications and ESD consultancy for automotive IC design. His research interests are the physics of ESD devices and advanced ESD characterization methods.

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**Nobuyuki Wakai** received BS degree in applied physics and Master course in crystallography engineering from Nagoya University, Aich, Japan, in 1991 and 1993, respectively. In 1993, he joined Toshiba Corporation which is currently Toshiba Electric Devices & Storage corporation and he is now working for it. From 1999, he additionally joined JEITA (Japan Electronics and Information Technology industries Association) committee activities to make standards for reliability test method and is currently working as chair of project group for both “ESD target level optimization” and “Soft Error testing”. Former one has a purpose to collaborate with ESD-industry-council also. From 2000, he started IEC (International Electrotechnical Commission), and now vice chair of TC47 (Semiconductor devices)/WG2 (Reliability test method), chair of WG5 (Wafer level reliability test method) and member of TC101 (Electrostatics)/WG5 (Protection of electronic devices against static electricity). ESD test methods were included as items in TC47/WG2 and TC101/WG5, respectively. Since 1993, he worked about all of reliability matters consisted of failure mechanism, failure analysis, test method and statistical consideration for analog and digital semiconductor devices. He is now general manager of Quality and Reliability Engineering Department of System devices division in Toshiba Electric Devices & Storage Corporation

**Hiroyasu Ishizuka** received BS degree in electrical engineering from the Shibaura Institute of Technology, Tokyo, Japan, in 1983. He is in a doctoral course at the Tsukuba University now. In 1983, he joined Hitachi Yonezawa Electric Corporation. In 1994, he joined Hitachi Microcomputer System Ltd. In 2003, he joined Renesas. Since 1992, he worked on the development and design group of ESD protection devices/circuits, and he was a manager while he worked in Renesas. His working area are very wide, from advanced CMOS technologies to mixed signal/analog technologies, from high voltage devices techniques to high speed IO/ESD design techniques, also he covers component level ESD, system level ESD, ESD control, testing, ESD analysis techniques and ESD design verification. From 2012, He was working as a technical consultant on ESD design methods and ESD qualification support in RCJ (Reliability Center for Electronic Components of Japan). Since 2015, he is working on driver IC ESD design and panel/phone system ESD consultant in Synaptics Japan, he is very interested in to study system ESD phenomena under system ESD testing and real-world ESD behavior. He authored and co-authored more 20 publications in technical journals and conferences and holds more 10 patents in the field, and he is a chief RCJ ESD coordinator, ESDC-11-0105. He is a recipient of the best paper award twice from the RCJ EOS/ESD/EMC Symposium (1996 and 2007), friendship award twice from the ESDA (ESD Association) EOS/ESD Symposium (1997 and 2007). He served as the TPC (Technical Program Committee) for the ESDA ESD Symposium (2008-2012 and 2017) and the Asian chair for ESDA IEW (International ESD Workshop) (2009-2011). He was a core-member of the Industry Council on ESD Target Levels from 2006 to 2012, since 2013, he is an associate member in it. In JEITA (Japan Electronics and Information Technology Industries Association), he is a core member of ESD WG and he is a chair of system ESD analysis WG. Adding he is a member of ESDA and IEICE (The Institute of Electronics, Information and Communication Engineers).

# REGISTRATION

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Last Name:_____ First Name:_____

Company Name:_____

Street:_____ City:_____

State/Province:_____ Country:_____ Zip/Postal Code:_____

Phone:_____ Fax:_____ Email:_____

☐ **China ESD Forum Workshop October 21-22, 2019** 4588 CNY / 680 USD

•Limited to the first twenty (20) completed registrations

Cancellation & refund requests will be considered if received in writing no later than August 20, 2019, and are subject to a $50 fee. Any other approved dispositions will also be assessed a $50 fee.

Credit card number:_____ Security code:_____

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**http://www.cvent.com/d/9yqld2**

**Phone: +1 (315) 339-6937**

**Email:** info@esda.org

## For other forms of payment Contact:

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wangrui@canmax.com.cn

**English :** Joanna Huang

+86 (512) 6285 2258

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Simultaneous translation avaiable for the tutorials!

## Accommodations:

Hotel Name

Hilton CNY 830/night

Genway International CNY 500/night

Atour Hotel (Qingjian Lake) CNY 380/night

The cooperate account we have in Hilton is 113120308, please use it for room reservation.

http://doubletree3.hilton.com/en/hotels/china/doubletree-by-hilton-hotel-suzhou-SZVTVDI/index.html