2020 International ESD Workshop (IEW)

May 4-8, 2020

Tagungshotel Jesteburg, Hamburg, Germany

14th Annual International Electrostatic Discharge Workshop

Now in its 14th year, the IEW continues to provide a relaxed, invigorating atmosphere to present new work and engage in discussions about the latest issues confronting the ESD and EOS communities. The workshop will include a tutorial, invited seminar speakers, discussion groups, invited talk speakers, technical presentation sessions, and special interest groups. The IEW is the perfect opportunity to submit late-breaking and exciting new research to stimulate discussion and interaction around new ideas, encouraging new research topics. To maintain the unique IEW experience and provide ample opportunity for discussion, there will be an increased focus on discussion groups and invited speakers in 2020. The IEW workshop presentation format for technical sessions will begin with each author presenting a brief summary to highlight key findings, followed by an interactive poster-based discussion session among authors and attendees. The IEW is closely aligned with the EOS/ESD Symposium for collaborative conference activities.

DON'T MISS THE DEADLINE!

October 11th, 2019

People's Choice Award will be presented to a poster chosen by attendees.

Submission Instructions

Submission instructions and an abstract template are available at https://www.esda.org/index.php/events/iew/. The submission is in PowerPoint format and is no longer than 6 slides. Submissions are due October 11, 2019 to iew@esda.org. There will be no published proceedings of IEW. Walk-on posters are also permitted at IEW with no prior review, but only those works which are submitted for review and acceptance will be included in the five-minute teaser presentation sessions.

FOCUS TOPICS FOR IEW 2020

ESD Soft Failures

The shrinking feature size of ICs and the increasingly complexity of electronic systems lead to a higher susceptibility to soft failures, such as unwanted bit errors, application crashes and system resets. Evaluation of the robustness against ESD/EMC/EMI induced malfunction is not easy. Finding the root cause of soft failures can be time consuming. Exchange your evaluation methodologies, test strategies, root cause analyses and best practices with other ESD experts.

Challenge of fully depleted SOI technology

Fully depleted SOI is a technology with underutilized capacities. It offers a path to downscaled, high performance RF circuits and high gate density. Yet, its ESD features have not been widely considered in the literature. Also the unexpected feature of latch-up in a SOI technology due to the back gate diffusions has not been highlighted. IEW 2020 dedicates a focus to this technology asking for poster contributions and offering discussion groups. Join and share your experience.

New Insights into CDM

There are discussions ongoing concerning new stress methods like the Low Impedance Contact CDM or the Capacitively Coupled TLP which are related to the CDM. What will be the challenges for future CDM testing? Is it sufficient just to look on the stress peak current only? What are the rise time requirements for CDM measurements or which kinds of packages do we have to test? Share your experiences with the community and influence the development of new methodologies.

Other topics and areas to consider for abstract submissions including but not limited to:

Anomalous/Unresolved ESD Issues
Random and unrepeatable ESD failures, case histories, ESD tester correlation issues, and unique window failures.

ESD Big Data
Summarizing and viewing large ESD and latch-up tester datasets. Mapping design data to ESD and latch-up test programs.

System-Level ESD Issues
On- and off- chip IEC protection clamps, component/system ESD co-design case studies, cable discharge clamps, transient latch-up, design of system-level clamp circuits, system-level ESD test issues and scan techniques, and ESD-induced soft errors.

Failure Analysis Techniques
Locating failure sites, in particular for CDM, imaging techniques, correlating FA identified damage site with ESD stress, distinguishing EOS-like failures from ESD failures, and unusual failure modes.

EDA Tools
EDA verification and simulation tools; techniques, design-flows, best practices, experiences with foundry rule decks, commercial tools, and custom tooling.

Electrical Overstress (EOS)
Root-cause analysis on a failure with an electrical induced physical damage (EIPD) signature, methodology for defining AMR for a product and verifying it for different timescales, and case studies identifying EOS damage mechanisms and the ensuing physical evidence.

ESD Control
ESD protection targets versus ESD control measures

Novel On-Chip Protection Clamps and Circuit Configurations
New clamp devices and clamp configurations, methods to increase the failure threshold of protected devices, high voltage clamps for automotive and power amplifiers, new chip protection concepts, and low-capacitance clamps for RF and high speed interfaces.

ESD Test Characterization, Methods, and Issues
TLP & VF-TLP debug and device characterization methods, correlation of TLP & VF-TLP tests with standard qualification tests, HBM and CDM tester artifacts, unresolved test results and failures, issues relating test qualification levels to real-world exposure, test chip methodology, cable discharge test methods, and test standards issues.

Technology Integration Issues
ESD sensitivity with technology transfers, 3D IC ESD design issues, qualification challenges for different fabs, unusual problems of process interaction with ESD, process monitor methods, and technology scaling issues.

Mark Your Calendar!

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