| | Time | Session | Content | Speaker |
|---|---|---|---|---|
| Monday, October 21, 2019 | 9:00 – 9:15 | Welcome | ESDA activites in China and important international ESD events are announced | Lisa Pimpinella |
| | 9:15 – 10:00 | IC Design | Design challenges for IC ESD protection providing the essential knowledge of on chip ESD protection design. The general aspects of IO protection, power protection and the SOC level ESD connectivity will be discussed. | Bernhard Stein/Harald Gossner |
| | 10:00 - 10:30 | IC Testing | HBM/CDM testing are the relevant testing standards for qualification of Ics and ESDA/JEDEC/ANSI standard JS001- and JS-002 are the the widely used standards for HBM and CDM qualification. The content of the standards and their correct implementations will be presented. | Nate Peachey |
| | 10:30 – 10:50 | Coffee break | | |
| | 10:50 – 12:15 | IC Testing | Transmission Line pulsing (TLP) is the tool of choice for ESD teststructure analysis as well as for characterization of IO pins in terms of their system ESD robustness. Transient analysis of the waveform as well as quasi stationary IV extracted from TLP are the base of design decisons for on chip ESD protection design. The set-up and test conditions for TLP will be shared and the variants of very fast (vf) TLP and charge couple (cc) TLP will be discussed. | Nate Peachey |
| | 12:15- 13:45 | Lunch Break | | |
| | 13:45 – 14:45 | IC Design | An ESD protection concept relies on a proper implementation of a top level ESD protection network. The implementation on SOC level will be presented and representative circuit types of IO protection will be shown. | Bernhard Stein/Harald Gossner |
| | 14:45 – 15:15 | IC Design | While digital general purpose IOs can be protected with widely known standard ESD concepts with very little constraints from circuit performance side, mixed signal ESD protection often requires careful co-design of ESD protection with circuit design. Examples of various RF, HV and other mixed signal concepts will be shared. | Bernhard Stein/Harald Gossner |
| | 15:15 – 16:00 | ESD control | The IC manufacturing, testing and handling has to occur in an ESD protected area (EPA). An overview of the implentation of an EPA following the standard of ESDA S20.20 and the specific measures to control CDM events in EPA are discussed. | Hiroyasu Ishizuka |
| | 16:00 – 16:20 | Coffee Break | | |
| | 16:20 - 17:00 | Panel | Q&A session | |

| | Time | Session | Content | Speaker |
|---|---|---|---|---|
| Tuesday, October 22, 2019 | 9:00 – 10:00 | System Design | Systemlevel Esd Design poses multiple design challenges to IC and board design. Also firmware and software strongly influence the system robustness. The various parameters influencing the soft and hard fail immunity will be discussed and a design guidance wil be shared. | David Pommerenke |
| | 10:00 - 10:30 | System Testing | Cover the proper implementation of the IEC61000-4-2 test. This might include a video showing the actual testing. Include the proper interpretation and analysis of test results. Also discuss the disconnect between device level and system level protection. | David Pommerenke |
| | 10:30 – 10:50 | Coffee break | | |
| | 10:50 – 12:15 | System Design | System Efficient ESD Design (SEED) will be introduced and will explain the fundamentals of system-level co-design. This workshop will also cover the conceptual aspects of SEED regarding hard and soft fail. The workshop will also describe the development of models using the TLP. | David Pommerenke |
| | 12:15- 13:45 | Lunch Break | | |
| | 13:45 – 14:45 | System Design | The base for SEED is the accurate TVS diode characterization and modelling. Recent standardization activities as well as engagement of TVS vendors have driven this to a elevated level allowing it to be used for system design assessment. The characterization and modelling approaches will be presented from the perspective of an TVS vendor. | Joost Willemen |
| | 14:45 – 15:15 | System Design | To introduce the application of SEED an example for a hard fail IC/PCB protection codesign based on TVS and IO models will be shown. | Joost Willemen |
| | 15:15 – 16:00 | Reald world ESD for Systems | Subsystems and boards are handled in various manufacturing environments which can lead to various types of ESD stress. The discussion covers system ESD stress to system ports and charged board event leading to hard fails. | Nobuyuki Wakai |
| | 16:00 – 16:20 | Coffee Break | | |
| | 16:20 - 17:00 | Panel | Q&A session | |