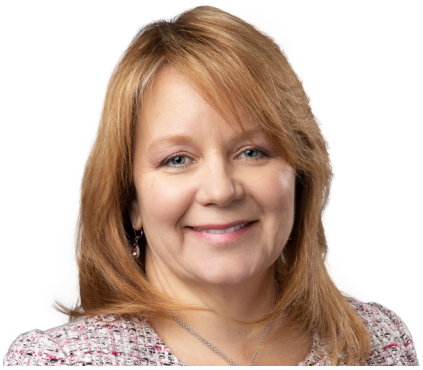
Seminar 1
ESD Solutions for RF Applications

Kathleen Muhonen,, Qorvo

Abstract
While designing circuits for complex applications can be challenging, RF circuits present additional requirements on the designer. Not only are these circuits very sensitive to ESD threats, but adding ESD protection will invariably compromise performance. Thus, in most cases, the design of functionality and ESD protection must be done as co-design. This seminar will address the various aspects of advanced ESD design. This will then be extended to RF applications and ESD co-design. Finally, this seminar will discuss various case studies to illustrate the principles presented.

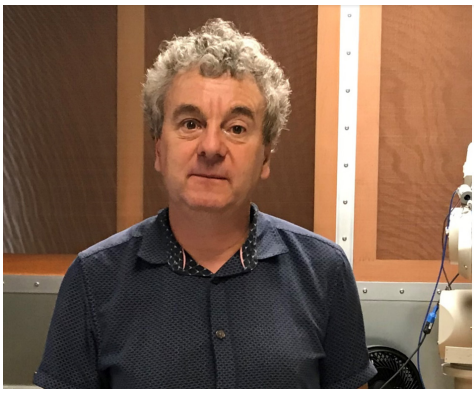


Biography
Kathleen Muhonen is currently an ESD Engineer at Qorvo in Greensboro, NC. She is involved in ESD on-chip protection for mobile and millimeter wave applications. Kathleen is heavily involved with system level testing and helped standardize IEC testing of RF components and in ESD instrumentation for better ESD characterization of clamps and materials. Previously she was responsible for RF characterization and model support for SOI and GaAs technologies for power amplifiers, switches and antenna tuners. She has also done extensive work on developing state of the art harmonic characterization of semiconductors, breakdown models for SOI FETs and improving de-embedding techniques of large-scale switches. Kathleen's previous experience includes assistant professor at Penn State Erie, linearization design for base stations at Hewlett Packard and power amplifier design at Lockheed Martin and GE Aerospace.
Kathleen is a member of the ESD Association and sits on all device testing standards committees, including serving as past TLP and HMM workgroup chairs. She has also served on the Board of Directors and is involved in the education committee for the ESDA. Her involvement in round robin testing for TLP, VF-TLP and IEC Component Testing has generated several papers presented at the EOS/ESD Symposium over the last decade.
Kathleen received her BSEE degree from Michigan Technological University in 91, a MSEE from Syracuse University in 94 and a Ph.D.EE from Penn State University in 99.

Seminar 2
Quantifying System Level ESD and Protecting I/O

David Pommerenke, IEEE Fellow

Abstract
This seminar will describe the different entry paths of ESD into a system, such as the breakdown through gaps in the plastic, the corona induced currents from discharges to displays, and the discharges into I/O such as USB. This will enable engineers to quantify the threat for the different entry paths, and base design guidelines on this information. In the second, part this seminar will explain the System Efficient ESD Design strategy that allows to design efficient protection even for 10 GHz+ I/O based on simulation. The simulation needs transient models for the TVS diodes and models for the ICs. It is shown how these models are obtained and how the simulation is performed. The last part of the seminar will show how to even reduce the likelihood of soft-failure on I/O, such as USB by selecting protection elements based on simulation.



Biography
Dr. David Pommerenke received his diploma and PhD from the Technical University Berlin, Germany. His research interests are system level ESD, electronics, numerical simulations, EMC measurement methods and instrumentation. He worked at Hewlett Packard for 5 years before joining the electromagnetic compatibility laboratory at the Missouri University of S&T in 2001. Dr. Pommerenke became the CTO of ESDEMC in July 2019 before joining the ESD/EMC group at the Technical University of Graz in Austria in January 2020. His new focus is on ESD, EMC, harmonics, and PIM. He has published more than 200 papers and is inventor on 13 patents. His main research interests are measurement/instrumentation ESD, electronic design and EMC. He is IEEE fellow and associated editor for the IEEE Transactions on EMC.

He can be reached at david.pommerenke@ieee.org

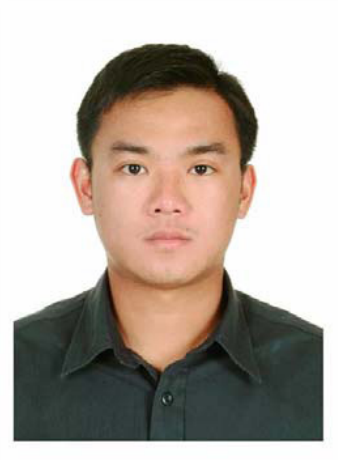
Seminar 3

Towards Optimal ESD Protection Diodes in Advanced Bulk FinFET and GAA Technologies

Shih-Hung Chen, imec

Abstract

As CMOS technology nodes scaling beyond 20nm, bulk FinFET (FF) has become the mainstream technology in mobile and computing applications. ESD reliability is strongly impacted by not only the geometry scaling, but also by newly introduced process options in the advanced bulk FinFET technologies. To further enhance function transistor performance, a gate-all-around (GAA) architecture has been proposed as a promising candidate in sub-5nm CMOS technology nodes. This new device architecture with new process options can bring further challenges of ESD reliability. In this seminar, we will look at the influence of the device architectures and the corresponding process options on ESD device characteristics in the FinFET/GAA NW technologies. 3D TCAD simulations bring an in-depth physical understanding of the ESD current conduction and failure mechanism in the ESD protection diodes.



Biography

Shih-Hung Chen received the PhD degree from the Institute of Electronics, National Chiao Tung University, in 2009. In 2002, he joined the ITRI, Hsinchu, as an ESD Engineer. Since 2010, he has been with Device Reliability and Electric Characterization (DRE) Group at imec, as a senior ESD researcher. He authored or co-authored more than 100 conference and journal publications. He has served as a TPC member in IEEE IRPS since 2016, and in EOS/ESD Symposium since 2014. His current research interests include ESD protections in sub-10nm technologies, in 3D/2.5D IC applications, and in STCO with the integrations of III-V materials.

Seminar 4
Introduction to ESD Design in High Voltage Technologies

Filippo Magrini, Infineon

Abstract
This seminar gives an introduction to ESD design in high voltage technologies for integrated circuits with pin voltages from 12 volts upwards. After a short introduction of typical applications and requirements, an overview of different technologies and the typical device portfolios in these technologies will be given. Different ESD protection concepts are introduced, analyzing advantages and disadvantages of the various possible approaches to implement ESD networks (diodes, snapback, active clamps…). Finally, HV-technology and design related challenges regarding ESD protection are discussed, with a special focus on relevant case studies.

Biography
Filippo Magrini was born in Parma, Italy. He received his M. Sc. degree in electronic engineering from the “Universitá degli Studi di Parma” in 2007, discussing a thesis on numeric simulations of power PiN diodes. In 2008, he joined the automotive power technology development department of Infineon Technologies where, since then, he has been responsible for the development of ESD protection devices and concepts in advanced Smart Power technologies. In the latest years, his focus has addressed reverse engineering topics, the development of HV-SCRs and the investigation of discrete MOSFETs’ dynamic behavior. His responsibilities also cover the support of design teams with respect to the implementation of robust on-chip ESD protection design. Filippo has authored and co-authored several papers published at international ESD and EMC conferences. He received the EOS/ESD Symposium best paper award in 2011.

KEYNOTE

Advanced ESD Design Facilitated by Circuit Simulation

Elyse Rosenbaum, Melvin and Anne Louise Hassebrock Professor in Electrical and Computer Engineering, University of Illinois at Urbana-Champaign

Technology scaling has made integrated circuits more vulnerable to ESD-induced damage, but that same scaling allows CMOS circuits to operate at unprecedentedly high data rates. For example, the IEEE 802.3bs standard for 400 Gb/s Ethernet specifies a per-lane bit rate of 53.125 Gb/s. Providing the necessary on-chip protection without compromising the circuit performance is more difficult than ever before. It can be assumed that there is only a small design window in which both performance and reliability specifications can be met, and circuit simulation will be a critical tool for executing the challenging circuit design. The simulation netlist must include the ESD protection devices, and those devices must be represented by models that are accurate under both normal operating conditions and high-current ESD conditions. This talk will start with an overview of state-of-the-art ESD protection for high-speed and RF IO pins. Next, the requirements for ESD models will be identified and the shortcomings of current models will be described.

Elyse Rosenbaum is the Melvin and Anne Louise Hassebrock Professor in Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. She received a PhD in electrical engineering from University of California, Berkeley. She is the director of the NSF-supported Center for Advanced Electronics through Machine Learning (CAEML), a joint project of the University of Illinois, Georgia Tech and North Carolina State University. Her current research interests include machine-learning aided behavioral modeling of microelectronic components and systems, compact models, circuit reliability simulation, component and system-level ESD reliability, and ESD-robust high-speed I/O circuit design. Dr. Rosenbaum has authored or co-authored nearly 200 technical papers; she has been an editor for IEEE Transactions on Device and Materials Reliability and IEEE Transactions on Electron Devices. She was the recipient of a Best Student Paper Award from the IEDM, Outstanding and Best Paper Awards from the EOS/ESD Symposium, a Technical Excellence Award from the SRC, an NSF CAREER award, an IBM Faculty Award, and the ESD Association's Industry Pioneer Recognition Award. She is a Fellow of the IEEE.

Feature: EOS/ESD Association, Inc. Symposium Award Paper

A1: Advanced CMOS, ESD Modeling and Simulation

Moderator: Yuan Wang, Peking University

A1.1 Novel Dual-Diodes for Rail-Based On-chip ESD Protections

Zhong Chen, Hui Wang, Pengyu Lai, University of Arkansas

Rail-based ESD network has been widely implemented for on-chip ESD protection. Innovative approach will be presented to utilize parasitic components in these dual-diode ESD structures for many applications such as high-speed interface ICs, MCU, RF, etc. Area-efficient dual-diodes can be integrated with different types of primary ESD structures to reduce adverse impacts on the circuit performance and meet specific pin requirements. In addition, this novel structure can alleviate design challenges due to system-level ESD requirements on ICs.

A1.2 WITHDRAWN

A1.3 (PUB.1) Design of A New Low Voltage Triggered Silicon Controlled Rectifier(SCR) for ESD Applications

Wenqiang Song, Feibo Du, Fei Hou, Jizhi Liu, Zhiwei Liu, IEEE; Juin J. Liou, IEEE; Shenzhen University

In this paper, a new low-voltage triggered silicon-controlled rectifier (NLVTSCR) with low trigger voltage and higher holding voltage is proposed and implemented in a 28nm CMOS process. The proposed NLVTSCR in the TLP test has a low trigger voltage and an adjustable high hold voltage from 3.44V to 4.93V. In addition, it does not require any additional masks, making it an excellent candidate for 3.3V ESD protection. Compared to conventional low triggered voltage silicon-controlled rectifier (LVTSCR), the proposed NLVTSCR device provides a higher holding voltage than its conventional counterpart.

A1.4 Study of ESD Device Modeling Based on Neural Network

Yize Wang, Yunhao Li, Yuan Wang, Peking University

Modeling method of electro-static discharge (ESD) devices based on neural network is introduced in this work. The new ESD models are scalable and can much reduce the complexity compared with traditional ones. All the modeling process and verification for the neural network model are shown in detail.

B1: ESD Protection in Bipolar, RF and High-voltage Applications

Moderator: Zhiwei Liu, UESTC

B1.1 Compact ESD Protection Cell for 5G Applications

Chun-Yu Lin, National Taiwan Normal University

Multiple millimeter-wave (MMW) frequency bands are considered for fifth-generation (5G) systems. A compact ESD protection cell by using an inductor with ESD protection devices to achieve the sufficiently small layout area, higher ESD robustness, and lower loss for 5G / multi-band MMW applications is presented in this work.

B1.2 (PUB.10) Design Optimization of High Voltage NPN ESD Protection Device in 130nm Power SOI Technology

Raunak Kumar, Jie (Jack) Zeng, Kyong Jin Hwang, Robert Gauthier Jr, GLOBALFOUNDRIES

A HV NPN ESD devices is evaluated in a 130nm Power SOI technology. Current flow and temperature distribution under ESD stress is investigated by TCAD and a new device architecture without STI is proposed. Non-uniform triggering issue is also investigated. Segment type layout design shows uniform triggering of multi-finger devices.

B1.3 (PUB.11) Optimization of GGNMOS Devices for High-Voltage ESD Protection in BCDLite Technology

Prantik Mahajan, Raunak Kumar, Robert Gauthier, Kyong Jin Hwang, GLOBALFOUNDRIES

Design optimization of Electrostatic Discharge (ESD) GGNMOS for high-voltage applications in low-cost BCDLite technology is presented. Clamp performance optimization through body PWELL engineering and device design techniques are investigated. A comparative analysis between two distinct device architectures (different Poly-LOCOS overlap) showing 100ns TLP measurement and TCAD simulation results is presented.

B1.4 (PUB. 12) DDSCR Device Structure Fabricated on 0.5μm CMOS Process

Xiangliang Jin, Yang Wang, Hunan Normal University

Dual Direction Silicon Controlled Rectifier(DDSCR) are primarily used for ESD protection in high voltage environments. According to the results of the device test, the trigger voltage and the sustain voltage of the DDSCR are 17.62V and 9.54V, respectively. Finally, by changing the important dimensions of the DDSCR, the ESD characteristics of the device can be significantly improved.

Technical Sessions: C1

C1: ESD Tester and ESD Testing

Moderator: Shurong Dong, Zhejiang University

C1.1 Consideration on Discharge Waveform of GND Relay Free System of High pin count ESD Tester

Masanori Sawada, Haruki Nakao, Hideaki Miura, Nobuchika Matsui, HANWA ELECTRONIC

Traditional ESD tester at the effect of parasitic capacitor in relay matrix, A-side and B-side waveform difference has been confirmed. To solve this problem, it reconsiders the relay base system and it proposes ESD tester with new structure for GND setting.

C1.2 TLP and vf-TLP Test Methods and Applications

Michael Reardon, Yingjie Gan, ESDEMC Technology LLC

This report explains the theory of TLP and vf-TLP test methods; the basic implementation of the TDR-O and TDR-S measure¬ment methods; typical applications of the methods; how to do a good measurements in terms of calibration and verification, probing fixture, TLP measurement repeatability; and other fre¬quently asked questions of TLP/vf-TLP measurement.

C1.3 WITHDRAWN

C1.4 CDM Measurement for Bare Dies and Wafers

Teruo Suzuki, Socionext

Resolving frequent ESD failures at an assembly house was time-consuming. Testing the robustness of the CDM in the wafer/bare die state would provide early information about problems with ESD design or electrostatic controls. With our new JS-002-compliant Wafer CDM tester, we tested products as wafers/bare dies to achieve the desired robustness.

C1.5 WITHDRAWN

Technical Sessions: D1

D1: System Level ESD

Moderator: Shurong Dong, Zhejiang University

D1.1 WITHDRAWN

D1.2 WITHDRAWN

D1.3 Direct Visualization of Breakdown Induced Metal Migration in Enhanced Modified Lateral Silicon-Controlled Rectifiers

Xinqian Chen, Chaolun Wang, Hejun Xu, Xin Yang, Xing Wu, East China Normal University; Feibo Du, Yuxin Zhang, Fei Hou, Zhiwei Liu, University of Electronic Science and Technology of China; Yongren Wu, Chihang Tsai, Zhirong Chen, Yurou Guo, Integrated Service Technology of Shanghai

Transmission electron microscopy (TEM), with its high spatial resolution and versatile external fields, is undoubtedly a powerful tool for the static characterization and dynamic manipulation of nanomaterials and nanodevices at the atomic scale. The rapid-development of thin-film and precision microelectromechanical systems (MEMS) techniques allows the microstructure during ESD to be probed and engineered inside TEM under external stimuli such as electrical andthermal fields at the nanoscale. Here, taking advantage of advanced in situ transmission electron microscopy, we manipulatedinterfaces of ESD. The progress of the in situ TEM paves the way to future nanodevices.

D1.4 Discharge Current Analysis of Charge Board Event and Consideration the Design Concept

Hiroyasu Ishizuka, Masanori Sawada, Synaptics HANWA ELECTRONIC

Analyzed the discharge current waveform of CBE(Charged Board Event) occurring in the system production line and the field, using mobile phone and panel module.
Main discharged current is characterized by very high speed rise time, narrow width and high current level without high energy, which indicates the need for a new design strategy to remove CBE failure.

D1.5 (PUB.20) Module and System Level ESD Co-Design and Simulation of Mobile Phone Antenna Systems

Yanlin Nie, Qiupei Huang, Zhiwei Liu, Jizhi Liu, University Of Electronic Science and Technology Of China; Xiang Li, Xiaofei Xie, Huawei Technologies Co., LTD.

In this paper the analysis of measurement pulse frequency effects on soft failure probability of DUT is presented. Different pulse intervals are implemented on a camera sub-system of a smartphone prototype. It is found that not only the pulse voltage but also the frequency affects soft failure probabilities.

Technical Sessions: A2

A2: Advanced CMOS, ESD Modeling and Simulation

Moderator: Yuan Wang, Peking University

A2.1 (PUB. 22) Design and Optimization of Diode Triggered Silicon Controlled Rectifier in FinFET Technology

Meng Miao, You Li, Robert Gauthier, Globalfoundries

Diode trigger SCR (DTSCR) structure is introduced in FinFET technology for low voltage circuit ESD protection. The current direction is chosen to flow across fins to make full use of the bulk silicon region. Further optimization of DTSCR is investigated to improve layout efficiency

A2.2 Investigation on Fabrication-Induced High-Leakage Issue of an Overdrive ESD Power Clamp in Advanced FinFET Technology

Guangyi Lu, Lihui Wang, Ling Wang, Xin Gao, Mei Li, Hisilicon Technologies Co., LTD

Fabrication-induced high-leakage issue of an overdrive ESD power clamp is presented. With silicon data exhibiting abnormal results, elaborate troubleshooting is performed and disclosed in this paper. Through alignments of silicon data and presumptive simulation results, fabrication-induced root cause is successfully revealed and confirmed by physical failure analysis (PFA) results.

A2.3 (PUB. 4) ESD Diode Devices Simulation and Analysis in a FinFET Technology

Yunhao Li, Yize Wang, Yuan Wang, Peking University

As CMOS scaling down to FinFET technology, the performance of ESD devices degenerate seriously. In this work, two types of ESD protection diodes, Gated Diode and STI Diode, are invested in 14nm FinFET technology. The corresponding 3D TCAD simulation result help to understand the working mechanism of ESD protection diodes.

A2.4 WITHDRAWN

A2.5 WITHDRAWN

A2.6 WITHDRAWN

Technical Sessions: B2

B2: ESD Protection in Bipolar, RF and High-voltage Applications

Moderator: Zhiwei Liu, UESTC

B2.1 (PUB. 13) Optimization of NPN ESD Protection Device for Improved Failure Current

Jie (Jack) Zeng, Raunak Kumar, Tsung-Che Tsai, Sevashanmugam Marimuthu, Robert Gauthier Jr, GLOBALFOUNDRIES

This paper present a high voltage NPN based ESD protection device with a designed PBL under collector region achieving 2.7X failure current improvement compared to structure without PBL in 130nm advanced BCD Technology. It has a flexible feature of tunable trigger and holding voltage without It2 degradation.

B2.2 (PUB 14) Optimized Local I/O ESD Protection for SerDes Interfaces In Advanced SOI, BiCMOS and FinFET Technology

Johan Van der Borght, Ilse Backers, Olivier Marichal, Bart Keppens, Koen Verhaege, Sofics

Semiconductor companies are developing ever faster interfaces to satisfy the need for higher data throughputs. However, the parasitic capacitance of the traditional ESD solutions limits the signal frequency. This paper demonstrates low-cap Analog I/Os for high speed SerDes (28Gbps to 112Gbps) circuits created in advanced BiCMOS, SOI and FinFET nodes.

B2.3 WITHDRAWN

B2.4 WITHDRAWN

B2.5 (PUB. 16) Verification of an Equivalent Circuit Model for LDMOS-SCR Based on 0.5μm CMOS Process

Zeyu Zhong, Xiangliang Jin, Hunan Normal University

Based on a LDMOS-SCR designed and manufactured in 0.5μm CMOS process, a SCR equivalent circuit model for ESD protection is applied and verified. Simulation results show a high consistency with the TLP I-V curve. It contributes to the simulation methodology of SCR devices for ESD protection.

B2.6 WITHDRAWN

A3: Advanced CMOS, ESD Modeling and Simulation

Moderator: Yuan Wang, Peking University

A3.1 WITHDRAWN

A3.2 Analysis of a Failure Case Related with Test System and Procedure

X. Huang, F. Liu, Chongqing Acoustic-optic-electronic Co. Ltd. of CETC & 24 Institute, University of Electronic Science and Technology of China; Y. Xiong , Chongqing Acoustic-optic-electronic Co. Ltd. of CETC & 24 Institute, Chongqing University; Z. He, W. Huang, C. Huang, X. Yang, L. Pu, L. Yao, Chongqing Acoustic-optic-electronic Co. Ltd. of CETC & 24 Institute

Analysis of a chip failure related with test system and procedure is presented and discussed. Several kinds of sockets are compared for reliability and simultaneity of forced contacts. Meanwhile, with bad contacts, the multimeter can charge the board abnormally due to its strong output driving capability. At last, the solutions are discussed for sockets, instruments and test system board design.

A3.3 (PUB. 6) A Novel Area-Efficient ESD Power Clamp with Enhanced Noise Immunity

Xiaoyun Li, Lihui Wang, Guangyi Lu, Xin Gao, Mei Li, Hisilicon Technologies Co., LTD

A novel area-efficient ESD power clamp with enhanced noise immunity is proposed. This design can extend on-time of big MOSFET and reuse shutoff NMOS transistor to reduce detection circuit's area. The 29.6% reduction of detection circuit's area is achieved. The verification is done under an advanced FinFET process.

A3.4 (PUB. 7) Experimental Investigation of ESD Protection for a 22-nm FD-SOI Process

Xiaotian Chen, Yize Wang, Yuan Wang, Peking University

To study the electrostatic discharge (ESD) characteristics of the full-depleted silicon-on-isolation (FD-SOI) device, some ESD structures are fabricated in a 22-nm FD-SOI process. The DC and TLP experimental testing have been fulfilled and investigated.

A3.5 (PUB. 8) A Modified RC and Diode Co-Triggered ESD Clamp Circuit

Zhaonian Yang, YiBo Zhang, Pan Mao, XI'an University of Technology

This paper presents a new ESD clamp circuit which is co-triggered by RC and diode. It is immune to the false triggering caused by fast power-up events due to the diode detection mechanism. With the addition of a common source amplifier, the detection signal is enhanced, and the clamp device is turned on more quickly. The proposed circuit is designed in a 0.18 μm 1.8-V CMOS process and verified by numerical simulation. The characteristics and the improvements of the new circuit are discussed.

A3.6 (PUB. 9) ESD Pulse Width Effect on RC-Triggered NMOS With Power On or Off

Xinyu Zhu, Fangjun Yu, Hongyu Shen, Zekun Xu, Shurong Dong, Zhejiang University

The robustness of RC-triggered NMOS clamp in 28nm process is significantly reduced under the condition of long pulse width and power on. The simulation results show that the device faces the risk of turning off in these two cases, and the simulation results are in line with the test results.

E1: ESD Manufacturing and Factory Control

Moderator: Marcus Koh, Everfeed Technology Pte Ltd

E1.1 WITHDRAWN

E1.2 How do I get my Manufacturing Site ANSI/ESD S20.20 Certified?

Bernard Chin, Qorvo; L.H. Koh, Everfeed Technology Pte Ltd

The author will articulate the following: 1) Provide challenges and factors to consider when ANS/ESD S20.20 on-site certification is required; 2) Establish an enhanced quality management system beyond ANSI/ESD S20.20 requirements; 3) Review some of the potential improvements to ANSI/ESD S20.20

E1.3 (PUB. 23) EOS/ESD Manufacturing Mitigation Review

L.H. Koh, K.Y. Loh,Everfeed Technology Pte Ltd; Bernard Chin, Qorvo International Pte Ltd

This paper serves to review the typical EOS/ESD manufacturing issues from component level to system level for ESD sensitive devices (ESDS). The automated testing handling equipment impact on ESDS component failure will be articulated. ESDS failure on printed circuit board assembly is included too.

E1.4 WITHDRAWN

E1.5 Global Supply Chain ESD Control Program Development

Davis Xi, Fred Bahrenburg, Jacky Zhang, Dell Technologies

This invited talk will cover the following areas: 1) ESD basic measuring instruments and methods, 2) ESD measurement standards, 3) ESD impact on PCBA quality, 4) PCBA processes effectively protect ESD, 5) New EE material design enhances ESD protection.

E1.6 WITHDRAWN

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