2026

Asia- International Electrostatic Discharge Workshop

July 13-16, 2026

IEW-ASIA

Setting the Global Standards for Static Control!

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Welcome to IEW–Asia 2026

Dear Colleagues and Distinguished Participants,

On behalf of the organizing committee, it is my great pleasure to welcome you to the 2026 International Electrostatic Discharge Workshop (IEW–Asia), co-located with IPFA 2026 at the Marina Bay Sands Expo and Convention Centre in Singapore from July 13 to 16, 2026. As the second IEW event held in Asia, this workshop continues to strengthen regional and global collaboration within the ESD and EOS communities. IEW–Asia 2026 provides an engaging platform for presenting new research, exchanging innovative ideas, and discussing the latest challenges in ESD/EMC design, reliability, and system integration, particularly in the context of rapid advancements in artificial intelligence and heterogeneous integration technologies. This event would not be possible without the dedication of our management committee: Dimitri Linten (imec, Vice General Chair), Jack Zeng (GlobalFoundries, Technical Program Chair), Guangyi Lu (Southeast University, Invited Talks and Seminar Chair), Hailian Liang (Wuxi University, Discussion Group Chair), CS Tay (Canmax Technologies, Local Publicity and Activity Chair), and Justin Ong (ESD Consulting, Local Publicity and Activity Co-Chair). We also sincerely acknowledge the strong support from the EOS/ESD Association, Inc., including Shih-Hung Chen (AMD, IEW-Asia Event Advisor), Lisa Pimpinella (Executive Director), Christina Earl and Brennan Pimpinella (Operations), and Michael G. Khazhinsky (Silicon Labs) and Robert Gauthier (IBM) as Events Directors.

This year's technical program features a distinguished keynote speech by Haiming Wang (Southeast University). We are also honored to host an outstanding lineup of invited speakers, including Joshua Yoo (Core Insight, Inc.), Wei Huang (ESDEMC Technology LLC), Marcus Koh (Electrostatic Singapore Academy), Abhijat Goyal (Marvell), Ling Zhang (Zhejiang University), Hailian Liang (Wuxi University), Wangyong Chen (Sun Yat-sen University), and Guangyi Lu (Southeast University). Their contributions span critical topics such as AI-assisted design, advanced ESD characterization, semiconductor manufacturing reliability, heterogeneous integration, electromigration, and on-chip protection design. In addition, we gratefully recognize the Technical Program Committee for their essential contributions: Jack Zeng (GlobalFoundries, Technical Program Chair), Masanori Sawada (Hanwa), Mototsugu Okushima (Renesas), Marko Simicic (imec), Lena Zeitlhoefler (Infineon), Chuan-Jane Chao (RichWave), Eleonora Gevinti (STM), Guangyi Lu (Southeast University), Kyong Jin Hwang (GlobalFoundries), Wei Liang (Intel), Jie Xiong (Hisilicon), Jiang Hsin Lee (Vanguard International Semiconductor), Yi-Ting Lee (Siemens EDA), Wang Yang (Nanjing University of Posts and Telecommunications), Joshua Yoo (Core Insight, Inc.), and Aihua Dong (Hisilicon).

In addition to keynote and invited presentations, the workshop features poster sessions, discussion groups, and opportunities for open interaction across disciplines. The co-location with IPFA 2026 further broadens the technical scope and fosters interdisciplinary exchange, enabling participants to engage with a wider audience and explore complementary areas such as failure analysis and system reliability. We extend our sincere appreciation to all speakers, authors, committee members, and contributors for their valuable efforts and dedication. We hope that IEW–Asia 2026 will inspire fruitful

discussions, encourage new collaborations, and provide a rewarding and memorable experience for all participants.

Chun-Yu Lin
National Yang Ming Chiao Tung University, Taiwan,
General Chair

IEW Keynote

Tuesday, July 14, 2026
11:15 – 12:15

Electronic Design Intelligence: Standardizing Autonomy Levels for RFIC Design

Haiming Wang, SOUTHEAST UNIVERSITY, Nanjing, China

The rapid integration of artificial intelligence (AI) and machine learning (ML) into electronic design automation (EDA) has catalyzed a surge in research across analog, radio-frequency (RF), and photonic integrated circuits (ICs). However, the absence of a standardized terminology to classify the autonomy and functional attributes of these systems remains a significant barrier to benchmarking progress. This talk introduces the Electronic Design Intelligence (EDI) framework, a structured classification system designed to define the decision-making loop in RFIC design. We propose four distinct levels of design autonomy to categorize the synergy between human expertise and machine intelligence: Level 1 (Human-Led): The designer maintains full control over the design loop and all decision-making processes. Level 2 (AI-Assisted): AI serves as a supportive tool, providing data-driven insights while the human designer retains decision authority. Level 3 (AI-Augmented/Copilot): AI takes the lead in executing the majority of design decisions, functioning as a primary driver within the human-supervised workflow. Level 4 (Full Autopilot): The EDI system manages the end-to-end design process autonomously, with the human designer acting solely as the final observer and authority. By categorizing state-of-the-art methods and applications within these levels, the EDI framework establishes a common language for industry. This standardization enables researchers and engineers to more effectively evaluate, compare, and communicate the capabilities of next-generation AI-powered EDA tools.

Haiming Wang was born in 1975. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Southeast University, Nanjing, China, in 1999, 2002, and 2009, respectively.

He joined the School of Information Science and Engineering and the State Key Laboratory of Millimeter Waves, Southeast University, Nanjing, China, in 2002, and is currently a Chair Professor. He is also a part-time professor with the Pervasive Communication Research Center, Purple Mountain Laboratories, Nanjing, China. He has authored and co-authored over 60 technical publications in IEEE TRANSACTIONS and other peer-reviewed academic journals.

Currently, he is an expert in China's 6G task force research supported by the Ministry of Science and Technology of China. Professor Wang has authored and co-authored more than 80 patents and 60 patents have been granted. He was awarded twice for contributing to the development of IEEE 802.11 by the IEEE Standards Association in 2018 and 2020. His current research interests include Radio Frequency (RF) Intelligent Design Methodologies and EDA Tools and High-Efficiency Nonlinear Wireless Communications.

IEW Invited Talk I

Tuesday, July 14, 2026
13:15 – 14:05

Recent Advances in ESD/LU Characterization and Testing
Wei Huang, ESDEMC TECHNOLOGY LLC

This presentation explores several recent advancements in Electrostatic Discharge (ESD) and Latch-up (LU) testing methodologies, focusing on HBM, CDM, LU, and TLP solutions. Regarding HBM (Human Body Model), parasitic properties within the test setup have become a primary concern in device characterization. This session discusses conventional methods for mitigating parasitic effects and introduces recent improvements, including a low-parasitic relay-based design and a novel solid-state HBM pulse module. For LU (Latch-up) testing, traditional systems often face limitations in stress capability and measurement granularity. Hardware constraints—such as a 100V/1A stress limit, lack of enough time-domain data, and manual temperature control—are addressed through the introduction of a next-generation LU tester. Key features and specific industrial use cases are presented. In the area of CDM (Charged Device Model), recent industry focus has shifted toward low-voltage repeatability and wafer/die-level testing. While a single "ideal" method remains elusive, this talk evaluates and compares several emerging "contact-first" discharge techniques.

Finally, for TLP (Transmission Line Pulsing), the demand for faster rise times in vf-TLP (< 30 ps) and higher pulse levels (> 200 A) is increasing for specialized applications. The ESDEMC group presents its latest developments in this field, including a vf-TLP module with a rise time < 10 ps and a high-current TLP setup capable of exceeding 600 A.

Wei Huang received his M.S.E.E. from the Missouri University of Science and Technology in 2010 and B.S.E.E. from Beijing University of Posts and Telecommunications in 2007. He was a research assistant at the MS&T EMCLAB with interests of electromagnetic, electrostatic and RF designs. He is the founder of ESDEMC Technology LLC and is focusing on new ESD and EMC test solutions developments.

IEW Invited Talk II

Tuesday, July 14, 2026
16:35 – 17:25

Full-Chain Automated ESD Power Clamp Design: From Specification to Silicon Validation With Diverse Performance Priorities

Guangyi Lu, SOUTHEAST UNIVERSITY, Nanjing, China

Electrostatic discharge (ESD) protection faces growing challenges with technology scaling, which demands simultaneous assurance of high-current robustness and internal node reliability. This talk presents an intelligent and automated design methodology for ESD power clamps, covering both main clamps and area-constrained local clamps. For main clamps, an application-driven topology selection framework is developed to address diverse performance priorities, followed by full-chain automation from specification to silicon validation. Representative topologies are curated based on formalized design rules, and device dimensions are optimized through algorithm-driven exploration, enabling balanced trade-offs among performance, power, and area (PPA). To further enhance internal protection against fast Charged Device Model (CDM) events, a complementary automated synthesis approach for local clamps is proposed. By incorporating conduction time (Ton) constraints into a genetic algorithm with analytical area estimation, the method achieves precise control of transient behavior under strict area limits. The optimized local clamps effectively suppress voltage overshoot at sensitive internal nodes while maintaining minimal area overhead. Validated through post-layout simulations and silicon measurements in a 40-nm CMOS process, the proposed methodologies demonstrate significant improvements in design efficiency, automation level, and protection performance, providing a comprehensive solution for modern ESD protection design.

Guangyi Lu received the B.S., M.S., and Ph.D. degrees in microelectronics and solid-state electronics from Peking University, Beijing, China, in 2011, 2014, and 2018, respectively. He served as a Principal Engineer with HiSilicon Technologies, Shenzhen, China, from August 2018 to July 2024. He joined the School of Integrated Circuits, Southeast University, Nanjing, China, in August 2024, and is currently an Associate Professor. His current research interests include AI powered IC design for ESD protections and input and output interface circuits.

IEW Invited Talk III

Wednesday, July 15, 2026
08:30 – 09:20

Building a Culture of Quality: Practical ESD Control for Reliable Semiconductor Manufacturing

Marcus KOH, ESDA Certified Professional, iNARTE ESD Engineer

Electrostatic Discharge (ESD) is a pervasive threat to yield and reliability, yet many programs fail to move from paper compliance to practical, floor-level effectiveness. This seminar provides a comprehensive overview of building a sustainable ESD control program, with a special focus on the most common and costly failure points. The speaker will cover essential foundations—grounding principles and personnel safety (wrist straps, smocks)—before advancing to more complex challenges. The presentation will include critical insights into: 1. Automation Risks: ESD process assessment for automatic handling equipment, wire bonders, and die attach systems. 2. Latent Defects: Understanding and preventing electrically-induced physical damage that escapes electrical testing. 3. The Certification Path: How a structured approach based on ANSI/ESD S20.20 can streamline your journey to a robust ESD program. Led by an ESDA Certified ESD Professional-Program Manager and iNARTE ESD Certified Engineer, this session is packed with real-world examples and actionable strategies. It is ideal for manufacturing engineers, quality assurance professionals, and managers looking to reduce costs, improve quality, and build a true culture of ESD excellence.

Marcus KOH is an expert in EOS/ESD, having served as an instructor, technical session speaker, local chair, publicity chair, and co-sponsor for various EOS/ESD Association (ESDA) Symposiums from 2012 to 2021. His contributions include numerous technical publications in renowned conferences, transactions, journals, and symposiums, underscoring his dedication in the field. Dr. KOH has been a proactive advocate for advancing EOS/ESD practices in the electronics assembly and manufacturing industries across the Asia Pacific. Renowned for his engaging workshops conducted in both English and Mandarin (Chinese), he has seamlessly integrated ANSI/ESD S20.20 and IEC 61340-5-1 standards into practical applications. His ability to demystify complex concepts and provide actionable insights has been pivotal in guiding ESD practitioners across the region, helping them achieve the prestigious iNARTE ESD Control Certification. A graduate of Nanyang Technological University, Dr. KOH holds a Doctorate of Philosophy and a Bachelor of Engineering (First-Class Honors). His current

research focuses on andragogy, lifelong learning, competency-based training, artificial intelligence, system reliability, and solving stochastic problems through advanced statistical modeling. With his deep technical expertise, innovative teaching methodologies, and commitment to fostering professional growth, Dr. KOH has established himself as a trusted mentor and effective facilitator for adult learners in highly technical fields.

IEW Invited Talk IV

Wednesday, July 15, 2026
09:30 – 10:20

Challenges and Limitation of AI related 2.5D/3D Heterogeneous Integration, Chiplet and System integration and Enabling Solutions

Yong Hoon (Joshua) Yoo, Core Insight, Inc. / Korea EOS/ESD Association

Starting several years ago, AI related industry became a major trend in industry and advanced package device revealed as a key element to make this happen successfully beyond legacy technology. More than 10 years ago, CDM sensitivity proposed to drop 250V level from 500V and this trend keep lowering down to 125V for 7nm and beyond technology node. Along with this, when device speed incredibly faster bandwidth 900GB/s and 1.8TB/s and final package chip ESD sensitivity drops below 100V. Die-to-Die interface even much lower level 30V or below for Advanced package devices. This is significant challenges for ESD control of AI related industry. Along with these changes, industry facing several other key problems to control ESD in manufacturing environment such as measurement methodologies and accuracy. Most of technologies for current ESD control measurement has developed and used over 30 – 40 years. Electrostatic fieldmeter and Electrostatic voltmeter technology has been used to identified charge level on device or process required insulator near the ESDS items. Are these measurement techniques suitable for sub-30V level of ESD control? Do we have fasted enough measurement bandwidth for evaluation and analysis of risk assessment where ultra-sensitive device handling? How should we fix problems? We should follow ohms' law. V = IR and I = V/R. Discharge current is a key driver to give damage to device. We can use lowering voltage on device and increase contact resistance to device. Resistance control of material requires better homogenous and optimized resistance ranges. Maintain low voltage on device and low offset voltage of ionizer are another key element to keep device safe instead of just fast discharge time. AC ionization technology makes pair of ions by switching electric field on sharp emitter points and this electric field potential threat that can give a damage to high-speed interfaces and ultra-sensitive devices. Steady-State DC ionization technology makes pair of ions by constant high voltage on sharp emitter points and can be cancelled high voltage electric fields by proximity close distance between two polarities. Thus, Steady-State DC technology can be maintaining low offset voltage lower than 5V level and improves yield impact in critical processes of advanced package device ESD control. Joshua will present how successfully yield improvement by Process Assessment and Steady-State DC ionization technology.

Yong Hoon (Joshua) Yoo has been involved in the static control industry since 1994 for ionization, ESD measurement and ESD risk assessment service in semiconductor, flat panel displays and automotive industry. He has been a member of EOS/ESD Association since 2000 and served as an Elected Board of Director in 2016 - 2018. He is the founder and president of Korea EOS/ESD Association since 2011. He is a member of Institute of Electronics and Information Engineers (Korean IEEE) since 2021. He is serving industry as Korea President of International Semiconductor Executive Summits (ISES) since 2024. He started his volunteering activities on EOS/ESD Association since 2013 as an active working group members, working group chair and technical program committee members of annual symposium for multiple events of ESD Association. With his leadership, Korea EOS/ESD Association very strongly presents and annual events over 10 years. He is a pioneer of contamination and ESD issue for flat panel display (FPD) in failure analysis and yield improvement. Since 2024, he conducted EOS/ESD assessment at multiple contract manufacturing sites and improved yield significantly in AI related chip and system manufacturing environment. He is an iNARTE certified ESD Engineer in 2007 and the EOS/ESD Association certified Professional ESD Program Manager in 2011. He has 14 patents for ionization system and ESD testing technologies.

IEW Invited Talk V

Wednesday, July 15, 2026
10:50 - 11:40

ESD design, debug and verification methodologies for state of the art heterogeneous 2.5D/3D/3.5D integration

Abhijat Goyal, MARVELL

This talk examines the emerging challenges in designing and verifying electrostatic discharge (ESD) protection circuits for high-speed interfaces within advanced 2D/2.5D/3.5D packaging architectures. The focus is on chiplet-based systems utilizing TSMC's CoWos (Chip-on-Wafer-on-Substrate) technology as the integration baseline. As chiplets from diverse vendors and process technologies are integrated into a unified system, ensuring robust ESD protection becomes increasingly complex. Each chiplet may exhibit distinct electrical behaviors, sensitivities, and interface requirements, complicating the development of cohesive protection strategies across the package. Traditional ESD verification approaches, which rely heavily on CAD tools, face significant limitations in this context. The consolidation of multiple netlists into a master netlist often leads to memory constraints and scalability issues. Moreover, accurately modeling current distribution across the interposer and substrate—particularly through microbumps connecting dies—is technically demanding. These challenges are further intensified by the inclusion of high-bandwidth memory (HBM) stacks, which introduce additional complexity in current flow and protection path analysis. To address these issues, we propose a set of design principles that streamline ESD implementation and verification in 3.5D systems. Derived from practical experience and simulation insights, these principles emphasize modularity, hierarchical verification, and simplified modeling techniques that preserve essential ESD behavior while minimizing computational overhead. By structuring the problem into a manageable framework, our methodology facilitates early detection of failure risks and enhances system-level robustness. This work contributes to the advancement of scalable and reliable ESD design practices for next-generation heterogeneous integration platforms.

Abhijat Goyal received a Bachelor of Technology degree from the Indian Institute of Technology (IIT) Madras, followed by a Master's and Ph.D. in Electrical Engineering from Pennsylvania State University. With over two decades of experience in the semiconductor industry, Dr. Goyal has specialized in electrostatic discharge (ESD) protection and analog intellectual property (IP) design. He is the author of more than 30 technical publications spanning diverse domains, including microelectromechanical systems (MEMS), carbon nanotube technologies, analog circuit design, and ESD. In addition to his scholarly contributions, Dr. Goyal holds multiple patents in these areas, reflecting his commitment to innovation and practical impact. Currently serving at Marvell, Dr. Goyal plays a key role in advancing ESD design methodologies and is actively involved in several industry-standard committees focused on ESD protection and reliability. His work continues to influence best practices and standards across the semiconductor ecosystem.

IEW Invited Talk VI

Wednesday, July 15, 2026
13:30 – 14:20

Fast, Accurate, and Reliable Electromagnetic Compatibility Design for High-Density Interconnects

Ling Zhang, ZHEJIANG UNIVERSITY, Hangzhou, China

The increasing complexity of high-density interconnects poses significant challenges to electromagnetic compatibility design in terms of efficiency, measurement accuracy, and reliability. In this talk, we present a set of methodologies addressing these challenges from three perspectives: fast modeling, accurate measurement, and reliable design. Physics-based and data-assisted modeling approaches are developed to accelerate electromagnetic analysis, reducing the design cycle from days to minutes in representative cases. A broadband multi-port on-wafer calibration method based on a 64-term error model extends the four-port measurement bandwidth from 50 GHz to 110 GHz. In addition, a system-level design approach is introduced to account for interactions among signal integrity, power delivery, and electromagnetic interference, improving robustness against electromagnetic disturbances. These results provide practical insights into the modeling, measurement, and design of high-density interconnect systems.

Ling Zhang received the B.S. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2015, and the M.S. and Ph.D. degrees from Missouri University of Science and Technology, Rolla, MO, USA, in 2017 and 2021, respectively, both in electrical engineering. From Jun. 2021 to Nov. 2023, he was a postdoc research fellow at Zhejiang University, Hangzhou, China. In Dec. 2023, Dr. Zhang officially joined Zhejiang University as a ZJU100 Young Professor and doctoral supervisor. Dr. Zhang has authored and co-authored more than 110 IEEE journal and conference papers. Dr. Zhang was the recipient of the Young Scientist Award in APEMC 2022, the 2024 IEEE EMC Society Herbert K. Mertel Young Professional Award, and the 2025 ACES-China Young Scientist Award.

IEW Invited Talk VII

Thursday, July 16, 2026
08:50 – 09:40

Electromigration Reliability in Advanced Interconnects and Backside Power Delivery Networks: A Comprehensive Analysis Using Multi-Physics Simulations

Wangyong Chen, SUN YAT-SEN UNIVERSITY, Guangzhou, China

This report examines electromigration (EM) reliability in advanced metal interconnects, with a primary focus on complementary FET (CFET) structures and backside power delivery networks (BSPDNs). The studies employ kinetic Monte Carlo (KMC) simulations coupled with thermal and stress analyses to investigate void formation, resistance degradation, and time-to-failure (TTF) under various conditions. Key results indicate that alternative metals like ruthenium (Ru) and molybdenum (Mo) significantly enhance EM lifetime compared to conventional copper (Cu) and tungsten (W), with Mo showing superior performance in middle-of-line (MOL) layers and Ru-Mo combinations optimizing BSPDN reliability. Thermal effects from self-heating and grain boundary impacts are critical factors, emphasizing the need for material-aware design in sub-3 nm technology nodes. This report provides a consolidated overview of methodologies, results, and recommendations for improving EM reliability in next-generation interconnects.

Wangyong Chen is an Associate Professor at Sun Yat-sen University. He received his Ph.D. from Peking University. His research focuses on thermal management and reliability design of integrated circuits. He has led more than 10 research projects, including the National Natural Science Foundation of China (NSFC) Young Scientist Program. He has authored or co-authored over 50 SCI/EI-indexed papers, including more than 30 as first or corresponding author in top-tier journals such as IEEE Electron Device Letters and IEEE Transactions on Electron Devices, as well as at conferences including the IEEE International Electron Devices Meeting (IEDM). He also holds over 10 software copyrights and has filed/been granted multiple patents.

IEW Invited Talk VIII

Thursday, July 16, 2026
13:50 – 14:40

High-current ESD/ EOS Integrated Protection with Enhanced Voltage Endurance for Improving IC Reliability

Hailian Liang, WUXI UNIVERSITY, Wuxi, China

Electrostatic discharge and surge impact are inevitable electrical phenomena during the standby, testing and operation of circuits. In recent years, with the wide application of AI robots, the improvement of integration density in electronic systems and the development and application of multi-power-domain chip integration have become an inevitable trend. High-frequency, multi-functional and highly integrated digital-analog hybrid electronic modules or devices have become an indispensable part of electronic systems. With the increasing demand for the performance and stability of AI robots and various electronic systems, the traditional protection requirements of 2000 V for ESD and 200 mA for electrical surge can hardly meet the stable operation requirements of highly integrated hybrid electronic systems. Combined with the electrostatic and surge protection requirements in practical application scenarios and products, this report elaborates the integrated protection mechanism of ESD and surge and its performance verification approach from low voltage to high voltage through experimental cases. It further discusses the energy-efficient design methods for the integrated ESD and surge protection of complex electronic systems, so as to provide technical support for the application of high-efficiency, high-stability and highly integrated electronic systems.

Hailian Liang, Professor, School of Integrated Circuit Science and Engineering, Wuxi University, Deputy Secretary-General, Wuxi Integrated Circuit Society. Dr. Hailian Liang has been engaged in the research on ESD and EOS protection for more than ten years. She focuses on the reliability of integrated circuits, and has extensive experience in the design and development of on-chip electrostatic and surge protection. She also has a good experience of the electrical performance measurement of various electronic systems for electrostatic and surge protection. She took a lead in developing and verifying a highly integrated electrostatic and surge protection method in China, which satisfies the requirements of on-chip ESD protection and port surge protection in electronic systems. She has also developed a variety of ESD and surge protection chips with robust latch-up immunity for high-voltage, medium-voltage and low-voltage

applications. Dr. Liang has served as a principal researcher in several national and provincial natural science foundation projects as well as enterprise R&D projects. In this seminar, she will share practical design methods, typical design cases and experimental experience of ESD and EOS co-design and integrated protection.

IEW Discussion Group I

Wednesday, July 15, 2026
11:50 – 12:40

ESD Control in Advanced Packaging
Moderator: Tay CS, CANMAX TECHNOLOGIES, Malaysia

As we herald in the exciting opportunities offered up by advanced packaging technologies, we need to be mindful of the challenges posed by ever more sensitive devices. What has worked well until very recently, the typical ESD control program developed around CDM 200V, will suddenly need to evolve quickly to the demands of CDM breaching thresholds below 10V.To compound the challenges, there is no known commercial tester that is able to test these packages for ESD robustness. We cordially invite you to join us on a session exploring:

1. What the gaps are in implementing ESD control for these advanced packages
2. Mitigation techniques being practiced currently, known solution providers in the industry
3. Work being undertaken currently to address those needs

IEW Discussion Group II

Thursday, July 16, 2026
14:50 – 15:40

ESD/EOS Design Challenges in High-Voltage (HV) Technologies
Moderator: Hailian Liang, WUXI UNIVERSITY, China

High-Voltage (HV) technologies, typically implemented in BCD (Bipolar-CMOS-DMOS) processes, are fundamental to power management, automotive electronics, and industrial applications. Unlike advanced CMOS, which is primarily driven by feature size scaling, HV ICs face distinct ESD and EOS challenges due to the inherent co-integration of low-voltage control circuits and high-voltage power devices. The complex parasitic bipolar transistors inherent in DMOS structures, combined with a wide operating voltage range (from 5V to over 100V), can trigger dangerous snapback behaviors and severe, difficult-to-control current crowding. Furthermore, the harsh and diverse operating environments typical of automotive applications demand exceptionally high ESD/EOS robustness, which in turn drives the need for effective and reliable on-chip protection solutions. This panel session will discuss:

1. Have panellists encountered ESD and surge protection challenges on power rails and power driver ports in high-low voltage mixed-signal circuits on BCD process platforms? What are the common protective measures and solution paths?
2. Have you observed sudden latch-up issues in power driver circuits during operation? What level of product damage has this caused? What technical measures have been adopted in engineering to prevent latch-up phenomena?

IEW Poster Teaser Session

Session A: ESD Protection Circuit, Device and Technology
Tuesday, July 14, 2026
14:15 – 14:50

A.1: ESD Protection Design for Wideband Bypass Circuits in CMOS Technology
Er-Wen Chien, Chen-Yu Liang, Chun-Yu Lin, NYCU, Chin-Ya Su, IMEC and KUL, Wei-Min Wu, Marko Simici, IMEC, and Patrick Reynaert, KUL

This study proposes a two-stage wideband bypass circuit integrating a transient-triggered power clamp in CMOS process. The architecture balances high-frequency noise suppression with robust ESD protection. Optimizing capacitor ratios achieves an applicable band above 0.36 GHz and significantly improves VF-TLP current handling capability to over 10 A.

A.2: Assessment of BiSCR ESD Protection Effectiveness for High Voltage LDMOS Devices
Ting Yang, GLOBALFOURNDRIES and NTU, Jie (Jack) Zeng, Kyong Jin Hwang, GLOBALFOURNDRIES, and Tupei Chen, NTU

The study evaluates how a Bidirectional SCR (BiSCR) structure improves the ESD robustness of high voltage LDMOS devices. LDMOS devices with and without BiSCR are compared by TLP measured results. This demonstrates that adding a BiSCR provides significant enhancement in ESD protection.

A.3: Transient Analysis of GaN-on-Si Schottky Diodes in ESD HBM Time Domain
Chin-Ya Su, IMEC and KU LEUVEN, Wei-Min Wu, Hao Yu, Arturo Sibaja-Hernandez, Wen-Chieh Chen, IMEC, Chen-Yu Liang, NYCU, Bertrand Parvais, VUB, and Patrick Reynaert, KU LEUVEN

This research analyzes the HBM transient conduction mechanisms of GaN-on-Si Schottky diodes. Analysis of the falling edge reveals two distinct conduction regimes. At low HBM stress, gate resistance dominates. At high HBM stress,

2DEG resistance become dominant component. Therefore, reducing 2DEG sheet resistance significantly enhances ESD robustness of forward Schottky diodes.

A.4: Stacked Schottky Diodes Studies for RF ESD Protection in a GaN Power Amplifier

W.-M. Wu, IMEC, L. Pucek, ZAGREB UNIVERSITY, E. Sac, IMEC and VUB, D. Yan, IMEC, T. Markovic, ZAGREB UNIVERSITY, M. Simicic, IMEC, B. Parvais, P. Wambacq, IMEC and VUB, and C.-Y. Lin, NYCU

To achieve 1 kV human-body-model (HBM) robustness in GaN power amplifiers, an ESD protection scheme based on stacked GaN Schottky diodes is proposed. This work demonstrates the RF co-design of the stacked Schottky diodes with the power amplifier. Detailed ESD characterization and analysis of the stacked Schottky diode structure are presented in this poster.

A.5: Comparative Study of Guard Ring Topologies for Latchup Performance in CMOS Circuits

Kuin Woon Jong, Rebello Alwyn, and Kyong Jin Hwang, GLOBALFOUNDRIES

This work presents a comprehensive experimental comparison of guard ring topologies, evaluating the relative effectiveness of partial and full configurations for latchup suppression. Results indicate that detector facing guard ring provide the dominant latchup protection and the detector facing bar-type guard ring offering a highly practical and area-efficient solution for area constrained layout designs.

IEW Poster Teaser Session

Session B: ESD Control, ESD/EMC Design and Verification, and 2.5D/3D Chiplet Design
Wednesday, July 15, 2026
14:30 – 15:20

B.1: ESD Footwear Tester with Training Authorization
Teerasart Songsa-ard, WESTERN DIGITAL STORAGE TECHNOLOGIES (THAILAND) LTD.

Audit findings identified production access with expired ESD and Process Instruction certifications. An integrated system combining ESD Footwear Testing and Training Certificate Verification was implemented to enforce access control at entry points. Deployed across 12 areas with 24 testers, the solution achieved 100% compliance and enables continuous monitoring via a centralized dashboard.

B.2: AI Memory ESD Sensitivity and ESD Control Challenges
Yvonne Yeo and Michelle Lam, IBM

AI accelerators require ultra low latency memory architectures such as High Bandwidth Memory (HBM) to meet growing data demands. However, next generation HBM4 drastically lowers CDM robustness to ~30 V, challenging existing ESD programs. This work advocates shifting from discharge control to comprehensive charge prevention strategies tailored for highly automated 2.5D/3D HBM manufacturing.

B.3: Automated Synthesis of ESD Diodes with Professional Backend Implementation under Robustness– Parasitics Trade-offs
Haoyu Xia, Guangyi Lu, Qi Wu and Haiming Wang, SOUTHEAST UNIVERSITY

This work presents an automated, simulation-driven synthesis flow for ESD diodes, balancing robustness, parasitic capacitance, and area overhead. Utilizing Bayesian Optimization with Gaussian Process Regression, the framework achieves sample-efficient design space exploration. The flow automatically generates DRC/LVS-clean, professional layouts, providing practical solutions for high-speed IC I/O interface protection.

B.4: Time-Dependent Inductance and Resistance of the FI-CDM Spark
Yaxin Liu, Guangyi Lu, Qi Wu, Haiming Wang, and Longxing Shi, SOUTHEAST UNIVERSITY

We propose a novel FI-CDM spark model incorporating time-dependent inductance and resistance to address limitations of the conventional two-pole RLC representation. A hybrid knowledge-guided, data-driven algorithm enables accurate waveform fitting, achieving significantly improved agreement in peak and full-wave regions and demonstrating robustness across multiple voltage levels.

B.5: Set-level ESD Solution for DDR4 Memory
Sangwoo Kim, SAMSUNG ELECTRONICS

We propose an on chip system level ESD solution for DDR4 memory. By controlling Command-buffer bandwidth, the approach suppresses invalid commands induced by ESD noise. The method eliminates on chip system level ESD failures, achieving a zero percent failure rate for DDR4 devices.

B.6: CDM in the Chiplet Era
Lena Zeitlhöfler, Friedrich zur Nieden, and Kai Esmark, INFINEON TECHNOLOGIES AG

Charged Device Model (CDM) testing according to JS-002 requires an enhancement to address new industry requirements. As device geometry, testing levels, and granularity of results become finer and packaging becomes obsolete, CCTLP is presented as an alternative for CDM testing. CCTLP improves accuracy and reduces measurement deviation, particularly at low test voltages and for small packages. A method is proposed to correlate results with known CDM target levels.

B.7: A Contact Sequence Based Conceptual Framework for CDM Risk in Stacked Die Interfaces
Jun-Bae Kim, SAMSUNG ELECTRONICS

3D stacked die packages increase CDM failure risk, which is a reliability challenge. We propose a contact sequence framework that quantifies risk with Signal Only Interval and Neighbor Ground Delay. Early ground first contact expands the discharge area, reducing the initial current density and mitigating failures. It provides robust design guidelines for stacked die integration.

IPFA-IEW Joint Poster Session

Thursday, July 16, 2026
09:50 – 11:50
IPFA Exhibition Hall

IPFA ESD and 4 IEW joint posters are presented

IPFA ESD Oral Session

Thursday, July 16, 2026
11:45 – 12:35
IPFA

IEW Social Networking Activity

Tuesday, July 14, 2026
17:50 – 21:00

Gardens by the Bay

- Dinner: 6:30pm
- Lightshow: 7:45pm & 8:45pm (free)
- Flow Dome & Cloud Forest" (Optional: Self-paid, SG$46/person, last admission 8:00pm)






IEW Schedule

Start	End	Monday, July 13, 2026
08:30	18:30	IPFA Tutorial Day

Start	End	Tuesday, July 14, 2026
08:30	10:05	IPFA Welcome and Plenary Session I
10:05	11:05	Break and IPFA AI for FA Poster Session
11:05	11:15	IEW Opening Welcome
11:15	12:15	IEW Keynote
12:15	13:15	Lunch
13:15	14:05	IEW Invited Talk I
14:15	16:20	IEW Teaser and Poster Sessions A
16:20	16:35	Break
16:35	17:25	IEW Invited Talk II
17:50	21:00	IEW Social Networking Activity

Start	End	Wednesday, July 15, 2026
08:30	09:20	IEW Invited Talk III
09:30	10:20	IEW Invited Talk IV
10:20	10:50	Break
10:50	11:40	IEW Invited Talk V
11:50	12:40	Discussion Group I
12:40	13:30	Lunch
13:30	14:20	IEW Invited Talk VI
14:30	17:30	Teaser and Poster Sessions B
17:30	17:45	Break
17:45	18:20	Transportation from MBS to Banquet Venue
18:45	22:00	IPFA Banquet

Start	End	Thursday, July 16, 2026
08:50	09:40	IEW Invited Talk VII
09:40	11:30	IPFA and IEW Joint Poster Sessions
11:30	11:50	Break
11:45	12:35	IPFA ESD Sessions
12:35	13:50	Lunch
13:50	14:40	IEW Invited Talk VIII
14:50	15:40	Discussion Group II
15:40	16:10	Break
16:10	16:50	IPFA Closing Ceremony

Note 1: Sessions highlighted in black take place in the IEW room (Lotus 4D/4E).
Note 2: The technical program is subject to change without prior notice