International Electrostatic Discharge Workshop (IEW)

12 – 16 May 2025

Hotel Dubrovnik, Gajeva ulica 1, Zagreb, Croatia

Setting the Global Standards for Static Control

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Group photo from 2023 IEW in Tutzing, Germany

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The IEW Experience

Dear Colleagues and ESD Enthusiasts,

Welcome to the 18th annual International ESD Workshop (IEW)! This year, we are thrilled to invite you to join us at the Hotel Dubrovnik in the vibrant city of Zagreb, Croatia, from 12 to 16 May 2025. This event promises to be an exciting opportunity to delve into the latest advancements and challenges in the field of Electrostatic Discharge (ESD) and Electrical Overstress (EOS).

The IEW continues to be a cornerstone for innovation and collaboration within our community. Our focus ESD focus topics this year will be on IC design, chip-level and system-level ESD, EDA, automotive applications, failure analysis, EMC, testing, and advanced technologies. We are particularly excited about our keynote and invited speakers who will bring light to new developments in the ESD field.

Our program is designed to stimulate discussions and provide a platform for presenting both completed research and open research questions. The program will include discussion groups, invited talks, technical presentation sessions and special interest groups. Each technical session will begin with a five-minute teaser presentation, followed by an engaging poster-based discussion, ensuring opportunities for interaction and idea exchange in a relaxed environment.

Join us in exploring the future of ESD and EOS, as we bring together experts from both industry and academia to share their insights and experiences. The IEW is closely aligned with the EOS/ESD Symposium, enhancing our collaborative efforts and broadening the scope of our discussions.

We look forward to your participation and to the vibrant discussions that will undoubtedly emerge from this year's workshop. Let's shape the future of ESD together!

***Marko Simicic**,*
imec,
Management Committee Chair
on behalf of the IEW management committee

(Tutorial) Optimization of ESD and Signal Integrity on System Level for Automotive Applications

Monday 12 May 2025, 13:00 – 16:30

Andreas Hardock, Sergej Bub, Nexperia

This talk briefly introduces the basics of electrostatic discharge and demonstrates practical tools and methods how to improve the ESD and SI performance of typical consumer and automotive applications also using modern simulation methods. In the first part, classical methods of signal integrity such as S-parameter, Time Domain Reflectometry and Eye diagrams are introduced and their application to various ESD protection components are presented. It is discussed how modern ESD protection elements behave in the time and frequency domain and how they can be analyzed with the help of simulations. In the second part, the methodology of System Efficient ESD Design (SEED) simulations of transient ESD events is applied on automotive applications such as 1000BASE-T1 Ethernet using concept of fully dynamic behavioral SEED models. In this context, the impact of system components such as CMCs as well as the positioning of ESD protection components is analyzed.

Andreas Hardock studied nanostructure technology at the Julius Maximilian University of Würzburg and did his PhD in the field of functional vias at the Technical University of Hamburg-Harburg. He started his professional career in 2015 in the automotive sector as an EMC engineer at Behr-Hella Thermocontrol. From 2016 to 2020 he was at Continental Automotive GmbH in Babenhausen, where he was responsible for SI / PI and EMC and ESD topics in the role of hardware architect in product development. Since 2020 he joined Nexperia as Application Marketing Manager with focus on ESD and EMC topics and products for the automotive market. Andreas is member of the IEEE EMC Society since 2011. Since 2019 he is an active member of the German EMC Chapter where from 2019 to 2020, he was responsible for organization of the Professional Talks. Since 2020 Andreas is a part of the executive team as treasurer.

Sergej Bub is a Principal System Level ESD Expert at Nexperia Germany GmbH in Hamburg. He graduated as M.Sc. in electrical engineering at Technical University of Hamburg specialized in nanoelectronics and microsystems technology. He is working at Nexperia in the research and development department in ESD Protection and Filtering group. His work covers modelling and simulation for System Efficient ESD Design (SEED) of high-speed application systems and discrete ESD protection components for automotive, mobile, consumer and computing areas, extended by development and optimization of dedicated ESD protection solutions for such applications as well as project management activities for R&D projects.

(Seminar) ESD Design Support in Practice: A Few Real-Life Examples

Monday 12 May 2025, 17:00 – 18:00

Gijs De Raad – Notable inventor, NXP Semiconductors

Providing ESD design support is something you can only learn in practice. There is no school for it. Also, exactly what the design support looks like is quite variable: it depends on the type of IC being made, the ESD building blocks and verification tools that are available, and also things like project timeline and even design habits or culture of the design group you work with. This talk will give a few real-life examples of what ESD design support can look like, with emphasis on showing how often very simple simulations can have a big impact.

Gijs de Raad was born in Ede, the Netherlands, on October 26, 1969. He received his MSc in Applied Physics in 1995 at the University of Groningen, the Netherlands. He received a PhD in Physics in 2001 at the Technical University of Eindhoven, the Netherlands, on the thesis “Voltage-dependent Scanning Tunneling Microscopy on the {110}-surfaces of GaAs, AlGaAs, and their heterostructures”. Since 2000 he has worked at Philips Semiconductors which later became NXP Semiconductors. He has been active as an ESD engineer since 2005, with particular interest in the physics of ESD devices. Today, Gijs specializes in ESD solutions for high-voltage and power ICs in mature technologies. These IC’s typically have significant analog content and in many cases require a custom ESD solution. Gijs started ESD work at the age of 35 literally from scratch, and so embodies the phrase “you’re never too old to learn”. For students he likes to add “you’re never too young to teach”.

(Keynote) ESD – Expectations, Surprises and Discoveries

Tuesday 13 May 2025, 09:30 – 10:30

Karim T. Kaschani, Robert Bosch GmbH

While electrostatic charging and electrostatic discharges (ESD) are among the oldest physical phenomena on earth, they drew attention in the design of integrated circuits due to unexpected device failures just about 45 years ago. We have learned a lot about ESD control and ESD protection since then. However, we are still often surprised to see that our expectations turn out to be wrong and there is so much more to learn. This keynote reviews some of these expectations and surprises taken from the different branches of the extremely diverse fields of ESD and EOS.

Karim T. Kaschani received his Ph.D. degree for his research in the field of semiconductor power devices in electrical engineering from the Technical University in Brunswick in 1996. He worked for almost 8 years for Siemens Semiconductors and Infineon Technologies as a development engineer and project leader in the field of advanced ICs for switch-mode power supplies, on concept engineering of high voltage SOI technologies and on the development of high voltage ICs. Afterwards he joined Atmel Automotive and worked for almost 7 years as head of the ESD test and consulting group and as product quality engineering manager. Thereafter, he joined Texas Instruments and worked for more than 9 years as senior ESD engineer responsible for the regional ESD and EOS support in Europe. He then worked for 2.5 years as leader of the ESD team for Elmos Semiconductors S.E. and is currently working as senior ESD engineer for Robert Bosch GmbH in Germany. He is a member of the steering council and also a member of the managing board of the ESD FORUM e.V. He holds several patents and is author or co-author of several papers, conference presentations and tutorials in the fields of semiconductor power devices, ICs, semiconductor technologies, ESD and EOS.

(Invited Talk) Challenges in ESD Discharge Risk Reduction to Support Advanced Packaging Manufacturing Roadmap

Tuesday 13 May 2025, 11:00 – 12:00

Dr. Philippe Muller, Suss MicroTec

During packaging and die to die bonding, there can be several ESD risks. This talk covers the typical process flows during temporary bonding and laser debonding of thinned wafers. It also includes discussion on dicing and Cu-Hybrid bonding with the two main approaches ‘wafer to wafer’ and ‘die to wafer’. The focus on the talk will be on the hardware associated aspects to depict possible areas where charging might occur. Further, some of the preliminary measures taken to reduce the risks of ESD will be presented.

Philippe Muller graduated his PhD in 2004 at the university of science and technology of Lille, France (USTL) in collaboration with Thales Research and Technologies, Palaiseau, France. He developed a high-power RF MEMS using Gold-gold wafer level packaging based on Karl Suss early MA/BA/SB6 wafer bond-aligner. He joined then imec, Belgium, as 3D packaging research engineer working on RF MEMS packages, above-IC MEMS, and RF-IPD integration. In 2009, he joined Lynred Palaiseau, France starting as Flip-chip expert within the hybrid packaging excellence center. He developed down to 10um pitch Indium bump assemblies for cooled IR sensors manufacturing. In 2015, he became technical product manager of the InSb MWIR focal plane arrays product line, leading the engineering support team and ensuring technical qualifications of the products in interface with the customers. In 2019, Philippe joined Huawei Belgium Research Center, Leuven as Lead 3D Integration Research & Development engineer. He worked in close collaboration with imec teams to develop nanoTSV, BSPDN, hybrid bonding and FoWLP technologies, evaluating thermal aspects and architecture optimizations for High performance and Sparking Neuronal Networks neuromorphic computing applications. Since 2023, Philippe joined Suss MicroTec in Germany as Technology Scout in the System Architecture and Innovation team. His role is now to help introducing raising Advanced packaging technologies in the Suss MicroTec portfolio, support product roadmap definitions and developments in the permanent, temporary bonders, inkjet printing and imprint/lithography/metrology product lines of Suss MicroTec.

(Seminar) ESD Risks During PCB Assembly Processes

Tuesday 13 May 2025, 13:00 – 14:00

Istvan Kovalik, Harman

PCB assembly processes from SMT lines to final assembly and test stations have many different production equipment and process steps. In some places, it is clearly visible if there is an ESD risk in the process, but problems can also arise in places where we would not even suspect it at a first glance. During this talk we would like to walk along the PCB assembly processes and have a look at some examples of identified risks in the production lines. Some risk assessment conceptions and questions will also be represented.

Istvan Kovalik began his work in the field of ESD control in 2003. He has fallen into love with this topic and started to go deeper into it. He's been working as an ESD Coordinator at Harman for 10 years, and responsible for all aspects of ESD control in three facilities in his country. He performs some volunteer work for ESDA and has received his ESD Program Manager Certification in 2023. Istvan recently started standardization work in IEC TC 101 committee's WG5 group.

(Invited Talk) Applications of Machine Learning to Microelectronics (and ESD) Design

Tuesday 13 May 2025, 17:00 – 18:00

Elyse Rosenbaum, University of Illinois Urbana-Champaign

Machine learning (ML) is used to make predictions, classify objects, derive dynamic behavioral models, and generate statistical distributions. In this presentation, we will look at specific applications of ML to microelectronics design, drawing primarily from work carried out by the researchers in the Center for Advanced Electronics through Machine Learning, CAEML. I'll conclude with a consideration of how those same models and algorithms might be applied to ESD design and ESD failure diagnosis.

Elyse Rosenbaum is the Melvin and Anne Louise Hassebrock Professor in Electrical and Computer Engineering at the University of Illinois Urbana-Champaign. She received a Ph.D. in electrical engineering from University of California, Berkeley. She is the director of the NSF-supported Center for Advanced Electronics through Machine Learning (CAEML), a joint project of the University of Illinois, North Carolina State University, and Penn State. Her current research interests include CDM-ESD reliability, ESD-robust high-speed I/O circuit design, compact modeling, optimization of heterogeneously integrated system-in-package, machine learning aided modeling of circuit lifetime distributions, and explainable models of analog circuits.

Dr. Rosenbaum has authored or co-authored over 200 technical papers; she has been an editor for IEEE Transactions on Device and Materials Reliability and IEEE Transactions on Electron Devices. She served as the General Chair of the 2018 International Reliability Physics Symposium. Dr. Rosenbaum was the recipient of a Best Student Paper Award from the IEDM, an Outstanding Paper Award and 2 Best Paper Awards from the EOS/ESD Symposium, a Technical Excellence Award from the SRC, an NSF CAREER award, an IBM Faculty Award, and the ESD Association's Industry Pioneer Recognition Award. She is a Fellow of the IEEE.

(Seminar) ESD in the Automotive Industry– A Proposal for Lowering Risks During System Level ESD Qualification and Reducing Component Cost

Thursday 14 May 2025, 11:15 – 11:45

Steffen Holland, Nexperia

Often, IC manufacturers get requests from their Tier1/OEM customers to provide ESD robustness levels according to ISO10605. The ISO10605 test has a contact and air discharge part. Due to the wide specification of the test generators (=ESD guns) and the stochastic nature of an air discharge the pulse form of the current pulses varies a lot. Additionally, the ISO10605 test is not specified for components which creates an even wider variability due to different setups. This results in a situation where a comparison between different parts is basically impossible which poses the risk of a failed system level ESD qualification. Customers often respond by requesting costly higher ESD robustness levels of the components.

In this talk a proposal is made to provide a repeatable test characterization for IC components which roughly correlates to the contact discharge of ISO10605. By providing this information together with SEED models Tier1 and/or OEM customers can perform virtual prototyping to optimize the system level ESD robustness and lower the risk of a failed ESD qualification. Additionally, cost savings are possible because the active area in the IC needed for ESD protection could be reduced.

Steffen Holland received the Ph.D. degree in physics from the University of Hamburg, Hamburg, Germany, in 2004. Until 2005, he was a member of research with the University of Hamburg. Afterward, he joined the process development group of Philips Semiconductors, Hamburg, Germany. He is currently with Nexperia Semiconductors, Hamburg, Germany, and working on discrete ESD protection devices as a System Architect. His main research interests include device physics and modeling.

(Invited Talk) Overcoming ESD and EMC Challenges in Advanced Optical Sensing

Thursday 15 May 2025, 09:40 – 10:30

Christian Stockreiter – ams OSRAM

Integrated optical sensors face various design challenges, particularly regarding electrostatic discharge (ESD) and electromagnetic compatibility (EMC). Addressing these issues is crucial to ensuring sensor reliability and performance in real-world applications.
This talk provides an overview of common optical sensors, focusing on their ESD and EMC requirements in terms of design architecture and testing methodologies.
Using real-world case studies, we will examine challenges faced by design teams during product development and highlight key strategies for overcoming them.

Christian Stockreiter received his master's degree and Ph.D. in Electrical Engineering from the University of Technology Graz (TUG), Austria, in 2004 and 2009, respectively. From 2004 to 2005, he worked as a Research Assistant at the Institute for Fundamentals and Theory in Electrical Engineering (IGTE) at TUG. In 2006, he joined the Systems and Analog Innovation team at NXP Semiconductors Austria as an RF System Engineer, focusing on the design of HF and UHF RFID systems. In 2008, he transitioned to Magna Steyr Fahrzeugtechnik in Graz as a Design Manager, where he was responsible for the development of automotive antenna systems.
Since 2010, he has been with the corporate R&D organization at ams OSRAM, where he currently leads the corporate V&V department. His responsibilities include validation methodologies, ESD, EMC, and overseeing the corporate R&D laboratories.

(Invited Talk) Make Your EMC & ESD Solutions Compatible!

Thursday 15 May 2025, 11:00 – 12:00

Patrice Besse, EMC & ESD manager – Fellow, NXP Semiconductors

Electronic modules should not create disturbance and should be immune against both transient aggressions and electromagnetic interference (EMI), keeping functions safe during ESD or EMI occur. Systems and integrated circuits should pass multiple EMC and ESD standards that can be specific with the application domains and over the globe. At each development step, from the technology to the validation, the ESD strategy and the EMC design must be fully compatible together to provide a common solution. In this talk, I will present basics about EMC requirements and how the EMC and ESD solutions can interact together.

Patrice Besse was born in France where he obtained Post-graduation in Compatibility Electromagnetic (EMC) in 2000. In 2004, Patrice has defended a PhD on ESD for HV analog in collaboration with Motorola and LAAS-CNRS, Toulouse, France. Then, Patrice has joined the Analog Design Group of Freescale Toulouse, (France) as ESD engineer. In the last 20 years Patrice has led ESD & EMC developments for different businesses with a main focus on automotive applications. Patrice is author of more than 40 publications, book chapter, with 42 patents granted in the field of EMC, ESD and analog design. Since 2014, Patrice manages EMC & ESD activities within NXP semiconductors, including Technologies development, ESD / EMC libraries and models, design for EMC and ESD, Lab validation with pre-certification and customer support.

Technical Session A: Die-to-Die and Advanced Packaging

Tuesday 13 May 14:30 – 16:30

A.1 CDM & CC-TLP on Bare Dies Fabricated in Leading-Edge FIN-FET Technology Nodes

Ellen Merkel, Heinrich Wolf, Fraunhofer EMFT; Bahar Youssefi, David Burnell, Cadence

This poster presents a comparison between CDM and CC-TLP testing on bare die intended for implementation in multiple chip modules. The DUT It discusses the difficulties of CDM testing on bare die and present the best practice for testing chiplets with CC-TLP.

A.2 Study of the Impact of Different Parameters on the CC-TLP Waveform

Vladislav Bukhanevich, Ellen Merkel, Heinrich Wolf, Fraunhofer EMFT

The poster analyzes the impact of various parameters on the CC-TLP waveform. The selected parameters are: distance between the Ground Plane and the metallic plane below the DUT, placement of the DUT relatively to the planes, size of the DUT, length of the contact needle and the pulse width.

A.3 Evlauation of ESD Diode Performance in Sub-300nm Thin Si Substrate

Wen-Chieh Chen and Marko Simicic, imec

The poster analyzes the impact of various parameters on the CC-TLP waveform. The selected parameters are: distance between the Ground Plane and the metallic plane below the DUT, placement of the DUT relatively to the planes, size of the DUT, length of the contact needle and the pulse width.

A.4 ESD Risk Evaluations in 2.5D/3D IC Stacking with TCAD Simulation

Shane Lin, Piet Wambacq, Vrije Universiteit Brussel, Marko Simicic, Nicolas Pantano, imec

Memory latency limits advanced computing performance. 2.5D/3D stacking offers closer integration but ESD protection is crucial. We investigate contact discharge damage to gate oxide in receivers and transmitters, evaluating voltage stress in planar transistors and discussing ESD risk differences in internal I/Os.

A.5 Nanosecond ESD Robustness of Advanced Silicon Photonics Devices

Po-Yen Lin, Piet Wambacq, Vrije Universiteit Brussel, imec; Marko Simicic, Kristof Croes, Wen-Chieh Chen, imec

This study employs vfTLP measurements to predict the behavior of photodetectors under CDM stress, applying vfTLP pulse widths from 1ns to 10ns. The vfTLP IV characteristic will be compared and discussed in this work. This approach aims to enhance the industry's understanding of ESD risks associated with advanced packaging technologies.

A.6 Exploring Distributed ESD Protection With Low ESD Voltage Targets for Heterogeneous IC Packages

Liesl Spruyt, Dragomir Milojevic, Université Libre de Bruxelles, imec; Marko Simicic, Nicolas Pantano, imec

Distributed ESD protection circuits in 5.5D (combined 2.5D and 3D) technology IC packages could decrease the required area whilst minimizing the impact on performance. We explore the location, type of circuit and influence of distance between the ESD protection circuits through simulation.

A.7 Impact of Diode Overshoot for ESD Protection During D2D and D2W Bonding Process

Emanuele Groppo, Technische Universität München; Harald Gossner, Umair Ishfaq, Nicolas Richaud, Intel

Charged Device Model events during Die-To-Die and Die-To-Wafer bonding feature fast rise time current pulses that can cause ESD diode voltage overshoots due to forward recovery effect. Transient overvoltages pose a severe threat to thin gate oxides reliability, hence diode optimization is required to ensure safe operation of such interfaces.

Technical Session B: Simulation to Silicon

Wednesday 14 May 9:10 – 11:00

B.1 CMOS-Technology: ULL RC SCR Clamps Voltage Overshoot and Impact of Supply Capacitance

Nandha Kumar Subramani, Alain Loiseau, Globalfoundries

The IO design uses the Ultra-Low-Leakage SCR clamp along with Tie-Low victim: passes 4kV HBM but failed 250V CDM. The failure analysis show hot spot on the Tie-low victim. The IO design with large supply capacitance (helps to absorb the voltage overshoot) passed the 500V CDM target.

B.2 Modular ESD Protection for Distributed Fail Safe ESD Strategy

Chloe TROUSSIER, Johan Bourgeat, Sebastien Dedieu, Frederic Bailleul, STMicroelectronics

A modular fail safe protection using GGNMOS and diodes has been developed. Using building blocks, design can obtain custom protection without additional the design time. The protection was tested in standalone and in a network using TLP. Recommendations are given to use this device depending on the protection strategy chosen.

B.3 Withdrawn as a full poster

B.4 Method of ESD Characterization and Modeling of ESD Network for CDM Predictive Simulation

Nicolas Richaud, Umair Ishfaq, Ritesh Agarwal, Harshit Dhakad, Krzysztof Domanski, Robert Haeussler, Florian Klotz, Harald Gossner, Intel

Dedicated test structure was developed to characterize for overshoot ESD victim using ultrafast-TLP setup with 20ps current pulse risetime. Model of diode are adjusted to reflect forward recovery during fast rise time of CDM current. Testbench for CDM predictive simulation has been proposed.

B.5 - withdrawn

B.6 AI-Driven TLP Data Analysis – A Case Study

Hossein Hosseini, Mehrdad Nourani, UT Dallas; Theo Smedes, NXP Semiconductors; Charvaka Duvvury

We have evaluated TLP measurement data on 18 identical GGNMOS devices collected using a Kelvin setup. We have demonstrated the proof of concept that unsupervised machine learning (ML) techniques (e.g. clustering) can be utilized to identify the data integrity and group devices based on their behavioral patterns.

Technical Session C: Latch-Up, GaN, and SEED

Thursday 15 May 15:00 – 16:50

C.1 A Case Study on ESD Trigger Circuit Latch-On Prevention

Marcin Grad, Paul Hendrik Cappon, Jian Gao, Sander Sluiter, Damien Fournier, NXP Semiconductors

We present two solutions for a latch-on mechanism leading to silicon failure. The problem is associated with leakage of trigger circuit device, which can prevent switching-off of the bigFET. Measurements and simulations show occurrence of latch-on and its sensitivity for various parameters as well as effectiveness of solutions.

C.2 Investigations of Transient-Induced Latchup in DTCO/STCO Technology Options

Kateryna Serbulova, Wen-Chieh Chen, Marko Simicic, Dimitri Linten, imec

The latch-up risk is still considered as one of the major reliability concerns in the state-of-the-art CMOS technologies for I/O applications. However, TLU immunity can be triggered by the fast transient events of a different nature. In this work, the TLU is evaluated for different pulses in DTCO/STCO scaling options.

C.3 Development of a New Latch-Up Measurement System for Advanced LSIs

Teruo Suzuki, Kazuya Okubo, Hiroyuki Koike, Socionext; Hideaki Miura, Masanori Sawada, Hanwa Electronic Ind. Co., Ltd.

Latch-up testing on large SoCs can induce currents over 100A, risking thermal runaway. Socionext has built the world's first fully JEDEC-compliant measurement system by integrating its thermostat-controlled socket, Hanwa's latest equipment, and a jointly developed temperature control program. This system has successfully conducted latch-up tests on multiple SoCs exceeding 100A.

C.4 System-Level ESD Characterization for CAN-Transceiver using Modular SEED Board

Kendrik Emkel Ginting, Michael Ammer and Barak Hasan Kara, Infineon

CAN Transceiver in its application is not a standalone device, but a part of a system with other components. The system-level ESD characterization can done using Modular SEED Board. Two different CAN-Transceiver ICs and TVS Diodes are investigated. The result is then used for comparison of system-level ESD model.

C.5 How to Develop ESD Robust Systems in an Efficient Way?

Barak Hasan Kara, Michael Ammer, Kendrik Emkel Ginting, Infineon

Goal is achieving Effective Co-Design of IC, external ESD by following SEED using simulation. It is discovered that missing information about ESD behavior of IC-Pins and external protection devices leads to misdesign. We discovered that external circuitry, PCB layout influence ESD robustness of system, which can be foreseen using simulations.

C.6 ESD Characterization in D-mode GaN RF Devices for RF ESD Protection Design in IC Consideration

Wei-Min Wu, Chin-Ya Su, Dongyang Yan, Bertrand Parvais, Nadine Collaert, imec

In this abstract, first VF-TLP measured results of G-S Schottky diodes in GaN RF HEMTs and inductors are revealed. With the size splits in the devices, discrepant ESD performance can be observed. Comprehensive SPICE simulations and more measurement results will be explored in the full poster.

C.7 ESD HBM Robustness Response to Barrier Layer Conditions in Schottky-based GaN-on-Si HEMTs

Chin-Ya Su, Partrick Reynaert, imec, KU Leuven; Wei-Min Wu, Hao Yu, imec; Bertrand Parvais, Nadine Collaert, imec, Vrije Universiteit Brussel

The wafer-level human-body-model (HBM) testing are conducted in the two different barriers (InAlN and AlGaN) of GaN HEMTs. The measured results of HBM robustness between InAlN and AlGaN are compared in this abstract and the comprehensive analysis with more measured and simulation data will be revealed in the full poster.

Discussion Groups: Session A

Tuesday 13 May 19:00 – 20:30

A1: ESD protection for RF and very-high-speed wireline IOs.

Moderator: Elyse Rosenbaum, University of Illinois; Jennifer Schütt, Nexperia

JEDEC Publication 157A (“Recommended ESD-CDM Target Levels”) proposes worrisomely low target levels for RF and High-speed serial IOs, e.g., a 1-A, 150-V CDM target for a 1-cm2 RFIC and a 2-A, 125-V target for a 25 cm2 processor or FPGA with SerDes operating above 56 Gbps. This working group will discuss the following three questions. (1) Do those low target levels compromise yield or increase field returns? (2) Does co-design of the ESD protection and IO circuitry enable us to achieve higher protection levels without compromising performance? (3) What data do ESD designers need to confidently design to a given target level without indulging in overdesign? Overdesign refers to the practice of conservatively over-sizing the ESD protection to guarantee it will provide adequate protection.

A2: Is it time to revise Latch-Up standards for today’s industry requirements?

Moderator: Vlatko Galic, University of Zagreb, FER

As semiconductor technologies continue to evolve, traditional latch-up (LU) testing methodologies face increasing challenges. The JESD78 standard has long been the industry’s benchmark, but with the rise of FinFETs, advanced HV technologies, and increasingly complex system architectures, the question arises - does it still fully address modern reliability concerns?
Lower operating voltages (<2V), higher voltage applications (>100V), and the growing demand for transient LU testing highlight potential gaps in existing standards. Furthermore, while industry perception still sees value in JESD78, there is a need to assess whether its coverage is sufficient for today’s diverse product landscape. Are there real-life failure mechanisms that remain unaccounted for? Should we redefine pass/fail criteria to include soft failures and functional degradations?
This discussion group aims to explore these questions, gather insights from industry experts, and evaluate whether it is time for an industry-wide revision of LU testing methodologies to better align with emerging challenges.

Report on DG Session A: Wednesday 14 May 2025, 11:45 - 12:10

Discussion Groups: Session B

Wednesday 14 May 19:00 – 20:30

B1: Future Challenges of CDM qualification

Moderators: Andrea Boroni, STM; Heinrich Wolf, Fraunhofer EMFT

The trend to integrate several dies/chiplets, sensors and even extremely sensitive electrooptical components with almost no protection into Systems in a Package (SiP) or Multi-Chip Modules (MCM) also requires a test method to evaluate the single components or chips prior to their integration into the complete system or module. In addition, high-speed device interfaces are capable to sustain low level current. The Capacitively Coupled Transmission Line Pulsing (CC-TLP) has demonstrated to be a possible solution in terms of reproducing the failure mode at a precise stress level and became a standard practice in 2022. Unlike the established standard test method Charged Device Model (CDM) the CC-TLP allows an extremely reproducible stressing also at low stress levels. In addition, there are several methods which will be described in a future technical report of the standardization body and which may also have the potential to overcome future testing challenges. This discussion group will try to answer questions like: What are the differences between CC-TLP, these additional CDM like test methods and FI-CDM, and how can we correlate their results?

B2: How can machine learning and AI techniques improve modeling methodologies to improve the accuracy and efficiency of ESD simulations?

Moderator: Renaud Gillon, Sydelity

With ICs becoming increasingly complex, the traditional ESD simulation and test methodologies are facing growing challenges in accurately predicting, efficiently identifying and resolving ESD related failures. With the rise of machine learning (ML) and artificial intelligence (AI), there is an opportunity to explore how these techniques can be used to enhance the modeling approaches, improve simulation efficiency, and accelerate testing.
This discussion group aims to address key questions such as:

- The potential of AI/ML in improving ESD modeling and simulation accuracy.
- How data-driven techniques can complement or enhance physics-based approaches?
- Can AI help reduce computational costs while maintaining accuracy?
- Can AI help reduce test time?
- What data requirements and validation challenges exist for AI/ML based approaches?
- Practical use cases, industry adoption, and future research directions.

By bringing together experts from industry and academia, this session will explore the current state of AI/ML in ESD modeling, identify practical implementation strategies, and discuss the future of intelligent simulation methodologies.

Report on DG Session B and C: Thursday 15 May 2025, 17:05 - 17:50

Discussion Groups: Session C

Thursday 15 May 13:00 – 14:30

C1: How does ESD design impact EMC performance in automotive ICs?

Moderator: Patrice Besse, NXP

As automotive ICs become more complex and operate in increasingly demanding environments, ensuring both robust ESD protection and excellent EMC performance has become a critical challenge. While ESD protection is essential for reliability, it can also influence EMC performance for both emission and immunity, leading to trade-offs that designers and ESD engineers must carefully navigate.

This discussion group will explore:

- The interplay between ESD protection strategies and EMC performance in automotive ICs.
- Design trade-offs and challenges in achieving both robust ESD protection and high EMC performance
- Measurement techniques and simulation methodologies for assessing EMC impacts.

Industry trends, evolving standards, and best practices for optimizing ESD/EMC co-design.

C2: ESD roadmap in advanced packaging technologies

Moderator: Harald Gossner, Intel

2.5D and 3D bonding technologies are key for future AI solutions combining complex compute dies with sensor or analog dies and stacks of memory dies. However, ESD test engineers face massive challenges when testing bare dies/wafers with tens of thousands of µ-bumps, as well as designers do, when designing ESD protection of very limited size and capacitance budget. To tackle these challenges, the Industry Council on ESD target levels published the White Paper 2 Part2 in 2023. The suggested CDM levels for heterogeneous integration are 30 V and below down to 5 V, on a roadmap toward 3V in 2028. This discussion group will try to answer questions like: How low will the protection level need to go? What CDM levels can ESD control achieve in 2.5D and 3D bonding processes? What is the test for characterization and for qualification of D2D interfaces? What are appropriate protection solutions for leading edge nodes?

Report on DG Session B and C: Thursday 15 May 2025, 17:05 - 17:50

Schedule

Monday 12 May 2025

12:00	13:00	Lunch
13:00	14:30	Tutorial: Optimization of ESD and Signal Integrity on System Level for Automotive Applications, Andreas Hardock, Sergej Bub, Nexperia
14:30	15:00	Break
15:00	16:30	Tutorial: Optimization of ESD and Signal Integrity on System Level for Automotive Applications, Andreas Hardock, Sergej Bub, Nexperia
16:30	17:00	Break
17:00	18:00	Seminar: ESD design support in practice: a few real-life examples, Gijs De Raad, NXP Semiconductors
18:00	19:00	Dinner
19:00	20:00	Welcome entertainment
20:00	21:30	Networking / Social Gathering

Tuesday 13 May 2025

07:30	09:00	Breakfast
09:00	09:30	Welcome speech
09:30	10:30	Keynote: ESD – Expectations, Surprises and Discoveries, Karim T. Kaschani, Robert Bosch GmbH
10:30	11:00	Break
11:00	12:00	Invited talk: Challenges in ESD discharge risk reduction to support Advanced Packaging Manufacturing Roadmap, Philippe Muller, Suss MicroTec
12:00	13:00	Lunch
13:00	14:00	Seminar: ESD risks during PCB assembly processes, Istvan Kovalik, Harman
14:00	14:30	Break
14:30	15:30	Technical session A: Die-to-die and Advanced Packaging
15:30	16:30	Poster Discussion A: Die-to-die and Advanced Packaging
16:30	17:00	Break
17:00	18:00	Invited talk: Applications of Machine Learning to Microelectronics (and ESD) Design, Elyse Rosenbaum, University of Illinois Urbana-Champaign
18:00	19:00	Dinner
19:00	20:30	Discussion Group Session A (Parallel sessions) A1: ESD protection for RF and very-high-speed wireline IOs A2: Is it time to revise Latch-Up standards for today's industry requirements?
20:30	21:30	Networking/ Social Gathering

Wednesday 14 May 2025

07:30	09:00	Breakfast
09:00	09:10	Announcements
09:10	10:00	Technical Session B: Simulation to Silicon
10:00	11:00	Poster Discussion B: Simulation to Silicon
11:00	11:15	Break
11:15	11:45	Seminar: ESD in the automotive industry– a proposal for lowering risks during system level ESD qualification and reducing component cost, Steffen Holland, Nexperia
11:45	12:10	Report on DG Session A
12:10	13:10	Lunch
13:10	18:00	Open time - Prearranged Activities or Welcome to Explore on Your Own
18:00	19:00	Dinner
19:00	20:30	Discussion Group Session B (Parallel Sessions) B1: Future Challenges of CDM qualification B2: How can machine learning and AI techniques improve modeling methodologies to improve the accuracy and efficiency of ESD simulations?
20:30	21:30	Networking/ Social Gathering

Thursday 15 May 2025

07:30	09:00	Breakfast
09:00	09:10	Announcements
09:10	09:40	Industry Council Report
09:40	10:30	Invited talk: Overcoming ESD and EMC Challenges in Advanced Optical Sensing, Christian Stockreiter, ams OSRAM
10:30	11:00	Break
11:00	12:00	Invited talk: Make your EMC & ESD solutions compatible!, Patrice Besse, NXP Semiconductors
12:00	13:00	Lunch
13:00	14:30	Discussion Group Session C C1: How does ESD design impact EMC performance in automotive ICs? C2: ESD roadmap in advanced packaging technologies
14:30	15:00	Break
15:00	15:50	Technical Session C: Latch-Up, GaN and SEED
15:50	16:50	Poster Discussion C: Latch-Up, GaN and SEED
16:50	17:05	Break
17:05	17:50	Report on DG Sessions B and C
17:50	18:00	Closing
18:00	19:00	Dinner
19:00	20:00	Networking/ Social Gathering

Friday 16 May 2025

07:30	09:00	Breakfast
09:00	11:00	Check Out

Be sure to visit tabletop exhibits by

D & Tsa Bt.

YOUR PARTNER IN INDUSTRIAL ELECTRONICS

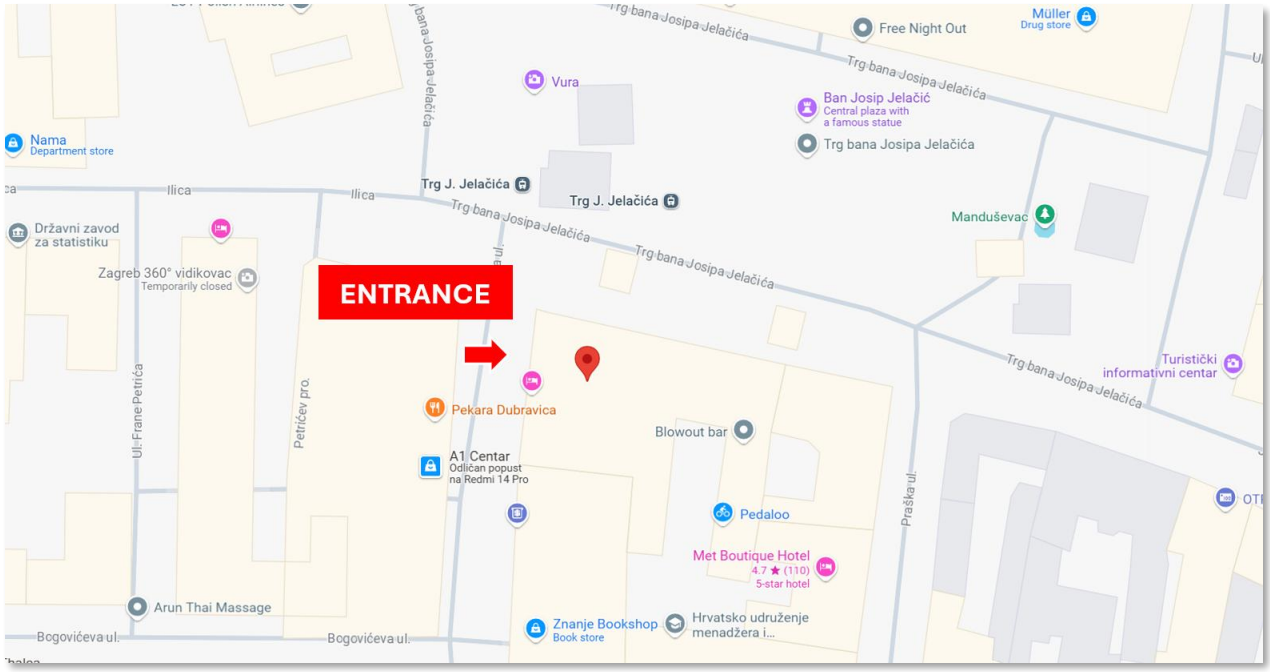
D és Tsa Bt. is a 100% Hungarian-owned company operating since 1996 under the EN ISO 9001:2015 quality management system. Our main focus is establishing and maintaining ESD protection by providing products, training, audits, and measurements. We also support the setup and maintenance of cleanroom environments. Our portfolio includes soldering technology products, hand tools, occupational safety equipment, and ergonomic solutions. We have four production facilities in Hungary, manufacturing our ESD garments and ESD entrance testers. Our goal is to build long-term cooperation with our partners.

DLB

AijGO

Directions to reach the IEW 2025 venue

The address of the venue is **Gajeva ulica 1, Zagreb**
This address is also known as “Gajeva 1” or “Ljudevita Gaja 1”.

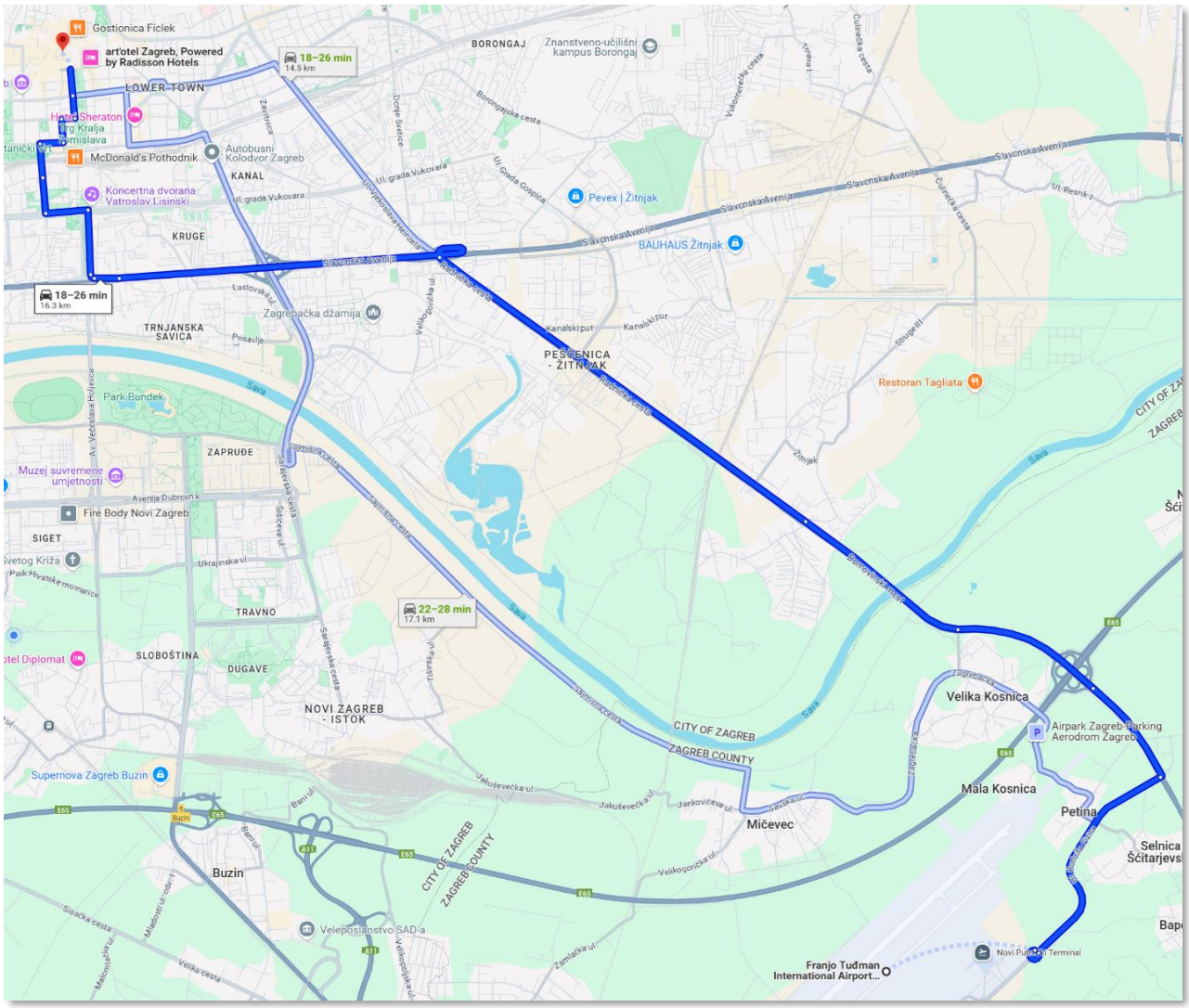


From the airport to the hotel	
Option 1 – Taxi	Option 2 – Public Transport

Option 1 – Taxi

Taxi (<30 min)

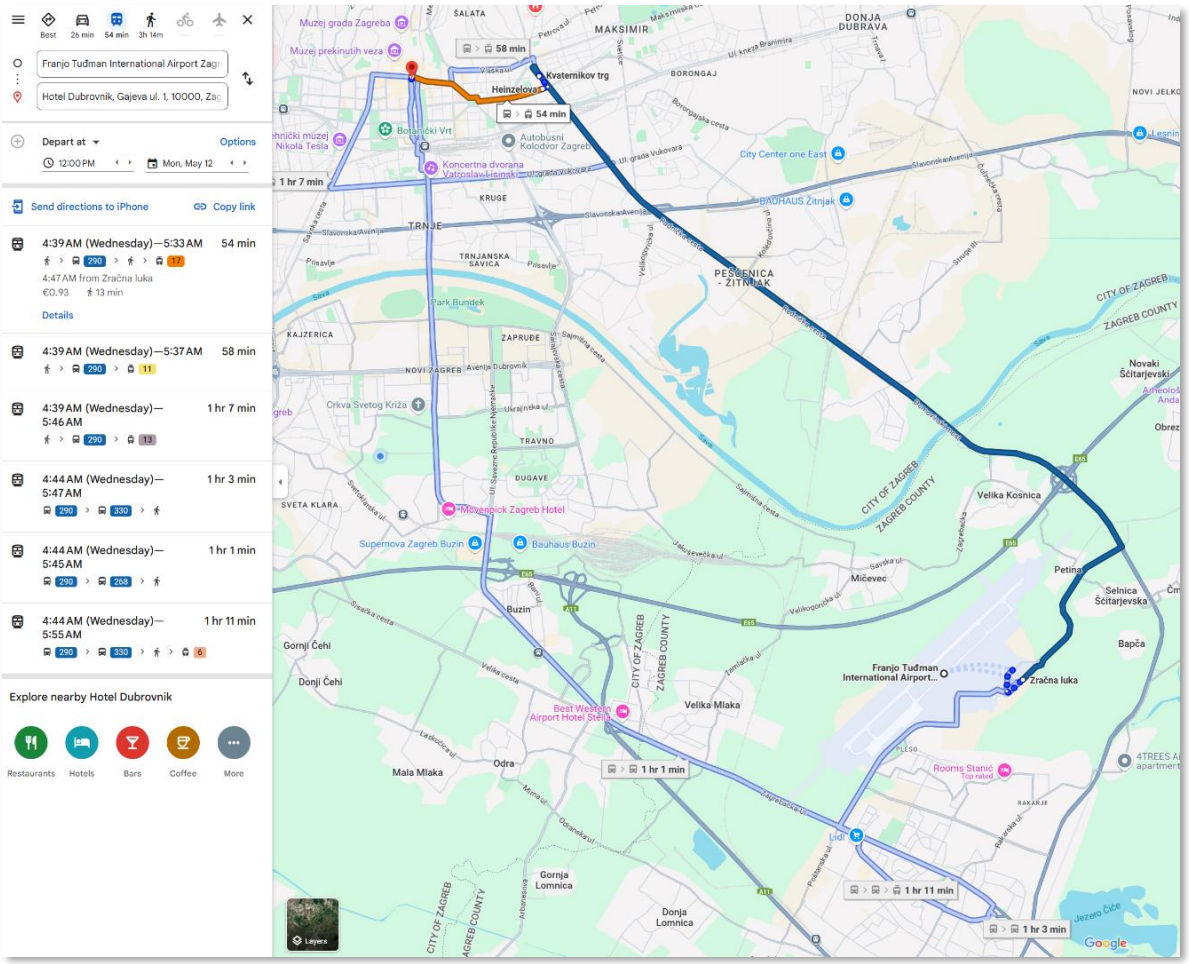
- Take a taxi at the airport
- Call Zagreb taxi at number +385 1 1717
- Use Zagreb taxi, uber, bolt or wizi taxi app



Option 2 – Public Transport

Bus and tram (~60 min)

- Option 1 (https://www.zagreb-airport.hr/en/passengers/to-from-the-airport/by-airport-shuttle/89)
  - Take Pleso prijevoz shuttle bus service
    - Leaves from the airport to the Zagreb Central bus station
  - From the central bus station take tram number 6 to the north (mountain direction)
- Option 2
  - Public transportation service of Zagreb (ZET)
    - Bus line 290 operates between Kvaternik Square and Velika Gorica, with a stop at Zagreb Airport in each direction. Timetable for the bus line 290 can be found at ZET's website



2025 International ESD Workshop (IEW)

12-16 May 2025

Hotel Dubrovnik
Gajeva ulica 1
Zagreb, Croatia

Registration Fee*: $1,995
Discount before March 21, 2025: members $1,795 / non-members $1,895

*The registration fee includes full workshop attendance, materials, meals Monday dinner through Friday breakfast, and lodging Monday night through Thursday night.

No lodging required? Use discount code COMMUTER2024 to receive a $400 commuter discount.

Guest Fee: $550**

** Guest stays in the same room and attends meals. No attendance is permitted at the conference sessions.

Multiple Attendee Discount: Save $100 per person when 5 or more colleagues from the same company register. Contact info.eosesda@esda.org for your discount code.

Student Discount: Save 50% when you provide your school ID confirming current enrollment to info.eosesda@esa.org. A discount code will be provided upon confirmation.

Register online: https://cvent.me/qlYDDl

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