2024

Asia-International Electrostatic Discharge Workshop
July 16-18, 2024

IEW-ASIA

Setting the Global Standards for Static Control!

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The Experience of First in-Person IEW in Asia

In the middle of July, we embrace a new IEW-Asia event co-located with the International Physical and Failure Analysis of Integrated Circuits (IPFA2024). Never change, IEW continues to provide a relaxed, invigorating atmosphere to present new work and engage in discussions about the latest issues confronting the ESD and EOS communities in its 17th year. In addition to everything IEW-Asia provides, IEW-Asia registrants can attend the full IPFA technical program (any technical session, invited talks, and keynote speakers), including the joint evening poster reception showcasing works from both conferences.

This year, the workshop retains the peculiar elements: 1 keynote speech, 2 discussion groups, 10 invited talks, and 2 technical presentation sessions with 12 exciting posters. Dr. Sia Choon Beng from FormFactor, Singapore, gives the keynote speech on improving wafer measurement techniques to overcome test challenges in semiconductor device reliability studies. Making accurate, traceable, and repeatable electrical measurements with a good wafer test probe system is crucial in studying CMOS device reliability. In his talk, he focuses on enhancing wafer-level characterization to help device reliability engineers make accurate and repeatable wafer-level measurements. Unlike the keynote speech, one of the strong interaction atmospheres at IEW comes from the discussion group sessions. This year, the 2 discussion group sessions are related to EDA tools in ESD applications and foundry ESD supports. These two sessions are led by Dr. Wei Gao from HiSilicon and Dr. Jack Zeng from GlobalFoundries, respectively.

In addition, the 10 Invited talks cover various ESD, latch-up (LU), and reliability fields, including design optimizations, testing methodologies, device/circuit simulations, and ESD environment control. Hanwa President Masanori Sawada gives a seminar on CDM basics and applications. Mr. Dunken Lee from Amazing IC gives a talk on system-level ESD protection design with TVS solutions in automotive applications. Professor Weiming Wang, Southwest University, provides insight into fully automatic synthesis flow on design optimizations of the ESD protection scheme in the ultra-wideband high-speed interface. Dr. Alwyn Rebello from GlobalFoundries discusses LU in high-voltage CMOS and BCD technologies. Professor Qiang Cui, Zhejiang University, provides the seminar on TCAD simulation for on-chip ESD protection analysis. Mr. Shinichi Yamaguchi from Shishido Electrostatic discusses the latest low-voltage ESD control ionizer technologies. Professor Pengpeng Ren, Shanghai Jiao Tong University, conducts his talk on aging and thermal assessment by hybrid graph networks. Lastly, Mr. Hiroyasu Ishizuka gives the seminar on component-level and system-level ESD design co-optimizations.

The core of the IEW technical program is the poster sessions, which provide an ideal forum for the participants to exchange ideas. This year, the 12 excellent posters have been arranged in two technique sessions. One session focuses on
the state-of-the-art ESD protection designs in HV technologies, chiplet interfaces, and system-level applications, and the other one has varied ESD/EOS/LU topics, including EDA verifications, device/circuit/system simulations, failure analysis, and prevention control. The sessions definitely give you comprehensive EOS/ESD aspects in this 3-day event. Nevertheless, every evening, casual networking and social gathering sessions can be the best place to connect you to the ESD family as well. On behalf of the 17th annual International ESD Workshop (IEW) Management Team, we sincerely hope you join us at the 2024 IEW-Asia in Singapore.

Shih-Hung Chen,
IMEC,
General Chair
The silicon foundry industry envisions manufacturing GPU with 1 trillion transistors by 2030, 10 times as many devices as typical today, to support advanced AI applications. GenAI applications such as ChatGPT’s public access are made possible through innovations in efficient machine-learning algorithms, the availability of massive data to train neural networks, and energy-efficient computing through the advancement of semiconductor device technology. Rising demands for GenAI applications continue to drive the development of advanced-node devices to build GPUs. Gate length down-scaling to beyond sub 3 nm regime, new materials, and development of new architecture such as nanosheet transistors result in area and power-efficient advanced-node transistors with very small on-state drain-source resistance, making it very challenging for test engineers to perform precise and consistent wafer measurements. Making accurate, traceable, and repeatable electrical measurements with a good wafer test probe system is crucial in studying advanced-node device reliability and ESD performance.

Threshold voltage measurements are necessary to assess transistor performance stability over time. Measuring threshold voltage under different operating and stress test conditions allows degradation trends to be identified, indicating potential reliability issues. Leakage current measurements provide insights into the integrity of gate oxide layers and junctions, revealing any defects or degradation affecting device reliability. Interface state density with flicker noise and RTS noise measurements help assess the quality of the semiconductor-dielectric interface, highlighting any interface traps that could lead to performance degradation. Temperature-dependent measurements are also essential to understand the impact of thermal stress on device reliability. These repeated electrical measurements, over time, provide comprehensive insights into advanced node device reliability, enabling proactive measures to mitigate potential failure mechanisms ensuring long-term device performance. This talk focuses on
improving wafer characterization and measurement techniques to help test engineers make precise and consistent wafer measurements.

**Dr. Choon Beng Sia** is an SSG Fellow conferred by the President of the Republic of Singapore. He received a doctorate in Electronics Engineering from Nanyang Technological University, Singapore. At MIT, Dr Sia studied Data Science and Big Data Analytics. In his current work at FormFactor as a Technical Director, Dr Sia develops solutions to address emerging semiconductor wafer test and measurement challenges. His research interests include designing, testing, and modeling silicon-based RF devices, THz calibration and measurements for beyond 5G and IoT applications, photonics tests for optical communication applications, and applying machine learning and AI to wafer tests. Dr. Sia serves on the IEEE MTT-3 technical committee that develops standards and best practices for RF measurements, and he is also on the MTT-3 speaker bureau, specializing in wafer RF tests. Through Enterprise Singapore, the Singapore National Standards Board, Dr Sia represents Singapore as a Technical Expert in various IEC technical committees, developing standards for MEMs, optical, and wafer-level reliability tests for semiconductor devices. He is a frequently invited speaker and organizer of IEEE workshops and international test forums and holds 13 international patents. Dr. Sia has published in more than 50 scientific journals and conference publications and has received multiple best paper awards at international conferences and symposiums.
IEW Seminar I

Tuesday, July 16, 2024
17:30 - 18:30

CDM Basic & Application
Masanori Sawada, HANWA Electronic Ind. Co., Ltd.

The seminar covers the basics and applications of the CDM test. The basics of the CDM test explain that the simulation of the CDM waveform obtained from the simplified LCR equivalent circuit can be performed and that the CDM waveform is affected by the measurement environment. Applying the CDM test in wafer and the new test method low impedance contact-CDM are explained in applying the CDM test.

Masanori Sawada received his MS from Wakayama University in March 1998. He joined Hanwa Electronic Ind. in April 1998. Masanori is with the technical group of ESD equipment. He designed multiple testers in Hanwa, including CDM, TLP, and Wafer-ESD.

He is a member of the RCJ symposium committee in Japan. At the 2009 RCJ Symposium, he received the Best Paper for his paper on CDM waveforms. He is also a member of JEITA's System Level ESD Working Group. He is the president of Hanwa.
IEW Seminar II

Wednesday, July 17, 2024
08:30 - 09:25

TCAD Simulation for On-Chip ESD Protection Analysis
Qiang Cui, Zhejiang University, Hangzhou, China

Electrostatic discharge (ESD) is a major threat to integrated circuits (ICs)' reliability, and the technology computer-aided design (TCAD) simulation is the key method to analyze ICs' on-chip ESD protection ability. To be ready for production, the ICs must pass various ESD test standards, including MIL-STD-883, IEC 6100-4-2, and AEC-Q100, as well as transmission line pulsing with different rise times and pulse widths. The TCAD simulation work reported in the existing literature typically only focuses on a narrow scope, such as steady state current-voltage (IV) characteristics, transient analysis, electron-hole contour, or temperature contour. The fragmented research on TCAD simulation failed to analyze on-chip ESD protection systematically. The paper developed a thorough TCAD simulation method covering all major ESD standards and models to fill this research gap. It elaborated the method with a silicon controlled rectifier (SCR) based protection device design. The abovementioned simulation method includes steady-state analysis, transient analysis, temperature effect, and circuit-device mixed-mode setup. This TCAD simulation method can effectively help designers analyze and design protection devices for ICs against ESD related reliability issues.

Dr. Qiang Cui is the Tenure-Track Professor of Zhejiang University's College of Integrated Circuits. Dr. Cui has over 15 years of experience in the semiconductor industry (Apple, Qorvo) and research institutes (Massachusetts Institute of Technology, University of Central Florida). He has led or designed several strategic integrated circuits widely used in wireless products. Dr. Cui is a senior member of IEEE and serves on the reviewer panel of several IEEE journals such as IEEE Transaction on Electron Devices, IEEE Electron Device Letters, IEEE Transaction on Device and Materials Reliability, Solid State Electronics and Microelectronics Reliability, and so on. Dr Cui's current research interests include automotive ESD protection, wireless communication ICs, high speed I/O circuits, and mixed signal IC design.
Understanding Specific Latchup Scenarios and Mitigation Methodologies in CMOS and BCD Technologies

Alwyn Rebello, GlobalFoundries, Singapore

This talk briefly overviews conventional and specific latch-up scenarios and latch-up prevention techniques in CMOS technologies. The discussion focuses on latch-up behavior in parasitic SCR detector structures with grounded N-Well (GNW) in CMOS technologies. In particular, the effect of design parameters such as injector to detector spacing, GNW to nearby Nwell (of a PMOS) distance, and various guard ring combinations on latchup robustness is presented. Furthermore, we discuss how GNW impacts the latch-up robustness of high voltage designs in BCD technology under different Deep-Trench-Isolation (DTI) and N-EPI pickup configurations (NCOMP).

Alwyn Rebello received an M.Sc. in Physics from Cochin University of Science and Technology, Kerala, India, in 2005 and a Ph.D. from the National University of Singapore (NUS), Singapore, in 2011. From 2011-2014, he worked as a postdoctoral research fellow at Montana State University and the University of Miami, U.S.A. Later, Alwyn continued his postdoctoral research on thin film-based resistive memory devices in the Department of Electrical and Computer Engineering, NUS, from 2014-2017. In 2017, he joined GLOBALFOUNDRIES, Singapore, where he is involved in developing ESD and latch-up protection for various technology nodes (0.18 µm – 28 nm). His research interests include ESD device development and latch-up prevention for various automotive and RF applications.
Design for reliability has become a critical aspect of circuit design under advanced technology. Among the reliability mechanisms, device aging in the front end of line and thermal-sensitive interconnect electromigration (EM) in the back end of line (BEOL) have been paid more attention. The device aging effect in standard cells of digital circuits increases the path delay, thus leading to timing violation errors. The aging effect is conventionally considered by setting a guard band in the circuit design. With the rapid evolution of process technology, the design margin left for the guard band decreases remarkably, posing challenges to the sign-off of circuit design. Instead, developing an aging library of standard cells becomes an effective way to include the impact of aging in the timing analysis inherently. However, due to the complicated application scenario, it is quite time-consuming for aging delay assessment of standard cells by Spice simulation under various conditions. It is necessary to accelerate this procedure in the aging-aware circuit design.

On the other hand, with the increase of device leakage current and aggressive downscaling of interconnect metal pitch, the resulting metal Joule heating leads to an evident hotspot in the layout, accelerating the EM failure. Conventionally, the thermal profile is assessed by commercial EDA tools like Totem and RedHawk. However, due to the same reasons as aging, thermal simulation is also time-consuming under complicated scenarios, especially under design iteration.

This work proposes a novel framework for rapid device aging-aware timing analysis and thermal-aware interconnect EM analysis. This framework harnesses the capabilities of Hybrid Graph Neural Networks to effectively capture cell structural details and extract cell delay and leakage-related information, enabling a straightforward mapping from operational conditions to specific cell aging delays and leakage current. It incorporates a Relational Graph Convolution Network (R-GCN) for modeling the complex relationships between nodes and a Graph Attention Network (GAN) for assessing the relative importance of each node based on their types. This integrated approach significantly streamlines the process of aging-aware timing analysis, offering a substantial improvement in both speed and
accuracy for digital circuit design. In addition, the concept of "characteristic temperature of the cell" can be determined with the output leakage current. Therefore, the thermal profile of the digital circuit can be developed with the standard cell as a "pixel", which can improve the resolution of the thermal-aware EM analysis.

Our framework has a 5% to 28% higher average prediction accuracy and better generalization ability on new cells than other benchmark networks. Compared with the conventional method, our framework greatly reduces time consumption and achieves an average acceleration ratio of 600 on prediction tasks of many cell structures and input conditions.

**Pengpeng Ren** received a Ph.D. from Peking University, Beijing, China, in 2016. After graduation, he worked as a staff engineer at HiSilicon Technologies. He has been an Associate Professor with the Department of Micro/Nanoelectronics at Shanghai Jiao Tong University since 2021. His current research interests include nanoscale CMOS reliability physics, design for reliability, and AI for EDA. He has authored or co-authored over 70 scientific papers, including papers published in IEDM, VLSI-T, IRPS, IEEE TCAD, and TED.
Advanced Automotive TVS Solutions: Mitigating Transient Voltage for Enhanced System Protection against ESD/EOS
Dunken Lee, Amazing Microelectronic Corporation

Automotive electronics have undergone significant advancements to ensure safety, environmental sustainability, and the seamless integration of state-of-the-art technologies. Notably, the proliferation of driver-assist technologies has substantially augmented vehicle and driver safety. Furthermore, the eagerly anticipated autonomous driving technology promises to relieve individuals from the burdensome task of manual driving.

The escalating integration of electronic modules into automotive systems brings about a convergence of benefits, offering enhanced comfort and security for vehicle users while concurrently presenting noteworthy concerns regarding reliability within the automotive environment. Consequently, automotive electronics designers are confronted with formidable challenges. These challenges encompass formulating robust protection methodologies to mitigate a spectrum of electrical hazards, including but not limited to electrostatic discharge (ESD) and transient electrical disturbances impacting power rails and data lines in automotive electronic circuits. The effective management of transient surges, which potentially jeopardize automotive electronics, emerges as a daunting imperative in the design process of automotive systems. Thus, vigilance and implementing precautionary measures are imperative wherever electronic modules are deployed in the automotive domain.

Automotive transient voltage suppressors (TVS) are indispensable components within the automotive sector, safeguarding electronic circuits from detrimental transient energy from voltage and current fluctuations. These automotive TVS devices leverage robust silicon TVS technology to clamp voltage spikes, thereby effectively attenuating transient amplitudes to safe levels. This presentation provides comprehensive insights into various facets of automotive technology development, encompassing diverse types and standards of automotive transients. Furthermore, it elucidates the functionalities and characteristics of automotive TVS devices, delineating their pivotal applications within automotive electronic systems.
Dunken Lee, born in Taiwan, R.O.C. in 1978, holds a B.S. from the Department of Electrical Engineering at National Cheng-Kung University (NCKU) in Tainan, received in 2000. He further pursued his education and obtained an M.S. from the Institute of Electronics at National Chiao-Tung University (NCTU) in Hsinchu, Taiwan, in 2002. In 2005, Dunken successfully passed the NCTU EE Ph.D. program entrance exam. During his military service in 2003, Dunken Lee joined Silicon Integrated Systems (SiS) Corporation, located in the Science-based Industrial Park in Hsinchu, Taiwan, R.O.C. There, he worked as an ESD protection circuits & latch-up prevention design engineer. His responsibilities included designing ESD protection circuits and preventing latch-up issues. His contributions in this role led to the publication of six ESD papers in renowned international EE journals and conferences.

Additionally, he holds eight patents for IC ESD protection design. His master's thesis received the prestigious Dragon Thesis Award from Acer Foundation, Taiwan, in 2002. Since 2007, Dunken Lee has been an ESD application senior manager at Amazing Microelectronic Corp., where he has made significant contributions to the field. He has been invited multiple times to be an ESD speaker at the Taipei Tze Chiang Foundation of Science and Technology and at Taiwan ESD conference tutorials. Currently, he holds the senior manager position at Amazing and remains dedicated to furthering advancements in electronic protection.
On-Chip Spiral Arbitrarily Tapped Coil Automatic Synthesis (OSTAS) and Its Application to Ultra-Wideband ESD Protection Circuits

Haiming Wang, Southeast University, Nanjing, China

With the evolution of information and communication technologies, the transmission rates of signals are becoming increasingly faster at the input and output ports of integrated circuits (ICs). On-chip ESD protection design for modern VLSI chips with high-speed interface ports becomes very challenging in achieving ultra-wideband performance while being robust against ESD threats. This talk presents an overview of design challenges and solutions for on-chip high-speed ESD protection. Design techniques such as tightening the ESD design window, optimizing ESD cells at the best efforts, and compensating ESD parasitics with passive devices are analyzed and compared. An on-chip spiral arbitrarily tapped coil automatic synthesis (OSTAS) was developed to compensate ESD parasitics for the best possible signal integrity in the viable design space to achieve ultra-wideband performance. OSTAS features a machine-learning-assisted optimization algorithm that skillfully combines prior domain knowledge and data-driven technique. With this algorithm, OSTAS achieves a fully automatic synthesis flow of on-chip spiral arbitrarily tapped coils that steadily converge to the global optimum solution with competitive sampling space and computation resources. Optimization cases by OSTAS for Tcoil with one-tapped ESD diode connection, Picoil with two-tapped ESD diode connections, and even distributed ESD protection schemes are studied in this talk to validate the smart and powerful candidate for the best possible high-speed ESD protection design explorations.

Haiming Wang was born in 1975. He received his B.S., M.S., and Ph.D. in electrical engineering from Southeast University, Nanjing, China, in 1999, 2002, and 2009, respectively. Haiming joined the School of Information Science and Engineering and the State Key Laboratory of Millimeter Waves, Southeast University, Nanjing, China, in 2002 and is currently a Distinguished Professor. He has authored and co-authored over 50 technical publications in IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION and other peer-reviewed
academic journals. Prof. Wang has authored and co-authored more than 80 patents, and 55 patents have been granted. He was awarded twice for contributing to the development of IEEE 802.11aj by the IEEE Standards Association in 2018 and 2020. His research interests include Intelligent Microwave Engineering (IME) and RFIC Design Intelligence Technologies.
When the ESD problem started, the main issue was HBM (Human Body Model). In response, basic ESD countermeasure guidelines were developed based on various findings. However, electrostatic damage to electronic devices did not stop. Because the current failure mode has shifted from HBM to CDM (charge device model) and other modes, and the control voltage is going down around ±30V, this presentation covers not only the importance of CDM countermeasures but also countermeasures against metal-to-metal contact, CBE (charge board event), and SDM (socketed device model).

For ionizers as countermeasure products, this presentation explains not only the required ionization decay time and ion balance but also the need to reduce induced charging from discharge electrodes in bar-type ionizers, the uniformity decay time and ion balance (IB) generated by each electrode, and the need to reduce dust emission from fan-type ionizers. We have reached good uniformity and low IB conditions. There are less than ±30 V by dissipative coating and around ±10 V by dissipative material casing.

Shinichi Yamaguchi has over 37 years of experience in the static electricity industry, providing technical guidance on various static electricity measurements, countermeasures for static electricity problems, and proposals for developing countermeasures and measuring instruments by ESD measuring instrument manufacturers and ionizer manufacturers.

He has been involved in the ESD market in Japan for more than 33 years and has conducted seminars and factory diagnoses at major semiconductor, electronic device, and LCD-related companies. He has also been active in the Asian market since 1998. He has conducted seminars and factory diagnoses for LCD, HDD, and semiconductor-related companies in the same way as in Japan.
Recently, ESD design at the component level has been the subject of good discussion, and several basic ESD design methodologies have been derived under ESD designer discussions and many experiments. Among these, the design method using an active clamp has been widely used because it is easy to handle comprehensively in the component level ESD design and has a good achievement for the component level ESD test. Also, it has produced very effective results for ESD events in semiconductor components' handling and assembly processes. However, it cannot cover all system level ESD events and failures.

However, customers of general electronic applications/devices often demand that semiconductor component designs be improved against system level ESD to prevent semiconductors from being damaged in the customer's manufacturing and the field. On the other hand, my experiences of analyzing several field returns and according to the committee's analysis, in focusing on the device hard damage that occurred in the manufacturing and the field, the main damage factors look like to summarize two stress events caused by CBE and CDE, under cellphone business and excluding EOS stress.

This talk discusses the basic component-level ESD design methodologies, analyzes system level ESD events in the manufacturing and the field, and then explores the causes of semiconductor component failures and improvement design methodologies.
Hiroyasu Ishizuka received a BS in electrical engineering from the Shibaura Institute of Technology, Tokyo, Japan, in 1983, and he joined Hitachi and worked in the device reliability field in the quality assurance dept. Since 1992, he has worked on the development and design group of ESD protection devices/circuits, including system ESD events and was a manager while he worked at Renesas Technology Corp and Renesas Electronics Corp. He is currently working on driver IC ESD design and panel/phone system ESD analysis at Synaptics Japan G.K. (2015-2020), Maxwell Japan Co., Ltd. (2020-2023) and YITOA Japan Co., Ltd. (now). He currently focuses on system level ESD testing versus CBE versus real-world ESD event phenomena.

He was a core Industry Council on ESD Target Levels member from 2006 to 2023. He was also a core member of the ESD project group (PG) and chair of the system ESD analysis working group (WG) at JEITA (Japan Electronics and Information Technology Industries Association) until 2023.
Harmonization to/Justification for a Common Industry/Automotive CDM Stress Procedure of Single Zap Per Pin Per Polarity

Nobuyuki Wakai, Toshiba

Charged device model (CDM) testing for non-automotive IC products has been harmonized to single-zap (1-Zap) per pin per polarity in various worldwide standards. In contrast, the AEC (automotive) Q100-011/101-005 CDM standard test procedure zap count has remained at three times Zap (3-Zap). The recent advanced device pin count has significantly increased by 1000-2000+. This has made CDM test time unacceptably long, particularly for 3-Zap CDM testing, resulting in CDM testing being the time-critical path for automotive IC qualification. Discharge phenomena by 3-Zap under the same conditions as any IC pin should not happen if a protected area (EPA) complies with ESD control (ESDC) standards such as ANSI/ESD-S20.20. This indicates a breakdown of ESDC in the EPA. Six supplier companies worked together to compare the CDM pass/fail voltage levels of 20 actual products. Due to overstressing, 3-Zap CDM pass/fail results lowered from 50V to 300V compared to 1-Zap. Other technical data and consideration results are shown. 3-Zap CDM stressing is causing unnecessary burdens (delay and cost) in new IC qualification and automotive customer re-qualification of already non-automotive qualified ICs. It is past time to reconsider and harmonize 1-Zap for appropriate CDM conditions.

Nobuyuki Wakai graduated from Nagoya-univ. MC in 1993. He has been working for Toshiba Electronic Device and Storage Corp since 1993. His majors are semiconductor whole reliability items consisting of oxide film, MOSFET, metal, interconnects, package, products, soft-error, and ESD. Nobuyuki is also working in various standard organizations in JEITA (Japan Electronics and Information Technology Association) reliability committee (Vice-chair), JEDEC-JC14, IEC TC47/WG2 (Semiconductor devices reliability test - vice chair), WG5 (Wafer level reliability – chair) and ESDA to standardize various semiconductor reliability test method standards.
Reliability Challenges in Advanced Chiplets and 3D Technologies

Dimitri Linten, IMEC

Technology scaling driven by design-technology co-optimization (DTCO) and system technology co-optimization (STCO) has introduced a plethora of innovative concepts that extend beyond shrinking transistor dimensions and introducing new device architectures like gate-all-around (GAA), nanosheet, and complementary FET (CFET). These advancements encompass a variety of novel technologies, each with distinct features and benefits. Alternate channel materials like III-V semiconductors, 2D materials, and transition metal dichalcogenides offer enhanced electron mobility, paving the way for higher-performance devices. Back-side power delivery networks represent a significant shift in how power is supplied to transistors, potentially reducing power loss and improving overall efficiency. Novel interconnect schemes, including advanced metallization techniques and new materials, are being developed to address the growing demand for faster and more reliable data transmission within and between chips. Optical interconnects revolutionize communication speed and bandwidth between chips. Advanced 2.5D and 3D stacking technologies enable the integration of heterogeneous components into a single package, significantly enhancing performance and functionality while reducing the system’s footprint. These stacking techniques are especially crucial for applications where space and power efficiency are paramount, such as automotive and mobile devices.

Each technological innovation introduces unique reliability challenges that must be carefully addressed to ensure long-term performance and stability. Integrating advanced chiplets using 2.5D and 3D stacking technologies in automotive applications presents specific challenges due to the harsh operational environment. These environments demand robust solutions that can withstand high temperatures, mechanical vibrations, and wide operational ranges, all while maintaining stringent reliability standards.

This talk discusses reliability challenges associated with integrating advanced chiplets into 2.5D and 3D stacking scenarios to construct complete systems within large packages. We focus on several key aspects. Firstly, we discuss electrostatic discharge (ESD) challenges that become more pronounced with increased system
complexity and density. ESD protection is crucial in preventing sudden and catastrophic failures during manufacturing and operational phases. Next, we examine the electrical reliability challenges, including power delivery, signal integrity, and electromigration issues. Mechanical reliability is also a focus, covering topics such as thermomechanical stress and warpage. Ensuring mechanical stability is critical to prevent physical damage that could lead to device failure. Finally, we address thermal reliability challenges, particularly pertinent given the higher heat generation and potential hotspots in densely packed 3D stacked systems. Efficient thermal cooling strategies are essential to dissipate heat effectively and prevent thermal-induced failures.

**Dimitri Linten** received a PhD in electrical engineering from the Vrije Universiteit Brussel (VUB), Brussels, Belgium, in 2006. Since 2019, he has been the department director of the Advanced Reliability Robustness & Test department at imec. He is a senior member of the IEEE (SM13). His main research interests are ESD reliability, memory and logic device reliability physics, radiation, mechanical and thermal modeling and characterization, and Hardware security. He has served as a technical program committee member of several international scientific conferences, including the International Reliability Physics Symposium (IRPS), the EOS/ESD Symposium, the International ESD Workshop (IEW), and the International Electron Devices Meeting (IEDM).
This workshop discusses the suitabilities, capabilities, features, and limiting bottlenecks that future EDA tools can have or provide for use by ESD designers to solve their device/wafer-level, chip-level, or package/board/module-level ESD issues. Firstly, TCAD-based simulation tools are suitable for device-level predictions but generally too slow; nowadays, machine learning-based optimization algorithms are quite efficient; however, including TCAD simulation into the optimizing loop still costs too much in iteration time. Secondly, for chip-level circuit designers, SPICE-based simulation is still a golden sign-off tool; however, lacking accurate ESD models, especially including transient over-shoot behavior, is still a bottleneck; not just ESD diodes but also PClamps can present significant overshoots during fast-CMD events; what's more, there also lacking reasonable SOA models for victim Mosfets' turn-on characteristics. Thirdly, there still lacks tools for board or module level ESD simulations like CBM or ESD events, which may occur in special events like Hot-plug; no mention that advanced 2.5D/3D packaging technology is being developed so rapidly, targeting a CDM spec as low as ~10V, where still no EDA tools available for such scenarios.
Recently, as more and more foundries provide specialty technologies for wide applications, the associated ESD protection solutions from foundries would be interesting to design houses. Different from standard CMOS technology, the ESD solution in specialty technologies, such as BCD technology, would be more process-dependent and more complicated, making it difficult for the design house to develop the required ESD solution in a limited time without a foundry-developed solution. In this workshop, it would be valuable to discuss the necessary ESD solution in Foundry PDK to support the design house for the whole chip ESD network design, ESD/EMC co-design, system level ESD protection, etc. On the other hand, it's also interesting to understand the demand from design houses. So, what should be included in the so-called "ESD solution" from Foundry PDK? Will it be enough to include ESD Pcell, ESD ground rule, ESD high current data/model, etc.?
IEW Poster Sessions

Tuesday, July 16, 2024
16:30 - 17:30
IEW Room

Wednesday, July 17, 2024
15:20 - 17:00
IPFA Exhibition Hall

All IEW posters are presented in both sessions.
IEW Poster Teaser Sessions

Session A: ESD Protection Circuit, Device and Technology
Tuesday, July 16, 2024
14:40 – 15:25

A.1: Investigations of Transient-Induced Latchup in Planar and FinFET Technologies
Kateryna Serbulova, Shih-Hung Chen, Guido Groeseneken and Jo De Boeck, IMEC

Due to the aggressive scaling of the transistors, their architecture is constantly changed. To fulfill the requirement of better gate control, the technology is moving from planar to FinFET. This may induce reduced STI depth. This work verifies the technology's impact on transient-induced latchup immunity.

Ting Yang, Kyongjin Hwang, Jie (Jack) Zeng, and Tupei Chen, GlobalFoundries

This study uses the TLP technique to investigate the impact of geometric and process variations on the ESD performance of LVSCRs. The goal is to explore relationships between ESD parameters, design layouts, and process variations, enabling optimized device design, predictive models, and standardized guidelines for reliable LVSCR production.

A.3 Method to Lower CDM Discharge Current
Eugene Worley, Silicon Crossing

A methodology is presented that lowers the CDM discharge current by increasing the cross-domain voltage drop. A CDM voltage of 150V and device models are used to demonstrate the viability of this method. The intent is to reduce the pad diode sizes and, correspondingly, the pad capacitance for ultra-high speed I/O.
A.4 The Impact of the P-substrate Connection on the HBM Robustness of P-Type ESD Device

Jian-Hsing Lee, Vanguard

Although the p-substrate connection of the p-type ESD device does not impact the device It2, connecting the p-substrate to the ground significantly degrades the HBM robustness of the device. From the experiment result, adding NBL to a p-type ESD device can make its HBM robustness invariant to the p-substrate connection.

A.5 Withdrawn

A.6 Local ESD clamp with ultra-low parasitic capacitance for Chiplet interfaces

Ehsan Fallah, Sofics

Due to numerous connections, chiplet applications require a minimized ESD protection area, with stringent parasitic capacitance limits for high-speed interfaces. Despite diminished ESD robustness needs in packaged chiplet interfaces, on-chip ESD devices remain crucial for die assembly, ensuring compliance with assembly suppliers' minimum ESD requirements. The local clamp approach offers lower leakage and capacitance than conventional methods, promising flexibility for die-to-die applications.
Session B: ESD Modelling, Verification and Testing  
Tuesday, July 16, 2024  
15:25 – 16:10

B.1: A Module Level ESD Test System to Evaluate the System Level ESD Performance  
Oscar Tang, Kwanghui Koo, Ruoyu Hu and May Wu, Amazon

This presentation proposes a universal ESD test system for the module-level ESD test. This method could evaluate the ESD immunity level of the module under IEC 61000-4-2 stress and estimate the risk to meet the system level ESD requirement.

B.2 Digital Transformation of ESD Compliance Verification  
Dennis Corpuz and Alden C. Villarubin, Venture Corporation Limited

Electrostatic discharge control emerges as a crucial component within process control, playing a pivotal role in ensuring the quality of the end product. Embracing digital transformation offers a promising avenue to enhance ESD compliance management. Real-time monitoring, tracking, automatic maintenance reminders, and digital checklists eliminate the inefficiencies associated with manual recording processes.

B.3 A Verilog Model-Based ESD Simulation Method for Accurate Failure Predication of GPS LNA  
Ke Xu, Xiaofei Xie, Qiaoyong Fang, Jianan Liu and Jie Hu, Xiaomi

A Verilog model-based ESD simulation method is developed to predict the possibility of GPS LNA failure in advance accurately. Experiments of a GPS LNA circuit show that the simulation accuracy is above 75% and can also accurately predict the possibility of failure of semiconductor devices.
B.4 Parameter Extraction Methods and Circuit Simulation Models
Eugene Worley, Silicon Crossing

A methodology is presented to find the least squares fit of TLP data to circuit simulation models. Specifically, Excel's "solver" is used to obtain model fits to TLP and DC measurement data. Examples of model parameter extractions include diode overshoot, RC electro-thermal including metal interconnect, and snap-back NFET models.

B.5 Failure Analysis Techniques Locating Failure Sites CDM and ESD
Prathapan Balachandran, Thermo

Failure analysis techniques are crucial in identifying failure sites in Charged device model (CDM) and Electrostatic discharge (ESD) sensitive devices. This paper evaluates the effectiveness of various techniques in pinpointing failure locations, including scanning electron microscopy, voltage contrast imaging, and liquid crystal imaging. Understanding these techniques is essential for enhancing reliability in semiconductor devices.

B.6 Interpretation of Grounding Requirements Per ANSI/ESD S6.1 - China, Under the Scope
Tay CS, Canmax Group

In China, multiple standards exist for grounding systems for ESD control, leading to decades of confusion. This paper hopes to provide clarity to users in China by citing what appears to be the most appropriate standard and relating it to the requirements of ANSI/ESD S6.1.
# IEW Schedule

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