2nd Annual India ESD Forum
November 14 & 15, 2022

This is a one-of-a-kind forum in India bringing forth the realities of ESD requirements considering the rapidly advancing semiconductor technologies. This forum is designed to be a two-day online event to bring together key semiconductor companies and esteemed academic institutions in India to learn and exchange information about designing ESD/LU protections for various domains, CDM design validations, and understanding of EMC/EMI concerns. Renowned experts from various industry-leading organizations and academia will be presenting tutorials and invited talks.

The tutorials and invited talks will cover the following areas/topics:

1. LU design rules and verification
2. Challenges in high-speed (HSS) IP design and CDM levels
3. EMI/EMC challenges
4. ESD challenges in 2.5D/3D integration
5. CDM simulation and SOC validation

A new session of case study presentations is offered this year to facilitate submissions on real-life ESD/LU/EMI/EMC challenges/problems to foster more discussions and knowledgebase expansion. We encourage you to send your case study to info.eosesda@esda.org for an opportunity to discuss it with your peers from industry and academia. Download the submission template from https://www.esda.org/events/2nd-annual-india-esd-forum.

Mark Your Calendar!

Date	Start UTC +5.5	End UTC +5.5		Title	Speaker
Monday November 14	9:00 AM	10:15 AM	Tutorial 1	Electronic Design Automation (EDA) Solutions for Latch-up Verification	Michael Khazhinsky, Silicon Labs (USA)
	10:15 AM	10:30 AM	Break		
	10:30 AM	12:00 Noon	Tutorial 1		
	12:00 Noon	1:00 PM	Lunch		
	1:00 PM	2:15 PM	Tutorial 2	Challenges in High-speed (HSS) IP Design and CDM Levels	Harald Gossner, Intel (Germany)
	2:15 PM	2:30 PM	Break		
	2:30 PM	3:45 PM	Tutorial 2		
	3:45 PM	4:15 PM	Break		
	4:15 PM	5:15 PM	Invited Talk 1	ESD Challenges in 2.5D/3D Integration	Mirko Scholz, Infineon Technology AG; Marko Simicic, imec (Belgium)
Tuesday November 15	9:00 AM	10:15 AM	Tutorial 3	EMI-Immune Integrated Analog and Mixed-Signal Circuits - Design and Measurement Examples	Prof Mary AM S Baghini, Indian Institute of Technology, Bombay (India)
	10:15 AM	10:30 AM	Break		
	10:30 AM	12:00 Noon	Tutorial 3		
	12:00 Noon	1:00 PM	Lunch		
	1:00 PM	2:00 PM	Invited Talk 2	Predictive CDM Simulation and Validation Strategy for SOC During Design Phase	Paul Zhou, Analog Devices (US)
	2:00 PM	2:15 PM	Break		
	2:15 PM	3:45 PM	Case Study	Case Study Presentations	Have a case study you want to share? Download the submission template from https://www.esda.org/events/2nd-annual-india-esd-forum and email it to info.eosesda@esda.org.
	3:45 PM	4:15 PM	Break		
	4:15 PM	4:45 PM	Invited Talk 3	Industry Council on ESD Target Levels: Setting New Standards for ESD Qualification	Charvaka Duvvury, ESD Consulting, LLC; Harald Gossner, Intel