2021

International Electrostatic Discharge Workshop

May 17-20, 2021

Special Virtual Event

IEW

Setting the Global Standards for Static Control!

EOS/ESD Association, Inc. 7900 Turin Rd., Bldg. 3 Rome, NY 13440-2069, USA
PH +1-315-339-6937 • Email: info@esda.org • www.esda.org

ESD ASSOCIATION

IEW 2018 Turnout Belgium

Management Committee

Management Committee Chair
Steffen Holland, Nexperia
Technical Program Chair
Heinrich Wolf, Fraunhofer EMFT
Keynote Chair
Theo Smedes, NXP Semiconductors
Invited Speaker and Seminar Chair:
Shih-Hung Chen, imec
Discussion Group and Special Interest Group Chair
Fabrice Caignet, LAAS/CNRS
Audio/Visual Chairs
Vasantha Kumar, Nexperia
Paul Phillips, Phasix
Industry Council Advisor
Harald Gossner, Intel Deutschland GmbH
EOS/ESD Association, Inc. Operations Chair
Christina Earl
EOS/ESD Association, Inc. Director of Events
Nathaniel Peachey, Qorvo

Technical Program Committee

Dietmar Walther, Texas Instruments Deutschland GmbH
Kai Esmark, Infineon Technologies AG
Nathan Jack, Intel
Christian Stockreiter, ams AG
Evan Grund, Grund Technical Solutions
Dolphin Abessolo Bidzo, NXP Semiconductors
Rita Fung, Cisco
Andrea Boroni, STMicroelectronics

Experience IEW

Greetings from the 14th annual International ESD Workshop (IEW) Management Team! This event presents a unique opportunity for attendees to participate in in-depth discussions and learning on EOS and ESD topics in a highly interactive virtual environment. This virtual event will be held via Microsoft Teams and Spatial Chat

Focused discussion groups, held in the afternoons, are a unique part of our interactive workshop. While each EOS/ESD topic discussion is facilitated by an expert on the subject, the main discussion will take place among the participants. The discussion groups will address topics of the focus issues and include ESD soft failures, challenges for advanced CMOS ESD protection, System level test for IOT and wearable devices, latch-up, on-chip health monitoring strategies and the effects if CDM limits are lowered to 150 volts.

Scheduled poster sessions are the core of the technical program. These poster sessions begin with a brief introduction of each contribution by the authors to the workshop participants. These teasers encourage the participants to visit each poster and its author in the subsequent interactive poster discussion session. To compliment the offering, attendees are also encouraged to bring open posters. This format provides an ideal forum for learning and the interchange of new ideas. Topics covered in the poster sessions include CDM effects and failures, Test cases, ESD verification with EDA tools, ESD devices for advanced CMOS technology, models for SEED simulations, on-chip ESD protection devices, latch-up and interconnect investigations.

Stimulating state-of-the-art EOS/ESD seminars, as well as invited talks are scheduled. Come and listen to presentations, and later meet with the presenters, discussing ESD protection for brain implantable electronics, FD-SOI technology, fast transients of CDM, side channel attacks on chips with security functions, ESD qualification methods of automotive manufacturers, EMC design and soft failures, electrical overstress and new IEC testing results.

Come and meet experts, share your views, ask questions, and extend your network with EOS/ESD experts from industry and academia. Above all, learn how to efficiently deal with today's EOS/ESD challenges and prepare for tomorrow in an informal and interactive atmosphere. Register for this event early. This will help us in the final planning and preparation for an extraordinarily successful event. We sincerely hope that you will join us virtually for the 2021 IEW.

For poster sessions, workshops, and networking, virtual attendees can use Spatial Chat. Spatial Chat is a video chat conversation platform that recreates real-life social interactions. Please visit https://spatial.chat/ to get familiar with the program. Access to the IEW spatial chat will be sent to attendees before the event.

Tutorial Monday 13:00 - 15:00

Advanced TLP Applications
Instructor: Heinrich Wolf, Fraunhofer EMFT

The tutorial covers accuracy aspects of transmission line testing and explains how to do characterization and parameter extraction for compact modelling including switching behavior and electro-thermal aspects. Furthermore, it discusses SOA measurements and the application of CC-TLP as a CDM like stress method.

Heinrich Wolf received his diploma degree in electrical engineering from the Technical University of Munich (TUM) and his PhD from the Technical University of Berlin, Germany. He joined the chair of integrated circuits at TUM as a member of the scientific staff working on electrostatic discharge related issues. This involved modeling of ESD-protection elements, parameter extraction techniques, and test chip design. In 1999, he joined the Munich branch of the Fraunhofer Institute for Reliability and Microintegration (IZM) which became the Fraunhofer Institution for Microsystems and Solid State Technologies EMFT in 2010. He was involved in the investigation of ESD protections for CMOS and smart power technologies. Furthermore, he worked on the simulation and development of ESD protections and on the development of ESD test methods and tester characterization. He is also coordinating the ESD related activities at the EMFT including the development of ESD test systems and the design of protection structures for deep submicron technologies. Furthermore, he works in the field of RF simulation and characterization in the frequency range up to 110 GHz. Currently he also represents the german ESD-Forum in the standards working groups.

Monday Entertainment 16:45 - 17:45

Chocolate Tasting “from 0 to 100 in 10 Chocolates"
This relaxing evening event is a culinary chocolate trip with Oliver Rohl from Schokovida in Hamburg. Attendees will enjoy a presentation about the whole world of chocolate while sampling everything from white to whole milk, plain and dark chocolate, truffle, and bar chocolate as well as cocoa beans. Everything is made by hand with high-end ingredients and a love of the trade.
Attendees who register early will have chocolate mailed to them to enjoy during this presentation. Attendees registering late will receive choclate after the event.

Keynote

ESD Protection for Medical Implants

Wolfgang Krautschneider, Hamburg University of Technology

Scaling-down of CMOS circuits is accompanied by a huge performance increase of integrated circuits that opens up much potential of electronics for medical implants. There are already some electronic implants in use, e.g., pace makers, cochlear implants and implants for deep brain stimulation. Implants for other medical applications are in an early state or under development.

Biological signal sources show in most cases a very high impedance and provide signals with a very low amplitude. This requires amplifiers with very high input impedance provided by MOS transistors. For handling the electronic circuits during assembly, all the pads connected to gates of MOS transistors have to be protected by ESD devices that may degrade the input resistance resulting in worse signal to noise ratios. An appropriate trade-off has to be found that will be illustrated by demonstrators for medical implants.

Another challenge for medical implants are the very high magnetic fields of MRI which may generate high voltages that have to be handled by protection structures.

One out of four persons in western countries gets the diagnosis cancer with metastases. They are treated by systemic therapy (chemotherapy etc.) combined with radiotherapy applying comparably high radiation doses. When these patients carry medical implants, the radiation can degrade the characteristics of ESD protection devices, so that design measures have to be taken to adjust their radiation robustness accordingly.

Wolfgang H. Krautschneider (M'85) received the M.Sc., Ph.D., and Habilitation degrees from the Berlin University of Technology, Berlin, Germany.,He was with Central Research Laboratories, IBM, Yorktown Heights, NY, USA, the Siemens Research Center, Munich, Germany, and the DRAM Project of IBM and Siemens, Essex Junction, VT, USA. He is currently the Head of the Institute of Nanoelectronics at the Hamburg University of Technology, Hamburg, Germany.

Invited Talks

Invited Speaker Chair:
Shih-Hung Chen, imec

Invited talks always give good opportunities to broaden workshop attendees' exposure to expertise in different focused areas of interests. This year, three invited talks are included with wide-range aspects from process technology, chip security, to system qualification. The talk from Dr. Philippe Galy, STMicroelectronics, is one of the focus topics of this year. It is dedicated to ESD/LU challenges for ultra-thin body and box (UTBB) fully depleted SOI (FD SOI) CMOS technology for 2D and 3D innovative solutions. Dr. Galy will give an introduction of this UTBB FD SOI technology and will also discuss innovative ESD solutions. The talk from Alexander Schlösser, NXP, will focus on side channel attacks for high security automotive chips. In this talk, Alexander will look at how hardware security analysis uses soft failures and will explore the differences and similarities to ESD-related failures. The talk from Dimitri Linten, imec, will focus on the scaling technology with system technology co-optimization (STCO) approach toward node N5 and beyond. Dr. Linten will give an introduction of the novel STCO approach and will discuss the ESD reliability challenges in this technology.

Invited Talk 1

UTBB FD-SOI and ESD/Latch-up: Challenges and Solutions

Philippe Galy, STMicroelectronics

This talk is dedicated to ESD/LU challenges for Fully Depleted SOI (FD-SOI) Ultra Thin Body and Box (UTBB) CMOS technology nodes for 2D and 3D innovative solutions. After an introduction on the UTBB FD_SOI technology provided by STmicrolectronics, especially in 28nm High k metal gate, the ESD protection challenges in this technology will be discussed along with solutions. Preliminary silicon results with 2D/3D innovative solutions are introduced according to performance and integration. Moreover, radiation effects are also addressed.

Philippe Galy born 1965, received the Ph.D. from University of Bordeaux and H.D.R from LAAS CNRS University of Toulouse. He is a fellow, technical director at STmicrolectronics Research and Development France. He has proposed a full CDM protection and several new ESD compact devices for mature & advanced CMOS technologies. He supports several teams for research focused on new innovative solutions: Memory + silicon Qubit and cryo-design, Neuromorphic, 3D ultimate integration. He has authored or coauthored several publications (+100), books (3), and patents (+100). He serves in TPC and is a reviewer for many symposiums and journals. He is also involved in National (3) and European projects (4). Also he joins the QuEng CDP team from Grenoble and also adjunct professor at " Université de Sherbrooke (UdS)".

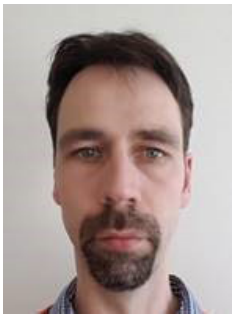
Invited Talk 2

Reliability Challenges in Scaling Era with System Technology Co-Optimization (STCO) Approach

Dimitri Linten, imec

From the 10 nm technology generation onward, traditional scaling has been complemented by design-technology co-optimization (DTCO), combining expertise from technology as well as from design. But, as the technology moving forward, the benefits of DTCO in system-on-chip (SoC) applications are expected a certain saturation. For 3 nm and beyond technology nodes, the focus will shift from scaling at logic cell level towards scaling at system level. Hence, DTCO is evolving into an system technology co-optimization (STCO)-oriented approach. More and more (sub-)system functions will be integrated in one chip with a special 3D vertically stacked or 2.5D interposer architecture. However, a chip-level or even a system-level electrical reliability becomes necessary to evaluate at the early stage of the technology/circuit/system development period.

In this talk, we will look at the technology features of the STCO approach, including different 3D integration technologies applied in different levels of interconnect hierarchy. In addition, the emerging reliability challenges will be also discussed from different aspects in the STCO framework. .



Dimitri Linten received PhD degrees in electrical engineering from the Vrije Universiteit Brussel (VUB), Brussels, Belgium in 2006. Since 2015, he is the R&D manager of the Device Reliability and Electrical characterization group at imec. He is a senior member of the IEEE (SM13). His main research interests are ESD reliability, Memory and logic device reliability physics, radiation, biosensors and security. He has served as a technical program committee member of several international scientific conferences, among which the International Reliability Physics Symposium (IRPS), the EOS/ESD Symposium, the International ESD Workshop (IEW) and International Electron Devices Meeting (IEDM).

Invited Talk 3

EM induced fault attacks and their security exploitation

Ingrid Verbauwhede, KU Leuven

ICs are continuously exposed to a wide spectrum of electromagnetic radiation. The power levels of these fields are usually relatively low and will therefore not affect the device or can be mitigated. In hardware security, however, we have to consider the case where an adversary will expose the device with intentional and directed electromagnetic radiation causing the device to malfunction in a controlled manner. The adversary will tune the setup such that common overcurrent or overvoltage protection mechanisms are not triggered. At the same time, the adversary can still change the state of the device without permanently damaging it. Such attacks, where an adversary actively manipulates the device to extract secret data from it, are commonly referred to as fault attacks. In this talk, we will discuss the impact electromagnetic field fault injection has on common microcontrollers. A successful fault attack is built up out of two parts. First, an adversary has to cause the device to malfunction; then, the malfunction can be exploited. In this talk, we will discuss how one can successfully create faults and how these can be exploited from a cryptographic point of view.

Ingrid Verbauwhede's main expertise includes system and architecture design, embedded system, ASIC and FPGA design, design methodologies for real-time, low power embedded systems, and embedded security systems. She has experience in interdisciplinary research linking design for security with novel technologies and circuits and investigating the requirements of novel cryptographic algorithms and software security requirements on secure hardware and HW/SW co-design. Her ability to cross the gap between algorithm and protocol development and actual implementation in hardware, software, and embedded systems has been widely recognized. Ingrid Verbauwhede has experience in running small and large research projects, fundamental ones (sponsored by NSF or FWO), basic research (funded by EU), and applied (in collaboration with industrial partners). Ingrid Verbauwhede is an IEEE fellow and a member of the Royal Academy of Belgium for Sciences and Arts. In 2016 she received an advanced ERC grant and, in 2017, an IEEE Computer Society Technical Achievement Award for pioneering contributions to design methodologies for tamper-resistant and secure electronic systems.

Seminars

Seminar Chair:
Shih-Hung Chen, imec

Four recognized experts from university, research institute, and industry will give seminar talks on some of the highly interesting topics at this year's IEW. These seminar talks are covered with the main ESD challenges in system-level, component-level, and even manufacturing perspectives. The seminar from Dr. Wolfgang Stadler, Intel, will focus on non-standard overstress in manufacturing phase and will show the (mis)correlation between IC ESD qualification waveforms and real world risks in handling ICs, boards, and systems. The seminar from Professor David Pommerenke, ESDEMC, will focus on system-level ESD testing and will discuss the reasons for large uncertainty of the test results even when carefully following the procedures in IEC 61000-4-2, as well as give suggestions to the test implementation. The seminar from Professor Franco Fiori, Politecnico di Torino, will focus on circuit-level EMC/EMI design and will discuss recent progresses on the EMI immune designs of MEMS readout circuits. Finally, the seminar from Johannes Weber, Fraunhofer EMFT, will focus on fast transient of CDM ESD event and will cover wide-range perspectives of the fast rise time (or fast slew rate) from the fundamental theory to the testing methodologies.

Seminar 1

Achieving Meaningful and Repeatable Results in ESD System Level Testing

David Pommerenke, Technical University of Graz.

The vast majority of system level ESD testing follows the specifications defined in IEC 61000-4-2. Unfortunately, even when carefully following the procedures in IEC 61000-4-2 there is a high level of uncertainty in the test results, and successful passing of the test requirements is often not a good prediction of ESD robustness in the field. The talk, which is based on a white paper by the Industry Council on ESD Target Levels explains deficiencies of the standard and problems within the generally applied test procedures. Based on this analysis the talk suggests improvements to both the standard, and the test implementation.
This includes
- better ESD gun specifications
- Full wave and SPICE models for ESD generators
- Simulation of ESD robustness following the SEED concept (System Efficient ESD Design)
- Improved documentation, such as measuring the ESD current during testing
- Improved test produced e.g., number of discharges, methods of stabilizing the arc in air discharge etc.
- Robotic ESD testing

The goal of the talk is to explain the reasons for the large test result uncertainty, to give suggestions to the standard committee for improvements and to enable engineers to implement the test in such a way that results are meaningful, repeat well and give indications for the root cause of a failure.

Dr. David Pommerenke received his diploma and PhD from the Technical University Berlin, Germany. His research interests are system level ESD, electronics, numerical simulations, EMC measurement methods and instrumentation. He worked at Hewlett Packard for 5 years before joining the electromagnetic compatibility laboratory at the Missouri University of S&T in 2001. Dr. Pommerenke became the CTO of ESDEMC in July 2019 before joining the ESD/EMC group at the Technical University of Graz in Austria in January 2020. His new focus is on ESD, EMC, harmonics, and PIM. He has published more than 200 papers and is inventor on 13 patents. His main research interests are measurement/instrumentation ESD, electronic design and EMC. He is IEEE fellow and associated editor for the IEEE Transactions on EMC.

Seminar 2

Correlation of Qualification ESD Robustness and Handling Threats

Wolfgang Stadler, Intel Deutschland GmbH

Today, almost all integrated circuits (ICs) are qualified with respect to Human Body Model (HBM) and Charged Device Model (CDM). Current international standards on ESD Control Programs require a minimum ESD robustness of 100 V according to HBM and 200 V of CDM for ICs to ensure safe handling. However, there is no clear correlation between qualification waveforms and waveforms of reel ESD events even on IC level, therefore, the qualification might not necessarily cover all problems.
The situation is even worse if ESD events on system level are considered. Such events mainly occur during board and system assembly or during testing, like Charged Board Events, Cable Discharge Events, or transient latch-up. Today, there are no widely accepted ESD qualification standards on most of these ESD system level events, this is one reason why the ESD control standards refer to IC level robustness only.
In this presentation, we will assess the (mis)correlation between IC ESD qualification waveforms and real world risks in handling ICs, boards, and systems. We will also discuss which ESD system level characterization methods could help to improve the ESD process assessment methodologies of boards or system handling processes.

Wolfgang Stadler received his diploma degree in physics in 1991 and in 1995 the PhD degree from the Physics Department of the Technical University Munich. 1995 he joined the semiconductor division of Siemens, which became Infineon Technologies in 1999. His focus was on development of ESD-protection concepts in CMOS technologies and on innovative ESD topics. In this role he was coordinator of several European and German ESD funding projects. Since 2003, he was also been responsible for the measurement characterization of I/O cells and PHYs. In 2011, he joined Intel Mobile Communications which is now Intel Deutschland GmbH. Within the corporate quality network, he is currently responsible for the ESD control program of Intel and for ESD risk assessment. Furthermore, he supports ESD/latch-up testing and qualification of products. Wolfgang holds several patents in ESD-related topics. He is author or co-author of more than 120 technical papers and has co-authored a book on ESD simulation. He has received several best paper awards and teaches courses on ESD device testing, ESD qualification, and ESD control measures (for example, TR53 ESD Technician Certification).

Seminar 3

EMC of Integrated Circuits, An Introduction to Test Methods

Mario Rotigni, STMicroelectronics

An integrated circuit is often at the source of EMC issues in modern electronics, taking the role of victim or generator of interferences. The explosion of applications in Automotive brings the subject under the spotlight even more than in the past. It is a consolidated procedure submitted to test the final product, the car, or the electronic control modules and the integrated circuits at their heart. The earlier a potential, not conformity, is detected, the cheaper its fix is. The industrial practice makes good usage of test and measurement procedures developed in the middle of the '90, specifically for the integrated circuits and an eye to reducing the cost and complexity of the required equipment. This presentation introduces such methods focusing on microcontrollers and systems on a chip, pervasively used to control traditional and new functions in today's and tomorrow's cars. The test of radiated and conducted emission will be presented and immunity (susceptibility), with some discussion of possible links with the ESD world.

Mario Rotigni was born in Bergamo, Italy, in 1958 and received a diploma in Electrical Engineering in 1977. He was with the R&D Department of Magrini Galileo for 12 years, working on the design of process instrumentation and test systems for high-voltage circuit breakers and their auxiliary equipment. The equipment operated in very hostile electromagnetic environments and EMC as part of dedicated design and test attentions. In 1990 he joined Audiotel to develop an Automatic Test Equipment dedicated to testing production microcontrollers and other integrated circuits. Since 1993 he is with STMicroelectronics, holding various engineering, design, and R&D positions in the Automotive Product Group. He is currently in charge of EMC of microcontroller and system on chip for all automotive applications. He has co-authored 21 papers about EMC

Seminar 4

Stress Current Rise Time Evaluation in the Single-Digit Picosecond-Domain

Johannes Weber, Fraunhofer EMFT

This seminar will cover theory including the definition of rise time/slew rate, relation to bandwidth oft the test system, and voltage overshoot of typical ESD protection schemes; as well as dependency of ESD robustness (peak current failure thresholds) on rise time (slew rate). Examples of discharges with ultra-fast rise times in the manufacturing line will be given. The seminar will also include discussion on current rise time evaluation of CDM testing and alternative contact-based test method CC-TLP as a method to repeatably control rise time of stress pulses. During the seminar, the speaker will challenge the limits of today's test methods and methodologies in the single-digit picosecond domain and discuss critical parameters that may influence the slew rate (rise time) sensitivity of high-speed devices (high-speed design, DC-blocking capacitor etc.).

Johannes Weber received his Master's degree in physics from the Technical University Munich (TUM) in 2015. He wrote his Master's thesis in the research area of Nuclear, Particle and Astrophysics at the Max Planck Institute for Extraterrestrial Physics (MPE). Afterward, he joined the Team of Analysis & Test at the Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT in Munich, Germany as a research associate. He works in the field of Electrostatic Discharges (ESD) and focuses on the development of ESD test methods and ultra-fast ESD events in the picosecond domain. His research mainly deals with the influences of critical stress parameters like the rise time or the energy content of the stress pulse on the failure level of advanced semiconductor technologies. Supported by the ERC Grant 2016 of the ESD-Association, he finished his PhD thesis with the title "Pulsed High Current Characterization of Highly Integrated Circuits and Systems" at the Bundes-wehr University of Munich in 2019.

Discussion Groups

Discussion Groups Chair:
Fabrice Caignet, LAAS/CNRS

The discussion groups are an integral part of the workshop. There will be six discussion groups offered, with three parallel sessions on Tuesday evening and three parallel sessions on Wednesday evening. The topics include ESD soft failures; ESD challenges for advanced CMOS (FD-SOI, beyond FINFETS); discussions on health monitoring, the appropriateness of system level testing for IoT devices/wearables; latch-up; and testing devices for CDM below 150 volts. Each discussion group has a moderator with extensive expertise on the topic to help guide and inspire the discussion. The success of these sessions depends on your active participation. We encourage you to bring along data, ideas, and other items of interest to share.

Session A
Parallel Groups–Tuesday 16:30–18:00

DG A.1
ESD Challenges for Advanced CMOS (FD-SOI, Beyond FINFETS)
Co-Moderators: Shih Hung Chen, imec; Philippe Galy, STMicroelectronics

While Bulk FinFET and Fully-Depleted (FD) SOI technologies have become the mainstream in the advanced CMOS IC industry, what are the next technology options or next device architectures after FinFET and FD SOI? Several promising candidates have been proposed; however, only very few prior works discussed ESD reliability in these promising future technologies. In addition, the challenges might not only from technology options but also from more realistic aspects, such as design verification and product qualification. This discussion group aims to look at the ESD challenges in advanced CMOS technologies with varied perspectives. With your ideas and sharing experience, this discussion group will be able to bring some clarity to those emerging ESD challenges.

DG A.2
System Level Test: is it Appropriate for IOT Devices/Wearables?
Co-Moderators: Adrijan Barić, University of Zagreb Faculty of Electrical Engineering and Computing; Harald Gossner, Intel Deutschland GmbH

System level testing using IEC 61000-4-2 is like an elephant in a glass shop; it seems to be widely applicable and it produces sound results. However, the question is, is it really useful and relevant for real world events or is there any better approach? Also, what are the most appropriate test levels for tiny IoT devices. Are the size of the IoT device and the technology node critical for the energy that can be dissipated on the device? What are the ultimate sustainable testing levels for the down scaled technology nodes that will inevitably penetrate into the IoT market? Finally, when we do system level testing, do we look only for the functionality of the device or we also have to worry about safety of the system. Is it possible to disturb the operation in such a way that the data sent from IoT device can generate a twisted image of the reality?

DG A.3

Is Latch-up Testing Still Relevant?

Moderator: Guido Quax, NXP Semiconductors

The category of low voltage IC products has experienced an ever decreasing operating voltage, such that a setup according to the latchup standard (JEDEC78E) does not lead to any current injection stress. On the other hand, the number of products with a severe system level stress requirement (like IEC61000-4-2 or IEC61000-4-5) is increasing. The risk for 'soft failures' (latchup) would, in this case, not be covered by passing the JEDEC78E test.

This leads to a question: does the standard need to get better 'aligned' with the modern product portfolio? And if so, how should that be done? One can think of product categories, each with their own stress. How should the reference stress for a product category be determined? Next to these possible improvements to the standard, we would like to reflect with you on the cause of current injection stresses in 'the real world'. In which situations do you think the +/- 100 mA stress could still occur, and are there actual field returns related to situations beyond this current stress level? How can the standard capture these situations? With this discussion we aim to get a better insight in the limitations of the current JEDEC78E standard.

Session B
Parallel Groups- Wednesday 16:30-18:00

DG B.1
ESD Induced Soft Failures
Moderator: David Pommerenke, Technical University of Graz

This discussion group will try to answer the root cause of soft-failures, methods for modeling, and countermeasures. The root-cause includes, the discharge, the system level coupling path, and the internal reasons of the IC which lead to a soft-failure. Modeling of soft-failures can be successful using circuit information if the region inside the IC is well defined. However, in most cases behavioral models will be needed. Here behavioral models for USB 3.x will be presented and compared to measurements. A variety of countermeasures exist, obviously in software, but it is also possible to use TVS diodes such that they not only prevent damage, but reduce soft failures strongly. This will be explained based on a USB 3.x example to start an open discussion on all aspects of soft failures.

DG B.2
Health Monitoring: Can we use Transient Event Detection of EOS/ESD to Build More Resilient Systems?
Moderatos: Franz Dietz, Henning Lohmeyer, Robert Bosch GmbH; Patrice Besse, NXP Semiconductors

Over the last years there has been significant attention within reliability engineering to the so called third generation of reliability. Such resilient systems are designed to be aware of their health status by recognition of critical stress-strength combinations. This enables the system to react to changed situations or even to compensate errors prior to failure. On a hardware level it is proposed to introduce detectors for aging, mission profile logging and impeding failure of SoC. Additionally, detectors for events exceeding normal operation region were proposed which arguable could include EOS/ESD. Specifically for ESD threads, transient event detectors have been discussed that monitor exposure of the systems to ESD-stress during assembly and field usage. Furthermore such detectors have been proposed to support analysis of ESD soft failures and enable containment of such events on system-level. By sorting through the different approaches and targets of implementing transient event detectors, the discussion group aims to identify the potential benefits and limits of such an approach in the context of resilient systems for different applications. What can we learn from detecting and even measuring strength of ESD/EOS events in assembly and field and how do we use such information for more resilient and safe systems?

DG B.3
Testing Devices for CDM Below 150 Volts
Moderator: Marko Simicic, imec

The CDM device testing levels are dropping below 150 volts. One of the reasons for that is the technology advancement. However, the zap-to-zap variability of the standard Field-Induced CDM (FI-CDM) tester used today drops significantly for low voltages. Alternative CDM testers such as the capacitively-coupled TLP or the low-impedance contact CDM (LICCDM) do not have issues with variability. However, their relay-based testing mechanism is significantly different to the current standard. In this discussion group, we will discuss questions as:

What are the reasons for lowering the CDM testing level?

Is the pulse rise time an issue for LICCDM/CC-TLP?

What are the concerns with testing CDM on non-packaged dies and wafers?

Should we be reporting the CDM currents instead of the voltages?

Technical Sessions

Technical Session Chair: Heinrich Wolf, Fraunhofer EFMT

This year's IEW technical program consists of three sessions, where peer-reviewed poster presentations are discussed together with the authors and interested colleagues. The authors will introduce their work in a short podium "teaser" presentation before the extended interactive discussion with the workshop participants at the poster sessions. This format allows an in-depth exchange of ideas among a diverse audience in a very informal setting. A wide variety of ESD subjects will be covered, including ESD simulation/verification of full chips and single elements, system related and general measurements aspects and device physics covering the behavior of single elements, and also latch-up.

Technical Session A: Simulation Related Topics

A.1 - WITHDRAWN

A.2 Full-Chip CDM Analysis: Is Static Simulation Enough?

Jordan Davis, Chanhee Jeon, Sung-Jun Song, Samsung Electronics; Yuri Feinburg, Simon Young, Silicon Frontline

To improve understanding and verification of ICs before manufacturing, a static approach to CDM verification and analysis is explored. In the absence of full-chip transient circuit simulation, considered computationally prohibitive, enhancements to the static approach have been made. These enhancements are able to find potential failures regardless of technology or design.

A.3 X-FAB ESD Design Checker an Automated Tool for Full Chip ESD Simulation

Vadim Kuznetsov, X-FAB Dresden GmbH & Co. KG; Lars Bergmann, X-FAB Global Services GmbH

X-FAB ESD Design Checker (XESDC) is the tool for full chip ESD analysis. It performs a virtual TLP test and finds ESD weaknesses of IC design using the CDL or SPICE extracted netlist and technology-specific ESD model library. XESDC works independently from EDA platforms using the built-in simulation core.

A.4 Chip-Level ESD Verification Using Graph-Theory Based Approach

Vlatko Galić, Adrijan Barić, University of Zagreb; Aarnout Wieers, Renaud Gillon, ON Semiconductor

A new Electrostatic Discharge (ESD) verification flow is proposed. The presented methodology uses piecewise linear models based on transmission line pulsing (TLP) measurements to ascertain the level of ESD robustness of integrated circuits (IC) and to detect ESD current paths. This flow is based on graph-theory Floyd-Warshall algorithm.

A.5 Calibration and Modeling of LICCDM Setups

Marko Simicic, Shih-Hung Chen, imec; Wei-Min Wu, imec, KU Leuven, NCTU; Shinichi Tamura, Yohei Shimada, Masanori Sawada, HANWA Electronic Ind. Co., Ltd.

This poster attempts to measure the frequency and time domain characteristics of the LICCDM probe. This will enable calibration and de-embedding of the system parasitic impedances. Also, it will enable us to build a precise model of the probe. The objective of this poster is to understand the LICCDM tester in depth and identify the potential pitfalls.

Technical Sessions continued

Technical Session B: System-Level and General Testing Aspects

B.1 Using Fast Transient Characterization (FTC) for EOS Risk Mitigation

Dietmar Walther, Raj Sankaralingam, Texas Instruments

The introduced method applies fast transient pulses (residual IEC 61000-4-2 pulses) with high energy to a powered device. Besides soft failures also electrical induced physical damages (EIPD) are observed which were undetected during HBM/CDM. Once fails are identified, simulation is used identifying circuit weaknesses to comprehend powered ESD fail modes.

B.2 De-Embedding of VF-TLP/CC-TLP Systems

Johannes Weber, Ellen Jirutková, Heinrich Wolf, Horst Gieser, Fraunhofer EMFT

This poster presents a De-/Embedding technique for TDR-based test methods like VF-TLP or CC-TLP. It replaces the manual determination of the time shift parameter between the incident and reflected pulse by fully reconstructing the signals at the DUT considering dispersion effects. Instead of S-parameters of the test fixture which should be de-embedded, its calibration requires only three pulses in time domain.

B.3 - WITHDRAWN

B.4 Combining TLP and VF-TLP Methods: VF-TLP Resolution with Longer Pulses

Dennis Helmut, Munich University of Technology, University of the Federal Armed Forces Munich; Gerhard Wachutka, Munich University of Technology; Gerhard Groos, University of the Federal Armed Forces Munich

Using a TLP setup with two distinct voltage sensors separated by a delay line, the new methodology extracts the DUT current and voltage waveforms from the overlapping sensor signals. This results in a clearly better rise-time resolution than standard TLP without the restrictions for pulse lengths that apply in vfTLP

B.5 - WITHDRAWN

Technical Sessions continued

Technical Session C: Device Physics and Testing

C.1 An ESD Protection Device with Floating P+ Diffusion for Tunable ESD Design Window and High Latch-up Immunity

Prantik Mahajan, Satya Suresh, Xiao Mei Elaine Low, Kyongjin Hwang, Robert Gauthier, GLOBALFOUNDRIES

Effective Supply Pin ESD protection with power clamp design incorporating Drain side Floating P+ Diffusion is presented. Conventional MV GGNMOS is typically limited in voltage applications. Tunability of the trigger and holding voltages is key to developing ESD protection power clamps with high Latch-up immunity covering a wide voltage spectrum.

C.2 Study of vfTLP Characteristics of ggNMOS in Advanced Bulk FinFET Techonology

Wen-Chieh Chen, Guido Groeseneken, KU Leuven, imec; Shih-Hung Chen, Dimitri Linten, imec

To investigate the impact of faster transient on the bulk FF GGNMOS, the vfTLP test results are shown in this work. The gate length dependence is demonstrated by vfTLP measurements and 3D TCAD simulations. Furthermore, the comparison of vfTLP and TLP results are presented.

C.3 Impact of Extreme Wafer Thinning on Latch-up (LU) Risk in Advanced CMOS Technologies

Kateryna Serbulova, Guido Groeseneken, KU Leuven, imec; Shih-Hung Chen, Dimitri Linten, imec

Latchup (LU) risk in advanced technologies cannot be eliminated and even becomes one of the major reliability concerns, especially for stacking architectures with extremely thinned Si substrate. LU originates from parasitic BJTs forming SCR path. In this work the current gain is evaluated for two parameter variations in TCAD simulations.

C.4 Influencing SCR Holding Current by Segmentation Topology

Vasantha Kumar, Steffen Holland, Hans-Martin Ritter, Nexperia; Hasan Karaca, Dionyz Pogany, TU Wien

A segmented layout topology on a novel SCR is used to obtain a higher holding current (Ihold). The SCR Ihold has been increased by reducing the emitter area of the PNP, which reduces the injection efficiency of the PNP. The increased ability to collect free carries results in higher Ihold.

C.5 Efficient 3.3V Power Clamp Circuit Using Low-Voltage 1.2V Transistors in CMOS Process

Ranabir Dey, Vijaya Kumar Vinukonda, Fabrice Blanc, Arm

Some 5nm technology goes with 1.2V thick-oxide devices. So triple-stack ESD clamps are needed to support 3.3V operation. As traditional stacked-clamp ESD efficiency is not optimum, a new 3.3V stacked-clamp with multi-gates RC trigger circuit is proposed. Better ESD clamping voltage efficiency is shown while keeping almost the same area footprint.

C.6 Co-Optimization on RF/High-Speed I/O Pad: Efficient ESD Solution for 5G Heterogeneous Stacking Interface in Advanced CMOS Technology

Wei-Min Wu, KU Leuven, NCTU, imec; Shih-Hung Chen, Marko Simicic, Dimitri Linten, imec; Ming-Dou Ker, NCTU; Guido Groeseneken, KU Leuven, imec

In the 5G broadband ESD design, moving first-stage ESD devices under I/O pads resulted in better ESD performance. However, extra parasitic capacitance was increased to RF bandwidth degradation. Therefore, ESD diodes layout optimization was proposed to enable capacitance and HBM improvement. CDM evaluation is also discussed for wafer-to-wafer integration issue

C.7 Triggering of Multi-Finger and Multi-Segment SCRs Near the Holding Voltage Studied by Emission Microscopy Under DC Conditions

Hasan Karaca, Rudolf Krainer, Dionyz Pogany, TU Wien; Clement Fleury, Silicon Austria Labs; Steffen Holland, Hans-Martin Ritter, Vasantha Kumar, Guido Notermans, Nexperia

Emission microscopy under DC current controlled mode has been used to study current flow distribution in multi-finger and multi-segment SCRs. The elements trigger at nearly the same current density indicating the substrate-coupled triggering mechanism found previously under TLP regime. On-resistance and holding current aspects are also discussed.

Schedule

Times listed in UTC+02:00 Access via Microsoft Teams unless noted

start	end	Monday
13:00	15:00	**Tutorial: Advanced TLP Applications** Heinrich Wolf, Fraunhofer EMFT
15:00	15:30	Break
15:30	16:30	**Seminar 1: Achieving Meaningful and Repeatable Results in ESD System Level Testing** David Pommerenke, Technical University of Graz
16:30	16:45	Break
16:45	17:45	Welcome entertainment- Chocolate Presentation
17:45	19:45	Networking/ Social Gathering via Spatial Chat

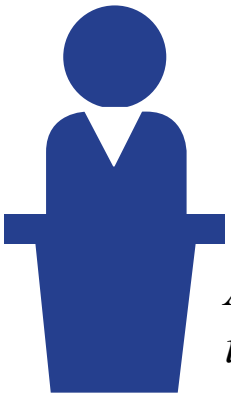
start	end	Tuesday
8:00	8:30	Welcome
8:30	9:30	**Keynote: ESD Protection for Medical Implants** Wolfgang Krautschneider, Hamburg University of Technology
9:30	10:00	Break
10:00	11:00	**Invited talk 1: UTBB FD-SOI and ESD/Latch-up: Challenges and Solutions** Philippe Galy, STMicroelectronics
11:00	12:00	**Seminar 2: Correlation of Qualification ESD Robustness and Handling Threats** Wolfgang Stadler, Intel Deutschland GmbH
12:00	13:00	Lunch
13:00	13:30	Technical session A: Simulation Related Topics
13:30	15:00	Poster discussion session A via Spatial Chat
15:00	15:15	Break
15:15	16:15	**Invited talk 2: Reliability Challenges in Scaling Era with System Technology Co-Optimization (STCO) Approach** Dimitri Linten, imec
16:15	16:30	Break
16:30	18:00	Discussion Group Session A via Spatial Chat A.1 ESD Challenges for Advanced CMOS (FD-SOI, Beyond FINFETS) Co-Moderators: Shih Hung Chen, imec; Philippe Galy, STMicroelectronics A.2 System Level Test: is it Appropriate for IOT Devices/ Wearables? Co-Moderators: Adrijan Barić, University of Zagreb Faculty of Electrical Engineering and Computing; Harald Gossner, Intel Deutschland GmbH A.3 Is Latch-up Testing Still Relevant? Moderator: Guido Quax, NXP Semiconductors
18:00	20:00	Networking/ Social Gathering via Spatial Chat

Schedule continued

Times listed in UTC+02:00 Access via Microsoft Teams unless otherwise noted

start	end	Wednesday
8:00	8:10	Announcements
8:10	9:10	**Seminar 3: EMC of Integrated Circuits, An Introduction to Test Methods** Mario Rotigni, STMicroelectronics
9:10	9:30	Break
9:30	10:30	**Invited talk 3: EM Induced Fault Attacks and their Security Exploitation** Ingrid Verbauwhede, KU Leuven
10:30	11:00	Break
11:00	11:30	Industry Council Report
11:30	12:00	Report on DG Session A
12:00	13:00	Lunch
13:00	13:30	Technical Session B: System-Level and General Testing Aspects
13:30	15:00	Poster Discussion Session B via Spatial Chat
15:00	15:15	Break
15:15	16:15	**Seminar 4: Stress Current Rise Time Evaluation in the Single-Digit Picosecond-Domain** Johannes Weber, Fraunhofer EMFT
16:15	16:30	Break
16:30	18:00	Discussion Group Session B via Spatial Chat B.1 ESD Induced Soft Failures Moderator: David Pommerenke, Technical University of Graz B.2 Health monitoring: Can we use Transient Event Detection of EOS/ESD to Build More Resilient Systems? Co-Moderators: Franz Dietz, Henning Lohmeyer, Robert Bosch GmbH; Patrice Besse, NXP Semiconductors B.3 Testing Devices for CDM Below 150 Volts Moderator: Marko Simicic, imec
18:00	20:00	Networking/ Social Gathering via Spatial Chat

start	end	Thursday
8:00	8:10	Announcements
8:10	8:40	Report on DG Session B
8:40	9:30	Technical Session C: Device Physics and Testing
9:30	11:00	Poster Discussion Session C via Spatial Chat
11:00	11:15	Closing



This year's IEW Presenter is sponsored by ...

Your company can be a proud sponsor of the IEW speakers and receive special recognition for your support of EOS/ESD Association, Inc!

At the 2021 IEW we are offering an exciting new opportunity for interested companies. Companies will have the opportunity to sponsor the Keynote, Invited Talks, and Seminars. Sponsorship recognition (company name and logo) will be given to sponsoring companies during the IEW sessions and in the IEW electronic handouts to attendees. Sign-up today to take advantage of this exciting sponsorship opportunity at the 2021 IEW.

2021 International ESD Workshop

May 17 - 20, 2021

If you are interested in sponsoring please fill out the information below or contact EOS/ESD Association, Inc. today!

Yes, I want to be a sponsor! ☑ $500

Amount enclosed $ _____ ☐ Check ☐ Credit Card

Credit card type: ☐ Visa® ☐ Mastercard® ☐ American Express® ☐ Discover®

Credit card number: _____ Expiration date: _____

Name on card: _____ Security code: _____

Cardholder's signature: _____

Cardholder billing address: _____

First Name: _____ Last Name: _____

Company Name: _____

Street: _____ City: _____

State/Province: _____ Country _____ Zip/Postal Code: _____

Phone: _____ Email: _____

Sponsor name to appear in publicity _____

Setting the Global Standards for Static Control!

EOS/ESD Association, Inc. 7900 Turin Rd., Bldg. 3 Rome, NY 13440-2069, USA
PH +1-315-339-6937 • Email: info@esda.org • www.esda.org

ESD ASSOCIATION®

International ESD Workshop Registration Form

May 17-20, Virtual

Attendee: _____

Company: _____

Address: _____

City: _____ State: _____ Zip: _____ Country: _____

Phone: (____) _____ E-mail: _____

Virtual registration (using Microsoft Teams) $300

Register by April 1st, 2021 to receive chocolate before event

Cancellation & refund requests will be considered if received in writing no later than April 1, 2021, and are subject to a $50 fee. Any other approved dispositions will also be assessed a $50 fee.

The German ESD FORUM e.V. supports the attendance of up to five students from Austria, Germany, or Switzerland. Students from these countries may apply for a $300 USD grant for IEW attendance from the German ESD FORUM e.V. (info@esdforum.de) until April 1, 2021.

Method of Payment

☐ Check — Only U.S. currency, checks drawn on a U.S. bank that is a member of the U.S. Federal Reserve will be accepted.

☐ Wire transfer — $15 fee

To pay by credit card, register online at https://www.cvent.com/d/7nqvf5

Discussion Groups

I am interested in the following discussion group(s)

Choose one from group A	Choose one from group B
☐ DG A.1	☐ DG B.1
☐ DG A.2	☐ DG B.2
☐ DG A.3	☐ DG B.3

Total Enclosed $ _____

Make checks payable to: ESD Association
Purchase orders not accepted for registration

Posters

Will you be bringing a poster to the open poster session? ☐ Yes ☐ No

If yes, what is the title of your poster? _____

Special Interest Groups

Would you like to form a new SIG? ☐ Yes ☐ No

If yes, what is the proposed topic for your group? _____

Setting the Global Standards for Static Control!

EOS/ESD Association, Inc. 7900 Turin Rd., Bldg. 3 Rome, NY 13440-2069, USA

PH +1-315-339-6937 • Email: info@esda.org • www.esda.org

2021 INTERNATIONAL ESD WORKSHOP

An exclusive virtual event!

May 17-20, 2021

APPLICATION FOR Vendor Presentation

Name of Company:_____

Street Address:_____

City, State, Postal Code:_____

Country:_____

Telephone:_____

Contact:_____Email:_____

Please provide web address to be used for your link on ESDA website: _____

We will exhibit and demonstrate the following products or services:_____

_____

We are_____Manufacturers_____Other (please specify)_____

Vendor Presentation Spot: $500.00 USD
FULL PAYMENT DUE WITH REGISTRATION

One Spot_____ Two Spots_____ Three Spots_____

Amount enclosed $_____ ☐ Check ☐ Visa® ☐ MasterCard® ☐ American Express® ☐ Discover®

Credit card number:_____ Expiration date: _____

Name on card:_____ Security code: _____

Cardholder's signature:_____

Billing Address_____

City:_____ State:_____Zip/Postal Code:_____

Application By:_____ Date: _____
(Signature)

NOTES:
1. Each exhibitor receives a 3-5 minute prerecorded video spot.

EOS/ESD SYMPOSIUM ON DESIGN AND SYSTEM

An exclusive Virtual/On-Demand Symposium on Design and Systems
Opens June 23rd. Access is 60 days

EOS/ESD Association, Inc. is sponsoring the 1st International EOS/ESD Symposium on Design and System (IEDS). IEDS is dedicated to the fundamental understanding of issues related to electrostatic discharge on design and system and the application of this knowledge to the solution of problems.

Seminars - Technical Sessions - Keynote - Workshops

Presented papers will be related to the following tracks:

- Advanced CMOS EOS/ESD and Latch-up
- ESD protection in Bipolar, RF, High-voltage, and BCD technologies
- ESD modeling, simulation and design automation
- EOS/ESD Failure analysis and case studies
- ESD and latch-up testing
- System ESD design and troubleshooting issues
- ESD manufacturing control issues and target level discussion

Conference Chair:
李军俊 (Junjun Li) ESD Association

Conference co-Chair:
董树荣 (Shurong Dong) 浙江大学 (ZJU)

Technical Program Chair
王源 (Yuan Wang) 北京大学 (PKU)

Technical Program co-Chair
刘志伟 (Zhiwei Liu) 电子科技大学(UESTC)

Setting the Global Standards for Static Control!
EOS/ESD Association, Inc. 7900 Turin Rd., Bldg. 3 Rome, NY 13440-2069, USA
PH +1-315-339-6937 • Email: info@esda.org • www.esda.org

Registration -

2021 INTERNATIONAL EOS/ESD SYMPOSIUM ON DESIGN AND SYSTEM (IEDS)

Register Online!
http://www.cvent.com/d/3yq3gg

1 Please Print or Type (Your name and company will appear on badge and/or certificate exactly as written below.)

Mr./Mrs./Ms.: _____ First Name: _____ Last Name: _____

Company Name: _____

Job Title: _____

Street: _____ City: _____

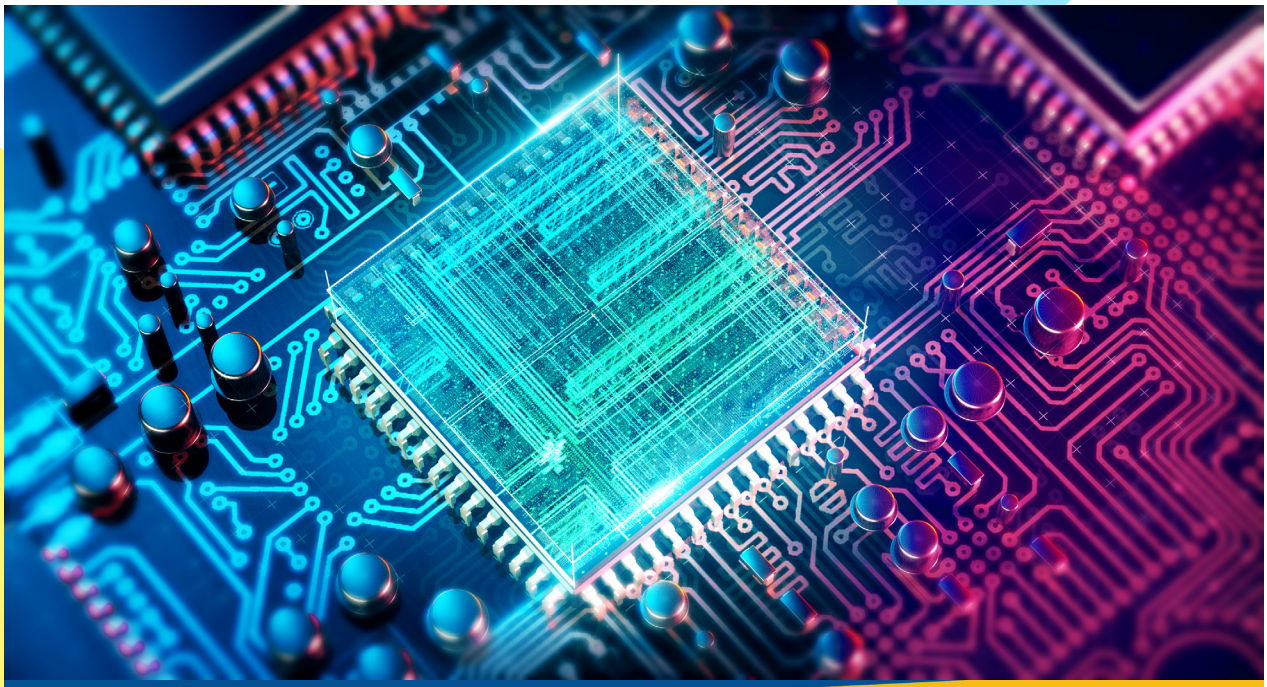
State/Province: _____ Country _____ Zip/Postal Code: _____

Address is (please circle the one that applies) Home or Company

Phone: _____ E-mail: _____

Symposium

☐ **International EOS/ESD Symposium on Design and System (IEDS) 60 day access.** $300



EOS/ESD Association, Inc. Tutorials in Singapore

Lifelong Learning Institute
11 Eunos Rd 8, Singapore 408601
August 16-19, 2021

Essentials for ESD Programs Factory:
Technologies • Controls • Procedures

AUGUST 16-17, 2021 9:00 AM - 5:00 PM

Marcus Koh, Everfeed Technology Pte Ltd.; Bernard Chin, Qorvo

This Seminar offers a broad exposure to the essentials of ESD control systems and programs. It offers a two-day comprehensive set of factory technologies and procedures designed for managers, technicians, and specialists desiring ESD control program training and information. The key concepts and information from the courses listed have been selected for this two-day seminar. Demonstrations and videos are included in this seminar. Examples of electrostatics and ESD calculations are included where appropriate throughout the seminar.

- ESD Basics for the Program Manager
- Ionization and Answers for the Program Manager
- Packaging Principles for the Program Manager
- System Level ESD/EMI: Testing to IEC and Other Standards
- Cleanroom Considerations for the Program Manager
- How To's of In-Plant ESD Survey and Evaluation Measurements
- Device Technology and Failure Analysis Overview
- Electrostatic Calculations for the Program Manager and the
- ESD Engineer
- ESD Standards Overview for the Program Manager
- ESD Program Development & Assessment (ANSI/ESD S20.20 Seminar)

DAY 1 August 16

PART I (9:00 AM-12:30 PM)

This section reviews the fundamentals of electrostatics, charge flow, electric field and voltage. The concept of capacitance and the fundamental relationship, Q = CV, is introduced and explored with demonstrations and videos. The practical application of these concepts to the measurement of resistance, fields and voltages, and the relevant standards are reviewed and demonstrated.

DAY 2 August 17

PART III (9:00 AM-12:30 PM)

Key ESD technical areas are reviewed such as air ionization, ESD-safe packaging, cleanroom principles and electrostatic attraction. Standards relevant to these areas are described.

PART II (1:30 PM-5:00)

The principles from Part I are then applied to grounding principles and standards, measurement of charge, standard models for ESD (i.e., human-body model and charged device model), and static induction with demonstrations and videos. Very simple and basic ESD protection circuit concepts and relevant failure analysis techniques are introduced and reviewed.

PART IV (1:30 PM-5:00)

The final section includes charge generation test methods, additional ESDA standards, system-level ESD standards and testing, practical auditing techniques and strategies, and ESD event detection. The tutorial concludes with a review of ESD Protected-Areas (EPAs), ESD Program Management and the application of ANSI/ESD S20.20.

EOS/ESD Association, Inc. Tutorials in Singapore

Lifelong Learning Institute
11 Eunos Rd 8, Singapore 408601
August 16-19, 2021

First Name: _____ Last Name: _____

Company Name: _____

Street: _____ City: _____

State/Province: _____ Country _____ Zip/Postal Code: _____

Address is (please circle the one that applies) Home or Company

Phone: _____ E-mail: _____

Tutorial Selection

☐ August 16-17 Essentials for ESD Programs Factory: Technologies • Controls • Procedures	$680 USD
☐ August 18 ESD Basic and FC140: System Level for the Program Manager	$460 USD
☐ August 19 Compliance Verification and Auditing	$460 USD

Register Online at: http://www.cvent.com/d/dhqzmn

Setting the Global Standards for Static Control!

EOS/ESD Association, Inc. 7900 Turin Rd., Bldg. 3 Rome, NY 13440-2069, USA

PH +1-315-339-6937 • Email: info@esda.org • www.esda.org

Coming Soon

The first ever IEW in Asia is coming to Taiwan in 2022!