2nd Annual International EOS/ESD Symposium on Design and System (IEDS)

November 9-11, 2022

Setting the Global Standards for Static Control!

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2022 IEDS – Capturing Latest ESD Research Topics from the Greater China Region and the World

As random as it may seem, lightning always seeks its way through the cloud onto the earth, exactly following the law of physics. The charge accumulation, the close contact, the least resistive path, and finally, the energy dissipation! As exciting as it sounds, this part of physics is waiting to be explored year after year. For the second time, plenty of the latest ESD research topics from the Greater China Region and the world are captured by the IEDS 2022 event!

Welcome to the International EOS/ESD Symposium on Design and System (IEDS), where the mind and energy of top research universities and leading industry R&D groups are showcased at this annual event. Our keynote speaker, Professor Ming Dou Ker, opens the conference with a talk on "Circuit Solutions to Improve Latch-up Immunity of CMOS Integrated Circuits". Our seminars focus on four hot topics to solve today's ESD problems: RF, system, high-voltage, and TCAD, each to be taught by its leading expert from a very specialized area. Following these, we have carefully arranged two days of technical sessions from submitted research papers and specially invited speakers. These presentations are scheduled in two parallel tracks, so you can always find something interesting to attend. After each day of technical sessions, we have invited recognized experts in the EOS and ESD technical fields to host a one-hour workshop. Attendees can choose their interested field for either brainstorming discussions or getting answers to questions not fully addressed in the presentations.

This year's IEDS conference is a virtual event with all live-streaming talks. While you attend different sessions, we encourage you to drop by the exhibitor hall where vendors showcase their latest products to conquer ESD problems and to assist with your daily jobs. You may be surprised by how much can be done from today's product lines, either testing equipment, EDA design tools, or newly invented materials. If you cannot find a solution, do not hesitate to ask!

We sincerely wish your 2nd IEDS experience is as fruitful as we designed and hoped. Most importantly, we wish that IEDS connects you to other ESD enthusiasts! In return, the ESD community thanks you for your curiosity and contribution!

Seminar Session A
Wednesday, November 9, 9:00 – 11:30 (UTC +8)

S.1 ESD Design for High Voltage Applications
Lorenzo Cerati, STMicroelectronics

This seminar introduces ESD design in high voltage technologies for integrated circuits with pin voltages from 12V upwards. An overview of different technologies and their typical device portfolios is given, highlighting the most common applications and requirements in the various fields where these technologies are used. Different ESD protection concepts are then introduced, analyzing the advantages and disadvantages of the many possible approaches to implementing ESD networks (diodes, snapback, active clamps, etc.) and providing some design-related challenge examples.

Lorenzo Cerati is ESD Design Solutions Technical Director and Fellow of Technical Staff at STMicroelectronics. Lorenzo received his M.Sc. degree in telecommunication engineering at the "Politecnico di Milano" Technical University in 1998, discussing a thesis on a CdZnTe cross-connect for optical networks. Since 2000, he has worked in STMicroelectronics in the ESD protections development team for Smart power technologies. Now, Lorenzo is the manager of the group responsible for ESD protection development, latch-up immunity, and bipolar parasitic analysis in BCD processes. He is also responsible for design team support to define, implement, and debug complex ESD architectures in BCD ICs.
Lorenzo represents STMicroelectronics in the ESDA standardization committees and is a member of JWG HBM, JWG CDM, WG5.4, WG 5.5 (where he is acting as vice-chairman), WG 5.6, and WG 14. Since 2016, he has also served as a technical and advisory support committee (TAS) member. Lorenzo served multiple times as a member of the ESREF, ICICDT, IRPS, IEW, and EOS/ESD Symposium technical program committees and authored several papers on ESD and EDA topics. Since 2015, Lorenzo is a member of the EOS/ESD symposium steering committee and was General Chair at the 2020 EOS/ESD symposium. Lorenzo has been a member of the ESDA Board of Directors since 2015.

Seminar Session A
Wednesday, November 9, 14:00 – 17:30 (UTC +8)

S.3 TCAD Fundamentals and First Applications to ESD
Kai Esmark, Infineon Technology AG.

TCAD (technology computer-aided design) tools have become an indispensable utensil for the semiconductor industry. There are countless possibilities to analyze, predict and optimize a certain semiconductor device behavior through modeling semiconductor fabrication and device operation. This includes the area for ESD and latch-up development, as early access to fundamental device parameters under very high current density and high-temperature transients are the key to overcoming the conceptual problem of concurrent engineering for ESD engineers. The first part of this tutorial is dedicated to a basic introduction to the TCAD world, including process and device simulation. Focus points are the capabilities but also limitations of these tools, like the requirements for a 2D/3D simulation approach and the validity of the models describing the fundamental physics, especially in the high-temperature regime.
The second part sheds light on selected applications, allowing the attendee to understand what typical ESD-related questions can be addressed by such alternate development and analysis techniques and the typical approach to get reasonable answers by the simulation tools.

Kai Esmark has experience in ESD and EOS for more than 20 years now. He is the senior principal for "overvoltage robust design" in the automotive business group of Infineon in Munich (Germany). In his role, he takes care of the development of robustness concepts against electrically related threatening scenarios on IC- as well as on the system level. He also acts as a consultant at Infineon regarding EOS (better: EIPD) related field returns supporting root cause findings.
Kai contributes to developing standard practice documents in the automotive industry dealing with semiconductor devices showing a signature of electrical overstress. These activities closely cooperate with USCAR (United States Council for Automotive Research) and VDA (German Association of the Automotive Industry). At the same time, he is serving the ESDA as an instructor giving tutorials at the annual EOS/ESD symposium about EOS and the use of TCAD tools for ESD development purposes.

Seminar Session B
Wednesday, November 9, 9:00 – 11:30 (UTC +8)

S.2 Introduction to RF ESD Design
Kathleen Muhonen, Qorvo

This seminar is an introduction to RF concepts and RF ESD clamp design. It is intended for ESD engineers who do not have an RF background to learn the concepts needed to design effective protection circuits. The RF concepts include impedance matching and smith chart basics. RF amplifier operation and load line basics are presented to give a foundation for the RF ESD protection circuit design. The seminar also touches briefly on RF switches and filters. The second half of the seminar focuses on designing an ESD clamp for an RF application. Concepts are presented, such as calculating the turn-on voltage of the clamp such that it protects the part but does not turn on during normal RF operation. A clamp's parasitics also need to be considered in an RF application so that the parasitics do not degrade the product's performance. Finally, some testing tools are reviewed concerning testing RF products. The challenges are highlighted, and different testing practices used in HBM, TLP, and IEC testing of RF products are reviewed.

Kathleen Muhonen is a principal development engineer at Qorvo in Greensboro, NC. She is responsible for developing ESD (electrostatic discharge) on-chip protection for mobile and millimeter wave applications. She is also involved with system-level testing and helped standardize IEC testing of RF components. She is heavily involved in ESD instrumentation for better ESD characterization of clamps and materials. Previously she was responsible for RF characterization and model support for Silicon and Gallium Arsenide technologies for power amplifiers, switches, and antenna tuners. She has also done extensive work on developing state-of-the-art harmonic characterization of semiconductors, breakdown characterization of RF switches, and improved de-embedding techniques of large-scale switches. Kathleen's previous experience includes assistant professor at Penn State Erie, linearization design for base stations at Hewlett Packard, and millimeter wave power amplifier design at Lockheed Martin and GE Aerospace. Kathleen has served as an EOS/ESD Association, Inc. member and sits on all device testing standards committees. She has also served on the Board of Directors and is on the Education Committee.
Kathleen received her BSEE degree from Michigan Technological University in 1991, an MSEE from Syracuse University in 1994, and a Ph.D.EE from Penn State University in 1999.

Seminar Session B
Wednesday, November 9, 14:00 – 17:30 (UTC +8)

S.4 Progress in System Efficient ESD Design of I/O protection

David Pommerenke, Graz University of Technology

The seminar shows progress on SEED design using examples that:

- characterize TVS
- characterize I/O
- combine TVS and I/O
- includes examples from RF front-end design

The test methodology based on a modular system is described in detail to show improvement in understanding the interaction between external and internal ESD protection.

Dr. David Pommerenke received his Diploma and Ph.D. from the Technical University Berlin, Germany. His research interests include EMC, RF interoperability, system-level ESD, electronics, numerical simulations, EMC measurement methods, and instrumentation. After working at Hewlett Packard for 5 years, he joined the Electromagnetic Compatibility Laboratory at the Missouri University of S&T in 2001 and changed to CTO at ESDEMC in 2019. Since 2020, he has been a professor at the Graz University of Technology in the EMC and RF coexistence laboratory. He has co-authored over 200 journal papers and is an inventor on 13 patents. He is an IEEE Fellow and associated editor of the TEMC.

Keynote
Thursday, November 10, 8:30 – 9:30 (UTC +8)

Circuit Solutions to Improve Latch-up Immunity of CMOS Integrated Circuits
Ming-Dou Ker, Institute of Electronics, National Yang Ming Chiao Tung University

The parasitic p-n-p-n structure is inherent in the bulk CMOS technology, which often causes latch-up failure of CMOS ICs during field applications. In applications with harsh environments (for example, automotive electronics), the overshooting/undershooting noise glitches coupling to the microelectronics systems (equipped with CMOS ICs) would be huge. The latch-up immunity of CMOS ICs in such harsh applications has been requested with a much higher specification than that used in consumer electronics. This speech gives a brief background of latch-up in CMOS ICs. The basic layout method is introduced to prevent latch-up occurrence on the I/O cells. Even if the I/O cells of a CMOS IC are free from latch-up, the core circuits in the CMOS ICs are still sensitive to latch-up issues. Thus, several novel circuit solutions to significantly improve latch-up immunity of CMOS ICs, which have been proven in silicon chips, are presented. Finally, some non-typical latch-up paths between the HV and LV blocks across different power domains in the mixed-voltage ICs are discussed. Some methods are shown to overcome such non-typical latch-up issues in the mixed-voltage ICs. Latch-up prevention in CMOS ICs by circuit solutions is an emerging topic that IC designers need to know.

Ming-Dou Ker received his Ph.D. from the Institute of Electronics, National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 1993. He worked as the department manager with the VLSI Design Division, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. From 2012 to 2015, Professor Ker was the Dean of the College of Photonics, National Chiao-Tung University (NCTU), Taiwan. Now, he is the Chair Professor in the Institute of Electronics, National Yang Ming Chiao Tung University (NYCU), Hsinchu, Taiwan. Currently, Professor Ker is the Director of the Institute of Pioneer Semiconductor Innovation, NYCU, and the Director of Biomedical Electronics Translational Research Center, NYCU. In the technical field of reliability and quality design for microelectronic circuits and systems, he has authored/co-authored over 600 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted hundreds of U.S. patents. He had been invited to teach and/or consult the reliability and quality design by hundreds of design houses and semiconductor companies in the worldwide IC industry. His inventions and designs have been widely used in

modern IC products and electronic systems. His current research interests include the reliability and quality design for nanoelectronics and gigascale systems and the circuits and systems for biomedical applications.

Prof. Ker had served as a member of the technical program committee and the session chair of numerous international conferences for many years, including IEEE Symp. on VLSI Technology & Circuits, IEEE International Solid-State Circuits Conference (ISSCC), IEEE International Symp. on Circuits and Systems (ISCAS), and IEEE International Reliability Physic Symp. (IRPS). He served as the Distinguished Lecturer in the IEEE Circuits and Systems Society (2006–2007) and the IEEE Electron Devices Society (2008–2020). Professor Ker served as Associate Editor of IEEE Transactions on VLSI Systems, Associate Editor of IEEE Transactions on Biomedical Circuits and Systems, and a Guest Editor for Frontiers in Neuroscience on the research topic of microelectronic implants for the central and peripheral nervous system. He was the Founding President of the Taiwan ESD Association, the 3rd President of the Taiwan Engineering Medicine Biology Association, and the Vice-President of the IEEE Taipei Section. Currently, he is serving as the Editor of IEEE Trans. on Device and Materials Reliability, Editor of IEEE Journal of the Electron Devices Society, and a Guest Editor for IEEE Trans. on Electromagnetic Compatibility on the special issue of "Electrostatic Discharge and Immunity – from IC to System". Prof. Ker has been a FELLOW of the IEEE since 2008.

2020 EOS/ESD Symposium Outstanding Paper Award
Thursday, November 10, 9:30 – 10:00 (UTC +8)

Cable Discharge Event Simulation and Measurement Methods
Pasi Tamminen, Danfoss (formerly EDR&Medeso)

Cable discharge events can damage sensitive electronics, and these risks can be estimated with measurement and simulation methods. Here measured cable discharges are compared to 3D simulation and vector network analyzer S-parameter-based discharge current calculations. This study shows that real-world cable discharge events can be estimated based on calculation methods.

Pasi Tamminen received the M.Sc degree in Electronics Engineering from Oulu University, Finland, in 1997 and continued to work in NOKIA Networks with automated production technologies, testing, machine vision, process control, and design for manufacturability. From 2001 to 2005, he was at VTT Technical Research Centre of Finland and worked with risk management, EMC/ESD, and cleanroom control methods. He received the NARTE ESD Engineer certification in 2005. Between 2005 and 2012, Pasi worked in NOKIA Mobile Phones by coordinating cleanroom technology and ESD/EMC/EMI control and design-related projects globally in manufacturing and supported R&D, sourcing, and quality. Between 2014 and 2015, he worked in Microsoft R&D on product EMC designs. In parallel, Pasi has worked with IEC and ANSI standardization bodies since 2006, done research on electrostatics, RF, EMC/ESD failures, component and system EMC/ESD/RF qualification, and control methods. He joined the Tampere University of Technology in 2012 and received a Doctor of Science and Technology degree in January 2017. Since 2017 Pasi has worked in EDR&Medeso on high-frequency electromagnetic simulations. Typical applications are ultra-fast ESD events, medical systems, matrix antennas, radars, microwave systems, military systems, RF filters, and automotive electronics.

Technical Session A1
Advanced CMOS, ESD Modeling, and Simulation
Moderator: Guangyi Lu
Thursday, November 10, 10:50 – 12:30 (UTC +8)

A1.1 (Invited) SPICE as a Circuit Simulation Tool for ESD Protection Design and Verification
Yuanzhong Zhou, Analog Devices, Inc.

State of the art in device compact modeling and SPICE simulation for ESD protection design and verification are reviewed. The key physical phenomenon and main challenges for a successful ESD simulation are discussed. The advantages and disadvantages of different modeling approaches are presented. SPICE simulation as a primary ESD design tool is proposed.

A1.2 A Behavioral Model for ESD Self-Protection RF Switches in the SOI CMOS Technology
Jian Liu, Nathaniel Peachey, Qorvo Inc.

A behavioral model for NMOS is built to simulate self-protection SOI RF switches under ESD events. TLP measurement results of multiple-stack SOI RF switches are used to create the ESD model for single-stack NMOS. The transient ESD simulation is performed to explain the SOI RF switch self-protection mechanism transition.

A1.3 Modeling and Reliability Considerations of Over-Driving Active ESD Protection Clamp
Efraim Aharoni, Tower Semiconductor, Kinneret Academic College; Avi Parvin, Yosef Raskin, Victor Kairys, Tower Semiconductor

Reliability constraints and measurements for modeling were investigated for boosted RC Rail Clamp ESD protection, over-driving the gate voltage of the bigFET clamp, during the ESD event. The main concerns of the boosting concept are the validity of the simulation models beyond the nominal operating voltage and possible degradation.

A1.4 Compact Modeling of Reverse Bias TLP I-V Characteristics of ESD Diodes

Sourabh Khandelwal, Danial Bavi, Macquarie University

This paper presents an accurate compact model for transmission line pulse (TLP) I-V characteristics of ESD diodes in reverse bias conditions. The breakdown voltage and post-breakdown I-V behavior of the ESD diodes are accurately modeled with the help of physically motivated model formulations. The ability to model reverse TLP I-V characteristics is one of the features of the new ASM-ESD compact model.

Technical Session D1
ESD Manufacturing and Factory Control
Moderator: Marcus Koh
Thursday, November 10, 10:50 – 12:30 (UTC +8)

D1.1 (Invited) Electrostatic Attraction on Sticky LEDs
Gim Wae Goh, ams Osram

The objectives of this presentation are: 1) articulate how to identify the cause(s) of stickiness if it was material adhesiveness, foreign material or ESA, etc., and 2) understand the root cause(s) helping manufacturing personnel mitigate production AHE unscheduled downtime, such as unit jammed at the track, yield loss or rework.

D1.2 (Invited) Facing Challenges Brought by Charged Board Event and Charge Device Model Failures
Dennis Manaoat Corpuz, AMTC Venture Corporation Ltd.

Using automated, high-precision machines like screen printing, component placement, reflow, soldering, singulation, testing, and packaging carries a risk of CDM and CBE failures. This paper articulates a manufacturing-level approach to deal with this issue that could cripple manufacturability and profit margins.

D1.3 (Invited) Characterization of Static Dissipative Flooring and Footwear to Achieve Low Walking Voltages
Bernard Chin, Qorvo

This paper shows the importance of standard test methods ANSI/ESD STM7.1 and ANSI/ESD STM9.1 during the material selection process of the ESD flooring material and footwear to achieve low walking voltage before large-scale manufacturing implementation. It was found that low resistance footwear produced consistently low walking voltages for different ESD flooring.

D1.4 Continuous ESD Monitoring System for Manufacturing

Kwanghoi Koo, Patrick Xu, Oscar Tang, Amazon

Electrostatic discharge (ESD) damage is a common failure mode in the manufacturing process. This paper introduces a continuous ESD monitoring system for new product introduction (NPI) line ESD qualification and early detection of the potential static charge build-up on the device to defuse the ESD damage risk.

Technical Session C1
System ESD, Failure Analysis, and Case Studies
Moderator: Xiaozong Huang
Thursday, November 10, 14:00 – 16:55 (UTC +8)

C1.1 (Invited) TEM Study of ESD Reliability at the Atomistic Scale
Xing Wu, East China Normal University

Understanding and controlling electrical stress is indispensable to increasing the quality and reliability of advanced devices. This study introduces the technology of transmission electron microscopy (TEM) study of ESD devices with nanoscale resolution.

C1.2 Verification of CDM Issues in IC Designs
Dan Yu, Zhuo Li, LI_SSU_WANG, Chipone Technology (Beijing) Co, Ltd.

Adding CDM protection devices to the connection paths between power domains in IC chip designs can prevent CDM damage. ESD air discharge tests were performed to prove the benefits of implementing CDM protection. A Calibre® PERC™ rule deck-based flow was written to verify that all CDM paths are properly protected.

C1.3 (Invited) 3D and Chiplet ESD Design Challenge
Xin Gao, HiSilicon

System-on-Chip (SoC) technology is consistently evolving. One of the latest advances is 3D packaging, also referred to as "more-than-Moore", to stack multiple chips and stitch chiplets. The 3D integration offers numerous advantages over traditional monolithic SOC design, such as higher performance, shorter global interconnect, and higher bandwidth. Challenges also arise in the ESD field. Chiplet ESD design challenges and verification solutions are discussed in this talk.

C1.4 System Efficient ESD Design of IO ESD Protection

Feifan Deng, Xinyu Zhu, Fangjun Yu, Yipeng Chen, Shurong Dong, Key Laboratory of Micro-nano Electronic Devices and Smart Systems of Zhejiang Province, Zhejiang University; Hongyu Shen, Huawei Technology Co., Ltd.

The failure mode often encountered in system efficient ESD design (SEED) is proposed based on a case: the failure caused by the mismatch between the on-board TVS and the ESD clamp in the chip. The paper presents the SEED method and solves the practical problem with test verification.

C1.5 ESD Verification of a 2.5D CoWoS Package Design

Sen Cao, Sanechips Technology Co., Ltd.; Chenfei Wu, Guohua Zhou, Keqing Ouyang, State Key Laboratory of Mobile Network and Mobile Multimedia Technology, Sanechips Technology Co., Ltd.; Quan Yan, Siemens EDA

In 2.5D chip-on-wafer-on-substrate (CoWoS) package designs, electrostatic discharge (ESD) protection must cover both individual dies and interposer. We expanded ESD design rules to the interposer and used the foundry PDK to check die-level ESD requirements. We ran checks using Calibre PERC software, then compared results against post-silicon ESD test results.

Technical Session B1
ESD Protection in Bipolar, RF, and High-voltage Applications
Moderator: Ming Qiao
Thursday, November 10, 14:00 – 16:55 (UTC +8)

B1.1 (Invited) ESD and EOS Integrated Protection for High Voltage ICs
Hailian Liang, Jiangnan University

The miniature and portable electronics make advanced ICs become higher integration. The electrostatic discharge (ESD) and electrical overstress (EOS) integrated protection for power terminals of electronics is becoming more important and urgent. The integrated ESD/EOS protection chip helps to enhance the ESD and surge robustness by designing the novel structure and utilizing the parasitic effect suppression technology without additional costs.

B1.2 Conceptual Analysis of Bi-directional ESD Device BV(Breakdown Voltage) Shift Phenomenon After TID (Total Ionizing Dose) Test
Lin Zhongyu, Zhong Daohong, Ma Zhen, The 58th Research Institute of China Electronics Technology Group Corporation

In this thesis, we publish a bi-directional ESD device design fabricated on HV CMOS SOI technology. This kind of device is used in the radiation environment. The LET threshold of SEL (single event latch-up) has reached 99Mev•cm2/mg(Si) (tested at The Heavy Ion Research Facility in Lanzhou (HIFRL)). But after the TID (Total-Ionizing-Dose) test, a BV shift was found. The conceptual analysis has been carried out by 2D and 3D TCAD simulations. After that, a proposal to solve the shift is demonstrated.

B1.3 Layout Geometry Impact on ESD Robustness of Multi-Finger Asymmetric DDSCR Devices

Wenjie Guan, Xianguan University, China Hunan Engineering Laboratory for Microelectronics; Yang Wang, Xianguan University, China Hunan Engineering Laboratory for Microelectronics, SuperESD Microelectronics Technology CO., LTD.

The purpose of this work is to optimize the layout of a multi-finger asymmetric dual direction silicon-controlled rectifier (ADDSCR) based on a 0.18-μm CMOS process to achieve high robustness. It can be applied to protect controller area network (CAN) transceiver pins used in automobile computer control systems. From the results, the reverse failure current of the 6-finger ADDSCR device using Layout_II_EN is 29.94A, which improves the reverse robustness of the multi-finger device.

B1.4 (Invited) Stacking Methodology for High Voltage ESD Protection

Da-Wei (David) Lai, Pride Silicon Technology Co., LTD

ESD protection in high-voltage technology is challenging due to narrow design windows, MOSFETs degradation, and those unexpected parasitic paths. Besides, latch-up is a risk when using traditional gate-grounded HV nMOS transistors due to a strong snapback. This talk discusses some practical stacking methodologies for HV ESD protection.

B1.5 Design of Dual-Direction SCR with High Holding Voltage for High Voltage ESD Protection

Yujie Liu, Xiangliang Jin, Hunan Normal University

An improved dual-direction silicon controlled rectifier (IDDSCR) for high-voltage electrostatic discharge (ESD) protection applications has been proposed and verified in a 0.18 μm standard BCD process. Measured TLP results illustrated that the proposed IDDSCR has a high holding voltage of 29.81 V and has good latch-up immunity.

B1.6 An Improved LDMOS-SCR Design for high-Voltage ESD

Xingtao Bao, Xiangliang Jin, Hunan Normal University

In this paper, a 0.18-μmBCD technique was used to design an I-LDMOS-SCR high with maintenance voltage. According to the results of the transmission line pulse test (TLP), the I-LDMOS-SCR maintains a voltage of up to 20.8V, which is suitable for protection against high voltage ESD.

Workshop A.1
Thursday, November 10, 17:30 – 18:30 (UTC +8)

ESD Protection for RF Applications
Nate Peachey, Qorvo

An ever-increasing number of consumer products include RF functionality. From an ESD protection and robustness perspective, the RF circuit provides unique challenges for the designer. At the IC level, on-chip ESD protection must be balanced with performance requirements. Performance requirements sometimes limit the ESD protection level that can be achieved. Furthermore, advanced ESD co-design of ESD protection and RF functionality may be necessary. However, ESD protection cannot be compromised at the consumer product level. Thus the system-level designer has the challenge of designing a high-performance electronic product while still meeting the IEC61000-4-2 requirements for product qualification. This workshop provides a forum to discuss and debate the various design and performance issues related to robust ESD design for RF ICs and consumer products.

Workshop A.2
Thursday, November 10, 17:30 – 18:30 (UTC +8)

Can Robust ESD Design be Achieved and Verified Using IEC 61000-4-2 Testing?
David Pommerenke, Graz University of Technology

A summary is given on IEC 61000-4-2 ESD testing and aspects of robust design to introduce the topic. The discussion is around the following questions:

- Which methods are used in mechanical, electrical, and software design to obtain ESD robust design?
- Which methods are used in design review to identify possible flaws in a design?
- Which problems have been observed with respect to the reproducibility of IEC testing?
- Which methods have been applied to improve reproducibility?
- How should the test standard be improved?

Technical Session A2
Advanced CMOS, ESD Modeling, and Simulation
Moderator: Yuan Wang
Friday, November 11, 9:00 – 12:00 (UTC +8)

A2.1 ESD Protection Design for Fan-Out Panel-Level Packaging

Chun-Yu Lin, Chia-You Hsieh, Zih-Jyun Dai, Yu-Hsuan Lai, National Taiwan Normal University

With a new concept of hetero-integration by combining display and functional redistribution layer (RDL) technologies, the fan-out panel-level package (FOPLP) technology with ESD protection design is studied in this work. The proposed ESD protection circuits in RDL are realized by low temperature poly silicon thin film transistors, and the circuits are used to protect a CMOS inverter. The ESD protection circuits for FOPLP applications are verified in this work.

A2.2 An Improved Area-Efficient Transient ESD Power Clamp

Qi-an Xu, Zhan Xue, Zhongpeng Jiang, Scott Song, Blacksmith Wu, Kanyu Cao, ChangXin Memory Technologies, Inc.

An improved area-efficient transient ESD power clamp is proposed. It uses the double feedback circuit techniques to reduce the RC time constant, which saves the layout area. The new power clamp can discharge the ESD current, tolerate very fast power supply ramp rates, and exhibit reduced area and leakage.

A2.3 Novel Ring Silicon-Controlled Rectifier for ESD Protection of Low-Voltage Circuits

Fangjun Yu, Xinyu Zhu, Feifan Deng, Yipeng Chen, Shurong Dong, Zhejiang University

This paper proposes a novel ring silicon-controlled rectifier (NRSCR) for electrostatic discharge (ESD) protection. The SCR discharge path is introduced by adding a P-type ESD implant layer (P-ESD) to the conventional diode structure. Compared with conventional SCR, the trigger voltage of NRSCR is reduced by 3.2V, and the robustness is about twice that of conventional diode and SCR, which is suitable for ESD protection of low-voltage circuits. The key parameters of the NRSCR are discussed and verified.

A2.4 MOSFET/TFET Mixed Power Clamp Circuit For ESD and Surge Protection

Zhaonian Yang, Xiaohan Yang, Shaanxi Key Laboratory of Complex System Control and Intelligent Information Processing; Yaping Yue, Shandong Inspur Intelligence Research Institute Co., Ltd.; Shi Pu, Xi'an Xiangteng Microelectronics CO., LTD.

This paper proposes a highly sensitive voltage detector, and its electrical characteristics are investigated using technology computer-aided design (TCAD) simulation. Germanium (Ge) source and line configuration TFET is adopted to obtain an ultra-sensitive detection capability. The corresponding operating principle is explained, and the impact of the key parameters on the voltage detector is also discussed. The simulation results show that the new proposed Ge source line TFET-based voltage detector has a low leakage current and high detection sensitivity under the electrostatic discharge (ESD) and surge events compared to traditional detectors.

A2.5 Predicting the ESD Window of GGNMOS Using Neutral Network

Xinyu Zhu, Fangjun Yu, Feifan Deng, Yipeng Chen, Shurong Dong, Zhejiang University

This work introduces a neural network modeling method for predicting the electrostatic discharge (ESD) window of Gate-Grounded NMOS (GGNMOS). Compared with TCAD simulation, the time consumption is reduced by 6 orders of magnitude, and the prediction error is less than 10%.

A2.6 Design of a High-ESD-Robustness Multi-point LVDS Interface Using Current Mirror in 0.18-µm 3.3-V CMOS Process

Lingli Qian, Mingyu Li, Shengdong Hu, Chongqing University; Xiaozong Huang, Chongqing Acoustic-optic-electronic Co. Ltd. Of CETC & 24 Institute

Multi-point low voltage differential signaling (MLVDS) interface with optimized ESD protection is designed and verified in 0.18-µm 3.3-V CMOS technology. Compared with the conventional MLVDS interface, the proposed MLVDS interface has the same parameters with a wide common-mode voltage range of -1.4 V to +3.8 V and a high transmission rate of 200 Mbps. At electrostatic discharge (ESD) events, the proposed MLVDS interface discharges the ESD current by itself without adding a mask and increasing any silicon footprint on ESD protection devices. Moreover, the proposed MLVDS interface is successfully designed to a high ESD robustness of 2.5 kV by replacing polysilicon resistance with a current mirror and optimizing the device layout.

Technical Session B2
ESD Protection in Bipolar, RF, and High-voltage Applications
Moderator: Wei Liang
Friday, November 11, 9:00 – 12:00 (UTC +8)

B2.1 (Invited) Cellphone Front-End-Module (FEM) ESD Protection Review
Alain Loiseau, GLOBALFOUNDRIES

This talk introduces RF switches and their applications in the Front-End-Module (FEM) of cellphones. The typical schematics and modes of operation are described. The self-protection capability of the switches is investigated as well as strategies to enhance the ESD performance. The key electrical requirements of the ESD protection are highlighted.

B2.2 Research on Diodes with the Novel Topological Layout for ESD Protection on High Speed I/O
Qinling Ma, Hailian Liang, Jiangnan University

Three diodes with novel topological layouts were researched and fabricated on the 22-nm CMOS process by using TCAD tools and a TLP test system. The interdigital diode without metal contacts can effectively reduce the turn-on resistance, and the interdigital diode with metal contacts can significantly improve the turn-on speed.

B2.3 New LVTSCR with Low Parasitic Capacitance for RFICs ESD Protection
Aoran Han, Yuxin Zhang, Tiantian Xie, Nanjin Li, Tao Wang, Zhiwei Liu, Xun Luo, University of Electronic Science and Technology of China; Feibo Du, Peking University Shenzhen Graduate School; Fei Hou, Chengdu University

A new low-voltage-triggered silicon-controlled rectifier (LVTSCR) with low parasitic capacitance is proposed for radio frequency integrated circuits (RFICs) ESD protection. Compared with the conventional LVTSCR, the parasitic capacitance of the new device reduces by 58%. It also has tunable trigger voltage (2.0V∼6.5V), low leakage current (∼3nA), and compact size (60×16.3μm2).

B2.4 Study of RC-Diode ESD Protection Circuit for High Frequency Applications

Chun-Yu Lin, Bo-Yan Li, Yi-Quan Fu, National Taiwan Normal University

The RC-diode ESD protection circuit has been presented to offer ESD protection in high-frequency integrated circuits. The protection circuit combines the ESD protection diodes with the embedded silicon-controlled rectifier (SCR) and the inserting resistors to provide the appropriate performances, including ESD-current-handling ability, signal loss, and layout area. This work provides a thorough study of RC-diode ESD protection circuit in CMOS silicon chip.

B2.5 An Open Short De-Embedding Accuracy Correction Methodology for On-Chip High-Speed ESD and RF Component Characterizations

Guangyi Lu, Wei Gao, Lihui Wang, Xin Gao, Mei Li, Hisilicon Technologies Co., LTD

An open short de-embedding accuracy correction methodology is presented in this paper. With the assistance of electromagnetic simulation, the error-inducing factor in silicon-data de-embedding is well reproduced and understood. The de-embedding correction algorithm is then fine-tuned by simulation and applied to subsequent silicon-data analyses.

B2.6 Implementation of Dual-Collector NPN BJT-Based ESD Protection Devices with Stable and High ESD Current

Jongkyu Song, Jin Heo, Jangkyu Choi, Jiho Kim, Jeahyun Yoo, Jooyoung Song, ChanHee Jeon, Samsung Electronics

A dual-collector NPN BJT is proposed for high-voltage ESD protection. The dual collector is formed by separating the N+ region of the collector using STI, allowing stable and high It2. To obtain the expected Vh and high It2, P-type doping concentration under the emitter is increased by combining different P-type layers of the base. The proposed ESD protection device is verified in silicon with 39% of It2 improvement and 23% area reduction.

Technical Session C2
System ESD, Failure Analysis, and Case Studies
Moderator: Chun-Yu Lin
Friday, November 11, 14:00 – 16:30 (UTC +8)

C2.1 (Invited) ESD Optimization Strategy for a High Voltage Driver with Negative Power Supply Rail
Xiaozong Huang, CETC & 24 Institute

ESD protection for high voltage ICs is essential and tough, especially for circuits with multiple power domains. In this work, a high voltage driver with a 28V power supply is analyzed due to the ESD robustness optimization requirements. An improved SCR with trigger voltage of ~43V and failed current It2 of ~5A takes the role of initial diodes. Meanwhile, the extra considerations of multi-domain and negative power supply rail are discussed to improve the ESD robustness of the whole chip from ~1000V to over 2500V.

C2.2 Multiple ESD Clamps and Decapacitor Sensitivity
Ritesh Agarwal, Vicky Batra, STMicroelectronics Pvt Ltd.

Historical credence had been that the more the number of ESD power clamps, the better it is for the ESD performance of an SoC. In advanced RF analog SoC, with more than 32 parallel ESD clamps and a large decoupling capacitor (order of nano-Farads), an unexpected failure occurred wherein these ESD power clamps could not limit the allowed ESD maximum stress voltage (MSV) to acceptable limits for a small range of ESD stress (termed as HBM ESD window). Analysis of the failure is presented, along with successful circuit fixes and techniques that ensure the safe operation of these circuits.

C2.3 Transmission Line Pulse Induced Breakdown of FinFETs
Xin Yang, Zuoyuan Dong, Yunhan Qian, Zijian Zhang, Fang Liang, Chen Luo, Chaolun Wang, Xing Wu, East China Normal University; Yihong Qing, Zhiwei Liu, University of Electronic Science and Technology of China; Kuei-Shu Chang-Liao, National Tsing Hua University; Yongren Wu, Chihang Tsai, Chinaisti (shanghai) Testing Technology Co., Ltd

As a result of the shrinking size of semiconductor circuits, fin field-effect transistors (FinFETs) with better gate control ability become a promising candidate in advanced nanodevices. Enhanced reliability is required for complex three-dimensional conductive channels. Understanding and controlling dielectric breakdown is indispensable to increasing the quality and reliability of advanced

devices. In this study, physical failures in FinFET devices induced by electrical overstress (EOS) and electrostatic discharge (ESD) were analyzed by using transmission electron microscopy (TEM) with nanoscale resolution. Two electric technologies are direct current (DC) and transmission line pulse (TLP). Interaction between current-temperature positive feedback and dielectric breakdown-induced epitaxy (DBIE) was studied. Under the DC stressing, the Si grew along with three sides of the fin, and the dielectric layer was destroyed by the stress. Contrarily, the TLP stress only wore and tore the dielectric layer, and the Si grew downwards. The technology computer-aided design (TCAD) simulations show that the breakdown depends on the balance between current-temperature positive feedback and the DBIE mechanism. This work provides guidance for enhancing the reliability of FinFETs.

C2.4 Novel Staircase Wave ESD Testing Method for Accurate Latch-Up Evaluation

Zhao Qi, University of Electronic Science and Technology of China, State Key Laboratory of Electronic Thin Films and Integrated Devices; Yonggang Shi, Fei Zhao, Bo Zhang, University of Electronic Science and Technology of China; Ming Qiao, University of Electronic Science and Technology of China, Institute of Electronic and Information Engineering of UESTC

With the development of the electrostatic discharge (ESD) protection devices, different protection strategies are proposed to increase ESD latch-up immunity, such as high holding voltage (Vh), high holding current (Ih), or double-snapback. As a result, the regular transmission line pulse (TLP) test is difficult to accurately judge latch-up states by the ESD window. In some cases, some high holding current devices are also latched up, although Ih and Vh meet the ESD window. This paper proposed a new testing concept and initially established a new transient staircase wave simulation evaluation system. By introducing the staircase wave simulation, the transient turn-off characteristics of the devices are achieved, which accurately judges their latch-up risks.

C2.5 Failure Analysis of ESD-Induced MOSFET Gate Oxide Damages via Step-by-Step Approach

Xia Luo, Jiexuan Xu, Xiaowei Xu, Zongbei Dai, Chao LI, Hongwei Luo, No.5 Electronics Research Institute of the Ministry of Industry and Information Technology

To discover the ESD-induced MOSFET gate oxide damages after the system-level tests during the product development phase, a systematic failure analysis was conducted via a step-by-step approach, indicating that the adopted approach can identify gate oxide damages.

Technical Session D2
Board and System Level ESD Protection Design
Moderator: Yafei Yuan
Friday, November 11, 14:00 – 16:30 (UTC +8)

D2.1 (Invited) ESD Phenomena and Protections on PCB of the Semiconductor Device or Panel Display (on Module Level)
Yasuhiro Fukuda, ESD Consultant

As the electron system is more vulnerable for ESD, the ESD-gun immunity test (IEC 61000-4-2) is important in the system design. The system is constructed by the semiconductor devices and panel display, etc. The ESD gun test and protection design (SEED, etc.) are requested on the module level. This paper summarizes and analyzes the ESD phenomena, the problem of the ESD gun test method, and protection on the module level.

D2.2 (Invited) Inductive Current Probe for ESD/EOS Measurements
Li Shen, ESDEMC Technology LLC

Inductive current probes are widely applied in ESD/EOS measurements. This presentation covers the considerations in current probe selection and setup for ESD/EOS applications, typical measurement setups and current waveforms (ESD simulator, long pulse TLP, cable discharge), influence from the inductive current probe on ESD current, frequency response calibration, and compensation methods.

D2.3 (Invited) Electrostatic Field Sensors and Applications in Static Instruments
Xiaolong Wen, University of Science and Technology Beijing

Currently, the primary sense principles of electrostatic field sensors (EFS) are field mill and vibrating capacitors. As the demand for better test performance and lower usage cost, we have brought out a new EFS based on micro-electro-mechanical systems (MEMS) technology and developed a series of instruments. The new technique promises to be widely used in EOS/ESD area for monitoring static-related parameters, such as electric field, static voltage, charge density, ion balance, etc.

D2.4 (Invited) Electrostatics Discharge Characteristics of Cable Discharge Event
Yu Zhang, Beijing Orient Institute for Measurement &Test

Cable discharge event (CDE) occurs when cables are electrostatically charged and connected to other interfaces. Its current waveform appears as sequences of oscillating rectangular pulses with fast rising time and short pulse width but high amplitude, which shows a great threat to devices. The waveform characteristics are investigated in the manuscript.

D2.5 (Invited) Simulation and Environment Experiments of Electron-Emitting Film for Prevent Spacecraft Charging and Discharging
Na Feng, Beijing Orient Institute for Measurement &Test

Prevention of spacecraft charging and discharging has become higher bus voltages. Numerous mitigation techniques against spacecraft charging include electron emission from the spacecraft chassis. A new electron emission device operating has been presented in this paper. The basic principle is based on a high voltage solar array tripe junction where the interface of metal and insulator is exposed to space. The electric field at the tripe junction and the current emission of the electron-emitting film were simulated in this paper, which was verified by ground environment experiments.

Workshop B.1
Friday, November 11, 17:00 – 18:00 (UTC +8)

High Voltage ESD Protection Effectiveness and Efficiency - From Component Level to Whole Chip Solutions

Jack Zeng, Globalfoundries

In the IoT era, high voltage technologies are gaining more and more traction spanning a wide range of market segments, while ESD protection for high voltage applications is becoming more and more challenging – constrained by cost, the effectiveness of protection, and safety concerns.
In this workshop, let's come together to find out effective and efficient ESD protection solutions, encompassing device and circuit co-design. What is the specific requirement for High voltage ESD devices from chip to system level (considering SOC design requirements)? Discussions regarding the high voltage ESD design window and SOA boundary of the baseline device are welcome. Some brainstorming about the need for defining a figure of merit (FOM) for high voltage ESD devices and what could be a reasonable FOM for each type of ESD device is encouraged. What kind of high voltage ESD device library is preferred by ESD circuit designers considering the FOM of different types of ESD devices? The discussion also covers the design trade-off between effectiveness and efficiency of high voltage ESD protection – low holding voltage vs. high holding voltage, snapback vs. non-snapback devices, and a plethora of other open issues including, but not restricted to, modeling the snapback region of certain ESD device operation.

Workshop B.2
Friday, November 11, 17:00 – 18:00 (UTC +8)

Challenges and Opportunities in Manufacturing ESD Control
Marcus Koh, Everfeed

China is a big manufacturing country, where the export of mobiles, computers, LCD TVs, etc., takes a large proportion of their total exports and plays an important role in the global overseas trade. It is predicted that, in the coming years, this proportion will become larger, and the export of electronic information products will be near USD1,000 billion*. The growth of China's market will be faster than that of the global market, with a GAGR of 10%, and in 2023, the value of China's electronic manufacturing services (EMS) in the global market is supposed to break USD500 billion.
However, inappropriate manufacturing electrostatic discharge (ESD) control will inadvertently impact products' yield and compromise EMS market value. ANSI/ESD S20.20 and IEC-61340-5-1 are the recognized EMS ESD control best practices, which can help to enhance products' yield and sustain EMS market value. This session attempts to articulate if better understanding and enhanced manufacturing ESD control best practices from backend semiconductor assembly to printed circuit board assembly to fully assembled system could mitigate semiconductor devices' on-chip ESD target reduction.

*Market Analysis of Electronic Manufacturing Services Industry in China 2016-2021, Research and Markets, 2018

Schedule (UTC +8)

Start	End	Wednesday, November 9, 2022
9:00	10:00	S.1 ESD Design for High Voltage Applications (Lorenzo Cerati) S.2 Introduction to RF ESD Design (Kathleen Muhonen)
10:00	10:15	Break
10:15	11:15	S.1 ESD Design for High Voltage Applications (Lorenzo Cerati) S.2 Introduction to RF ESD Design (Kathleen Muhonen)
11:15	11:30	S.1 ESD Design for High Voltage Applications Q&A (Lorenzo Cerati) S.2 Introduction to RF ESD Design Q&A (Kathleen Muhonen)
11:30	14:00	Lunch
14:00	15:00	S.3 TCAD Fundamentals and First Applications to ESD (Kai Esmark) S.4 Progress in System Efficient ESD Design of I/O protection (David Pommerenke)
15:15	16:15	Break
16:15	17:15	S.3 TCAD Fundamentals and First Applications to ESD (Kai Esmark) S.4 Progress in System Efficient ESD Design of I/O Protection (David Pommerenke)
17:15	17:30	S.3 TCAD Fundamentals and First Applications to ESD Q&A (Kai Esmark) S.4 Progress in System Efficient ESD Design of I/O Protection Q&A (David Pommerenke)

Start	End	Thursday, November 10, 2022
8:00	8:30	Opening + Awards
8:30	9:30	Keynote - Circuit Solutions to Improve Latch-up Immunity of CMOS Integrated Circuits (Professor Ming-Dou Ker)
9:30	10:00	2020 EOS/ESD Symposium Outstanding Paper Award Winning Presentation - Cable Discharge Event Simulation and Measurement Methods (Pasi Tamminen)
10:00	10:50	Break + Exhibit Hall
10:50	12:30	Technical Session A1 - Advanced CMOS, ESD Modeling, and Simulation
10:50	12:30	Technical Session D1 - ESD Manufacturing and Factory Control
12:30	14:00	Lunch + Exhibits
14:00	16:55	Technical Session C1 - System ESD, Failure Analysis, and Case Studies
14:50	15:40	Technical Session C1 Break
14:00	16:55	Technical Session B1 - ESD Protection in Bipolar, RF, and High-Voltage Applications
15:15	15:40	Technical Session B1 Break
16:55	17:30	Exhibits
17:30	18:30	Workshop A.1 - ESD Protection for RF Applications

Start	End	Friday, November 11, 2022
		Workshop A.2 - Can Robust ESD Design be Achieved and Verified Using IEC 61000-4-2 Testing?
9:00	12:00	Technical Session A2 - Advanced CMOS, ESD Modeling, and Simulation
9:00	12:00	Technical Session B2 - ESD Protection in Bipolar, RF, and High-Voltage Applications
10:15	10:45	Break
12:00	14:00	Lunch + Exhibits
14:00	16:30	Technical Session C2 - System ESD, Failure Analysis, and Case Studies
14:00	16:30	Technical Session D2 - Board and System Level ESD Protection Design
15:15	15:40	Break
16:30	17:00	Exhibits
17:00	18:00	Workshop B.1 - High Voltage ESD Protection Effectiveness and Efficiency - From Component Level to Whole Chip Solutions Workshop B.2 - Challenges and Opportunities in Manufacturing ESD Control

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