Year in review – SystemLevel ESD

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Scope

Review system level ESD publications since 2015 addressing:
• System level and IC level protection codesign.
• Discharge pulse models and models of IOs and TVS supporting the codesign approach.
• Ultrafast discharges under system ESD conditions like the secondary discharge.
• System and PCB analysis methodology like EM scanning
• Novel approaches in system level ESD testing to address real world soft and hard fails
• Investigations of system level tests and modelling are dominating
• Strong interest in soft fail characterization

Hot Spots

Place of publication
EOSES E Symposium 23
Transactions EMC 23
EMC Symposium 11
APEMC 7
TDMR 3
ACES 1
EDAPS 1
IRPS 1
ASICON 1
AP-RASC 1
CRI Radio Prop 1

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Top Stories –
System level and IC level protection codesign

- Showcasing system level ESD TVS/board/IC codesign approach by using SEED type approach for
  - CAN interface based on TLP IV characteristics (Chuang TDMR 2017)
  - USB interface applying transient models for TVS diodes (Wei IRPS 2018)

C-H Chuang and M-D Ker
‘System-Level ESD Protection for Automotive Electronics by Co-Design of TVS and CAN Transceiver Chips’
IEEE Transactions on Device and Materials Reliability,
VOL. 17, NO. 3, SEP2017

Top Stories –
System level and IC level protection codesign

- Pengyu Wei, Javad Meiguni, David Pommerenke ‘System-Level Design for ESD Protection on Multiple IO Interfaces’,
  Proc. IPRS 2018, Burlingame, CA

And more at EOSESD 2018
Top Stories - SEED Modeling of IOs and TVS


- Full transient analysis of a SEED model
- Shows impact of decap caps as well as powering

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Top Stories - SEED Modeling of IOs and TVS


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Top Stories - SEED Modeling of IOs and TVS


- Relevance of modelling of return path
- Cap and inductor as C(V) and L(I)

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Top Stories - SEED Modeling of IOs and TVS


- Need of a three terminal model
- Dependency of fail threshold on driver state

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Top Stories - SEED Modeling of IOs and TVS

F. Escudie, F. Caignet, N. Nolhier, M. Bafleur,
‘From quasi-static to transient system level ESD simulation: Extraction of turn-on elements’,
Proc. EOS ESD Symposium 2016, 7A-3

Top Stories - Ultrafast Discharges

H. Wolf, H. Gieser,
‘Secondary Discharge – A Potential Risk during System Level ESD Testing’
Proc EOS ESD Symposium 2015, 2B.3
Top Stories - Ultrafast Discharges


- Ultrafast discharges with less than 30 ps risetime

DZ Li, S Marathe, P Wei, A Hosseinbeig, D Pommerenke; ‘Full-Wave Simulation of System-Level Disruption During Secondary ESD Events in a Smartphone’ IEEE Transactions on Electromagnetic Compatibility April 2018, 1 - 8

- Transient cosimulation of 3D EM and circuit simulation
- Coupling of secondary discharge into victim pin
Top Stories - System/PCB/IC analysis methodology

M. Park, J. Park, J. Kim, M. Seung, J. Choi, C. Lee, S. Lee

VDD noise due to a 4kV IEC pulse
• Supply noise shows an oscillating behavior with a time constant of a few 10 ns
• A typical supply noise amplitude measured on PCB is of several 10 mV

N. Thomson, C. Reiman, Y. Xiu, E. Rosenbaum,

• Advantage of on-chip monitors
• Capture supply noise at various nodes
• No need of redesigning of PCB
A Hosseinbeig, OH Izadi, S Shinde, D Pommerenke, H Shumiya, ‘A study on correlation between near-field EMI scan and ESD susceptibility of Ics’, Electromagnetic Compatibility & Signal/Power Integrity (EMCSI) 2017

- EMI analysis identifies regions with high activity
- Higher activity leads to higher ESD sensitivity


- On-chip detector with pulse width dependency
- Use of detectors for design assessment
Top Stories - System/ PCB/IC analysis methodology


- Targeted injection of TLP to one end of a signal line
- Allows to distinguish between sensitivity of receiver and transmitter

Top Stories - Soft Fail Caused by System ESD


- Weak LDO leads to high supply noise under ESD
- Discharge at RX causes TX output noise
Top Stories - Soft Fail Caused by System ESD

- Higher load and removal of Decaps leads to higher ESD susceptibility
- Higher voltage decreases ESD susceptibility

Top Stories - Novel approaches of Systemlevel Testing

- Stress depends on charging of shield or data line
- Discharging the shield first can still lead to high stress of data line
Top Stories - Novel approaches of Systemlevel Testing


- Discharge through Body worn devices
- Very high peak currents


- Gaming station MS Kinect used for detection of posture
- E-field and voltage calculated
- Distant measurement of human body charging possible