EOS/ESD Association, Inc.

Electrostatic Discharge (ESD) Technology Roadmap

EOS/ESD Association, Inc.
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1.0 SYNOPSIS

This document has four main sections. The first section provides estimates of future ESD thresholds for semiconductor devices and the potential impact on ESD control practices. These levels are strongly technology- and design-dependent and should be revised periodically in light of advances in the electronics industry. The threshold estimates discussed in this roadmap reflect prevailing trends in semiconductor technology as viewed by selected industry leaders. As in previous versions, this roadmap emphasizes the integrated circuit (IC) industry. Other major electronics industry segments are also experiencing increased ESD sensitivities (lowering ESD thresholds). Examples include optoelectronics (light-emitting diodes, lasers, and photodiodes), printed circuit board assemblies, and thin-film transistor-based displays and circuits. However, ESD trend information is not usually readily available for these devices, and the standardized ESD tests are not defined or broadly applied.

This document presents the thresholds as "roadmaps" of estimated threshold changes until 2030. These projections provide a view of future device protection limitations driven by circuit performance requirements and technology scaling effects. It also provides a common view of expected ESD performance variations from the perspectives of device (IC) suppliers, original equipment manufacturers (OEMs), and other IC users. Finally, these trends point to the need for continued improvements in ESD control procedures and compliance. The paper also links these trends to process capability and discusses progress in characterizing other ESD events, such as system-level events, charged-board events, and cable discharge events.

The second part covers device testing trends and characterization from the ESDA and ESDA/JEDEC teams working on these methods. It is followed by an outlook on important trends in the semiconductor industry looking towards 2030. The roadmap closes with a section on computation methods and artificial intelligence (AI).

2.0 DEVICE THRESHOLD TRENDS

2.1 Overview

In the late 1970s, ESD became an issue in the electronics industry. ESD events from people were causing device failures and yield losses. As the industry learned about this phenomenon, device design improvements and process changes made devices more robust and processes better able to handle them. During the 1980s and early 1990s, device engineers created protection structures that could withstand higher levels of ESD stress, making devices less sensitive to ESD events. Device engineers and circuit designers identified key technological parameters and design techniques that helped them develop more robust devices.

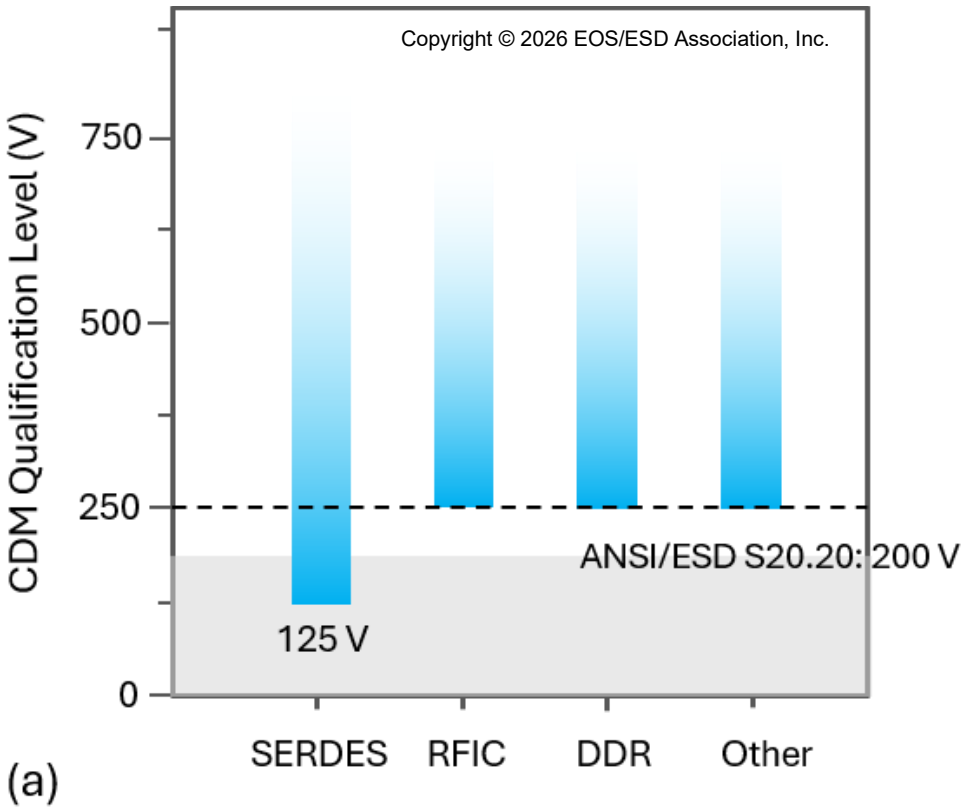
In the mid to late 1990s, the demand for higher performance and the increased circuit density predicted by Moore's Law created problems for traditional ESD protection circuits because this required additional area and added capacitance. Continued scaling toward sub-50 nm feature sizes achieved higher density and performance. Large, high-pin-count (> 1000 pins) packaged devices containing high-speed SERDES (HSS) input/outputs (IOs) operating at 10-15 gigabits per second (Gbps) were introduced to meet demand for high-speed communication applications. With today's advanced technology nodes at 3 nm and beyond, HSS IOs in the 112 Gbps to 224 Gbps range are more prevalent.

Improved ESD control methods now allow us to limit charging voltages in ESD-controlled areas to 100 volts and below. This enables safe handling, manufacturing, and assembly of ESD sensitive IC products even if they are designed for a low ESD target level. Consequently, the human body model (HBM) and charged device model (CDM) target levels have been adjusted. The following section discusses these target levels and the actual ESD qualification levels.

2.2 Device ESD Threshold Roadmaps

The current recommended ESD target levels are 250 volts CDM and 1000 volts HBM. These target levels are safe to use if devices are manufactured, handled, and assembled in ESD controlled areas that follow an ESD control program as defined in ANSI/ESD S20.20 [1], IEC 61340-5-1 [2], or JEDEC JESD625 [3]. Statistical data [4, 5] also justify the recommended ESD target levels, showing no significant difference in ESD-related field returns with reduced HBM and CDM qualification levels. By applying process-related measures based on ANSI/ESD SP17.1 (Section 2.5), the threshold levels can be reduced further to enable applications where the application functionality limits the achievable ESD protection level. For example, a delicate balance often exists between CDM robustness and high-speed data rates. Figure 1 shows the range of CDM and HBM qualification levels published in data sheets for different IO types. These are compared with the recommended target levels of 250 volts CDM and 1000 volts HBM, and the achievable ESD control level based on ANSI/ESD S20.20 [1].

A clear mismatch exists between the recommended target level and the published qualification level obtained from products. Several factors contribute to these differences. For example, the automotive qualification targets are defined by automotive quality requirements. AEC Q100 [7] is a commonly used specification. These requirements extend to automotive communication interfaces like local interconnect network (LIN), controller area network (CAN), and Ethernet, leading to even higher qualification levels for these pins. On the low end of the recommended CDM level, for example, some SERDES products with data rates of 224 Gb/s can achieve only around 125 volts CDM. An example of current products that may not reach the target HBM levels is compound semiconductor devices. For discrete devices and high-performance RF products in particular, HBM withstand voltage may be only 250 volts.



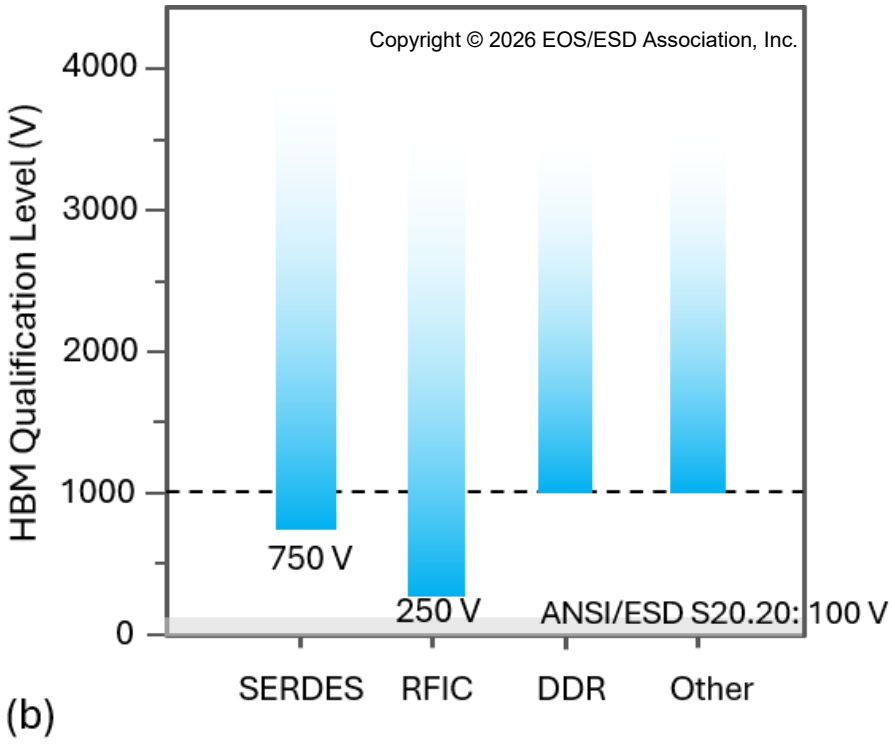


Figure 1: Current Status of (a) CDM and (b) HBM Qualification Levels

Looking forward to 2030, ESD protection levels are expected to be further lowered, particularly for CDM. SERDES products are expected to reach data rates of 448 Gb/s and may then support only 1.8 to 2.0 amperes of protection for CDM. For large packages, this translates to 75 to 100 volts. Similar but less dramatic reductions are expected for some high-performance RFICs. Exceptions for RF products include ports such as antennas, where the RF port has zero bias. In this case, as the RF frequency is increased beyond 5 GHz or so, high-pass filtering of the RF signal can protect the pin against both CDM and HBM threats. For double data rate (DDR) high-bandwidth memories, achievable CDM levels are expected to decrease with each generation. The first reduction is expected for DDR6, where the best achievable level is expected to be around 200 volts. DDR7 will bring the next reduction, going to a CDM level of 150 volts. Figure 2a shows the expected threshold levels.

As expected, HBM thresholds for leading-edge SERDES, RFICs, and DDR7 products will also decrease. The high data rates of SERDES products are expected to require a corresponding reduction in HBM thresholds to 500 volts. The same is true for high bandwidth memories. For RFICs, the reduction of HBM levels is expected to occur in more than just compound semiconductor ICs. However, zero-bias ports will continue to reach high HBM thresholds due to high-pass filtering techniques. Figure 2b shows these expected threshold levels.

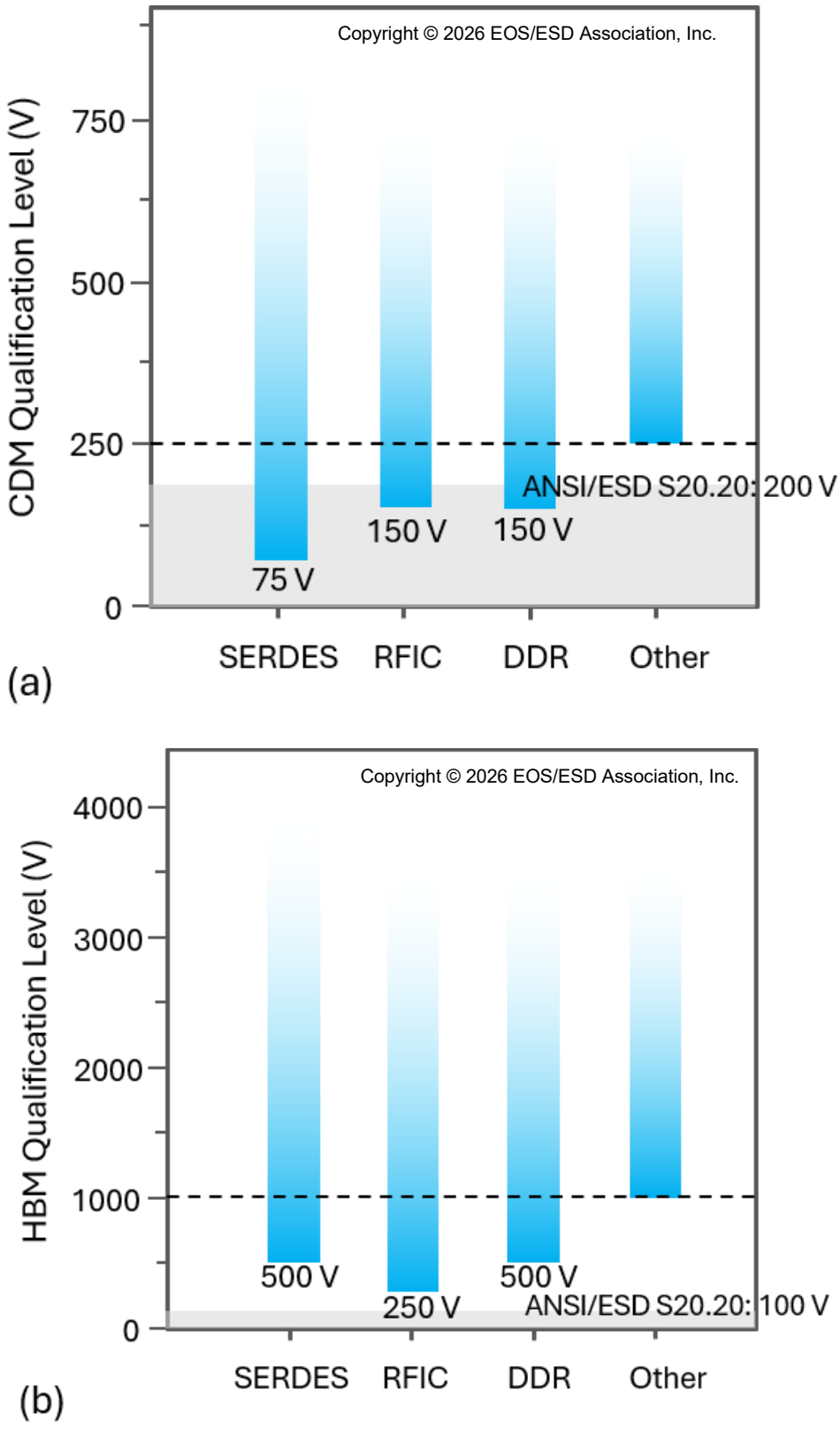


Figure 2: Projected Status of (a) CDM and (b) HBM Qualification Levels in 2030

The introduction of 2.5D and 3D integrated ICs required defining even lower CDM target levels for internal die-to-die (D2D) interfaces. Figure 3 shows the D2D interface roadmap. Scaling the interconnect pitch drives the reduction in the CDM target level for D2D interfaces. For high-density interfaces with pitches below 10 micrometers, little to no area is available to place ESD protection devices or circuits. These low CDM protection levels are often achieved only through the self-protection capability of the connected circuitry and require good communication among the fab, the outsourced semiconductor assembly and test (OSAT) provider, and the IC design team. Advanced ESD control measures such as placing ionizers and, if possible, real-time monitoring of small ESD events are needed to enable safe handling and assembly of these interfaces. Because HBM is not a risk for D2D interfaces, the HBM target level is not defined. Section 4.0 provides a detailed outlook on the technical challenges of using D2D interfaces.

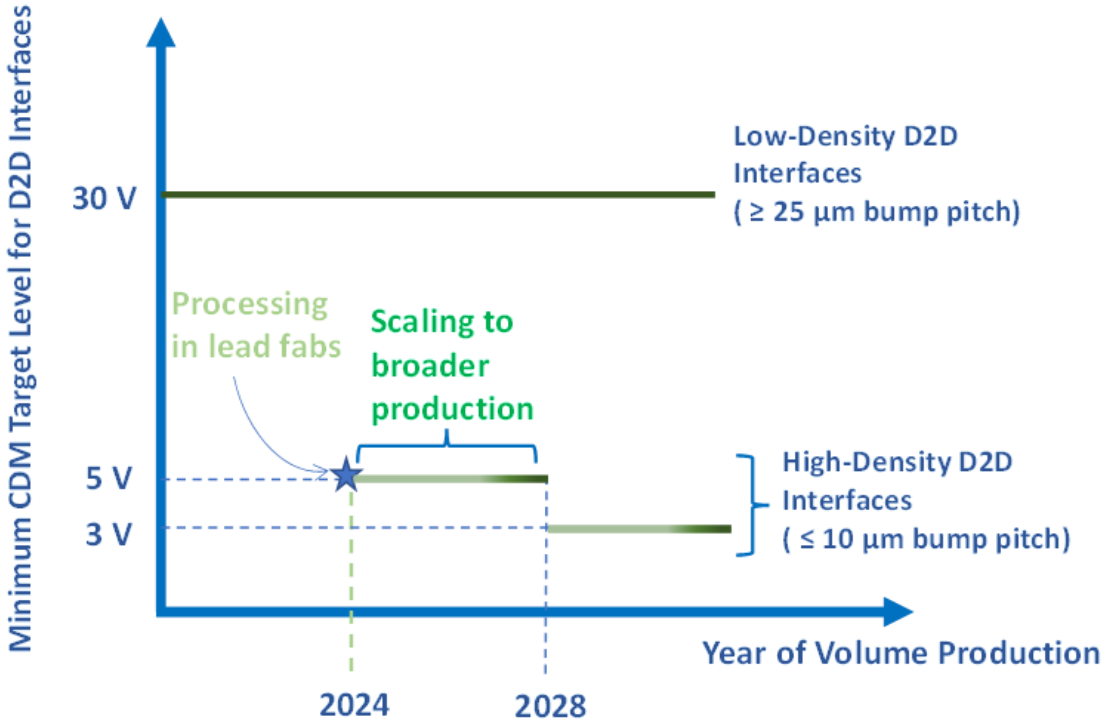


Figure 3: Roadmap of CDM Targets of Die-to-Die Interfaces [6]

2.3 No Correlation Between HBM and CDM Target Level and System Level ESD Robustness

For several years, many have believed that device-level ESD (for example, HBM) predicts or is a prerequisite for high system-level ESD robustness. This misconception has led many OEMs to impose higher HBM requirements on devices, believing it will improve their chances of passing IEC 61000-4-2 [8] or ISO 10605 system-level tests [9]. The Industry Council on ESD Target Levels White Paper 3, Parts I and II, addressed this misconception [10,11]. Figure 4 clearly shows that increasing the HBM target level does not reduce system-level failures.

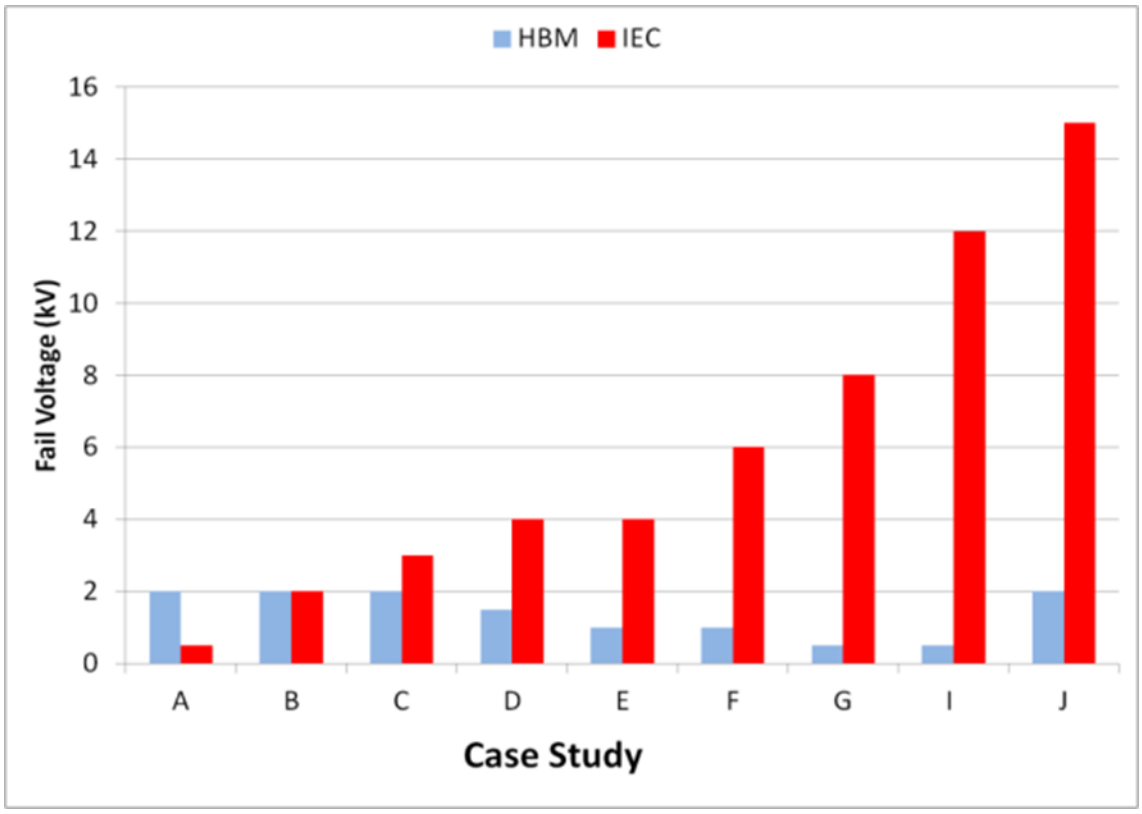


Figure 4: Comparison of IC Device Level and System Level ESD Failure Threshold of Various Systems (A-J) Showing that HBM Protection is not Related to System Level ESD Robustness [11]

Instead, as introduced in White Paper 3 Part I, a co-design approach is required. A basic version of the so-called system-efficient ESD design (SEED) has been proposed to address hard failures related to IC pins with a direct external interface. More advanced co-design approaches are needed for soft reversible failures, which are more frequently reported. These are harder to understand and overcome. These require an extension of the SEED approach to other failure mechanisms, including latch-up and electromagnetic interference (EMI) effects. White Paper 3 part II [11] from the Industry Council on ESD Target Levels discusses these challenges and approaches.

2.4 ESD Control Programs

ESD control programs have been in place for many years. One of the earliest programs supported gunpowder production. This simple program effectively kept the powder wet during manufacturing and handling. This kept the static charge low enough that the gunpowder would not ignite.

In the 1950s and 1960s, electronic devices were less sensitive to ESD events. The devices of the time could withstand most events without a problem. Even when devices failed due to ESD events, these failures made up a very small portion of overall failure rates.

In the late 1970s, with the introduction of large-scale integration (LSI), ESD became a significant problem. A group of industry experts realized this and organized the first US ESD Symposium in 1978. At the time, they exchanged technical papers and held workshops on problems and solutions. Companies also began implementing ESD control programs. Each company had its unique program and did not share the information. At that time, the need for standardized programs was not recognized.

The US Military was one of the first organizations to recognize the problems with static electricity and ESD. The first standard to address ESD process control was MIL-STD-1686, released in May

1980. This standard, along with its companion handbook, MIL-HDBK-263, was the industry's first ESD control standard. All electronics suppliers to the military were required to comply with this standard. However, most of the private sector still followed the company-developed procedures. Today, the US Military uses ANSI/ESD S20.20 for its ESD control program.

These early standards were focused on people and packaging. The controls for insulators were left mostly to the end-user, with little consideration beyond removing non-required insulators. Tools, machines, and automated equipment were not addressed, as most processes were manual. The basic instructions were to keep everything and everyone handling the devices at the same potential.

Another issue with these early ESD control programs was that the materials used to control static electricity lacked standards to qualify the materials. This led to many different types of testing, methods, and instrumentation, causing different results. In some cases, materials measured by these methods did not perform well in controlling static. In the early 1980s, a professional association, EOS/ESD Association, Inc. (ESDA), was formed to resolve material testing issues. The first standards from the ESDA were simple material tests for items such as wrist straps, work surfaces, and flooring. The standards created a way to compare one product to another. Suppliers could use the standards to improve products. For example, the simple wrist strap has changed significantly over time. What started as a simple metal bead band has evolved into a system that makes better contact with a person and, in some cases, allows for continuous monitoring. Wrist straps provide a much more reliable connection than before and last longer. The standards also provide a way to test wrist straps consistently so manufacturers can remove and replace defective ones. Before this, manufacturers used materials until the materials were physically damaged, without regard to electrical properties.

In the 1980s and 1990s, the electronics manufacturing industry shifted from each company handling all manufacturing in-house to a model that included many contract manufacturers (CMs) or electronic manufacturing suppliers. At the same time, the military and the European standard, CECC-00015:1991, did not evolve with technology or changes in manufacturing supply chains. The standards were either too restrictive or did not address all aspects of an ESD control program.

In 1995, the ESDA was tasked with replacing MIL-STD-1686 with an industry standard. The standard, ANSI/ESD S20.20-1999, replaced company-developed ESD process control programs. After the release of this standard, a third-party certification program was established to demonstrate compliance and has been successfully applied to factory certifications worldwide, as shown in Figure 5. ANSI/ESD S20.20 has been periodically updated to keep pace with device technology, emerging information about ESD failures, and improvements in ESD control technologies and measurement methods, with the latest version being ANSI/ESD S20.20-2021 [1]. In parallel, the IEC has created and periodically updated a similar control document, IEC 61340-5-1 [2], which is technically equivalent to ANSI/ESD S20.20. JEDEC has also recently released JESD625C.01, which can now also be considered technically equivalent to ANSI/ESD S20.20.

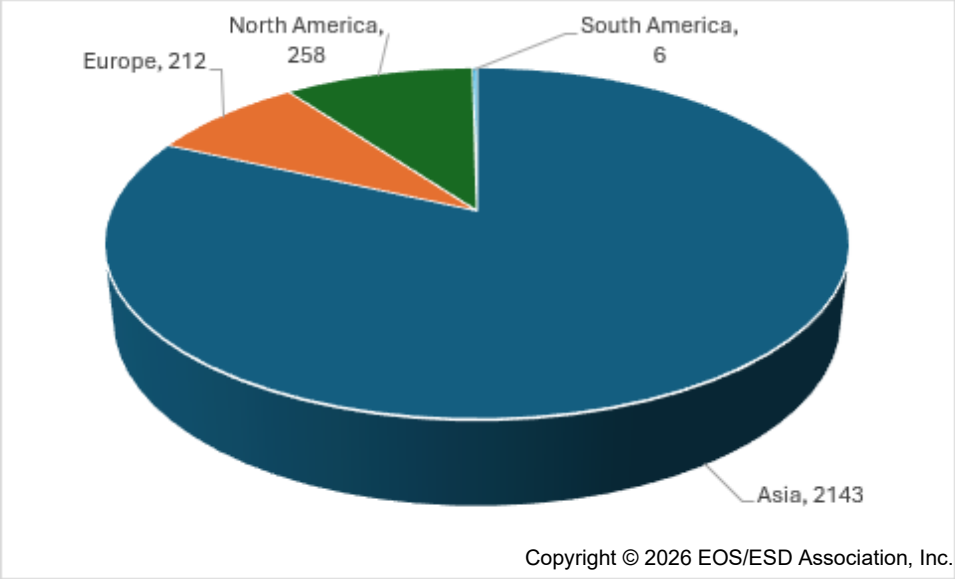


Figure 5: ANSI/ESD S20.20 Certificates Issued Through August 2026

2.5 ESD Stress in Processes

The ESD sensitivity discussed in Section 2.2 will significantly impact manufacturing process yields over the coming years. Companies must increase efforts to verify that processes can handle these devices and, where necessary, improve ESD control programs. This could include changes in the ESD control item limits, compliance verification frequency, and other ESD monitoring forms, such as ESD event detection.

The ESDA has released a standard practice on ESD process assessment. ANSI/ESD SP17.1 [12] describes a set of methodologies, techniques, and tools that can be used to characterize a process where ESD sensitive (ESDS) items are handled. The process assessment in ANSI/ESD SP17.1 covers risks from charged personnel, ungrounded conductors, charged ESDS items, and ESDS items in an electrostatic field. The basic approach is to compare parameters measured in the manufacturing process, for example, an electrostatic voltage on an ESDS item, with the limits derived from the HBM or CDM robustness of the ESDS item. This document's procedures are for use by personnel with advanced knowledge and experience in electrostatic measurements. Assessing the results from the measurements described in this document requires significant experience and knowledge of ESD physics and the manufacturing process.

2.5.1 Discharge of Personnel

It has been shown that for a person grounded by a wrist strap system, the person's resistance to ground directly correlates with the maximum voltage on the person. Tests on a person wearing a wrist strap using standard shoes on non-ESD protective flooring have shown that a total resistance to ground through a wrist strap of 4.0×10^7 ohms or less is necessary to maintain body voltage to less than 100 volts. ESDS items being handled in a manufacturing environment following ANSI/ESD S20.20 are susceptible to damage by electrostatic discharges greater than or equal to 100 volts HBM, and, therefore, the maximum body voltage of personnel handling ESDS items should be limited to below 100 volts. Testing was done by using a wrist strap with a 1-megohm resistor in the cord and adding series resistance to the wrist strap system. The resistance was placed between the end of the wrist strap cord and the ground connection. Then the person wearing the wrist strap walked on the non-ESD floor while their voltage was measured. Figure 6 shows the relationship between the body voltage of personnel wearing standard shoes on a non-ESD floor connected by a wrist strap to ground as a function of the total resistance to ground through the

wrist strap. The system resistance limit for wrist straps in ANSI/ESD S20.20 is 3.5 x 10^7 ohms, which provides approximately a 10% safety margin.

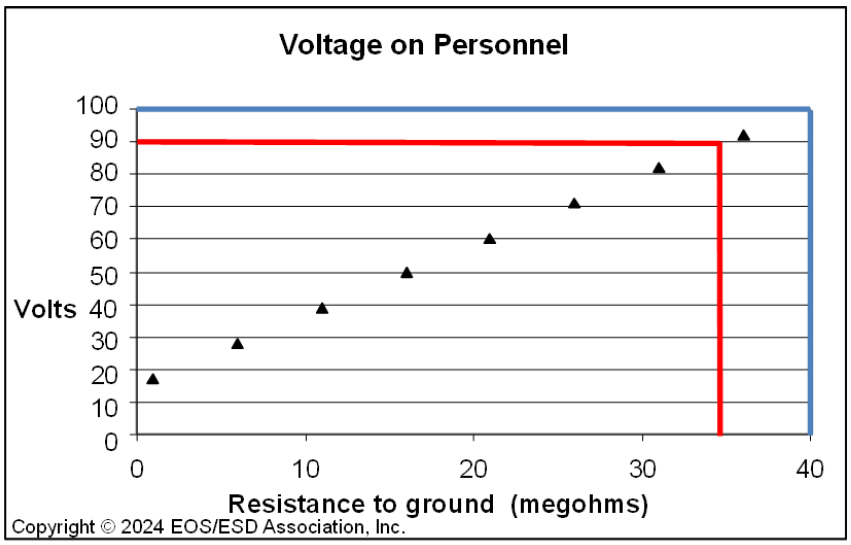


Figure 6: Relationship Between Body Voltage and Resistance to Ground

NOTE: Red: body voltage limit of 90 volts for handling ESDS when grounded with a wrist strap using a resistance to ground limit of 3.5 x 10^7 ohms as per ANSI/ESD S20.20 [1]. Blue: body voltage limit of 100 volts for handling ESDS when grounded with a wrist strap using a resistance to ground limit of 4.0 x 10^7 ohms.

The situation is more complex for an ESD control program that uses a footwear/flooring system to ground personnel. As people walk across a floor while wearing footwear designed to keep personnel grounded, it is difficult to predict the voltage on a person's body due to the constantly changing body capacitance and the continuous charging and discharging of the person.

ANSI/ESD STM97.2 [13] can be used to determine the process capability of the footwear/flooring system. Figure 7 shows an example of the information provided.

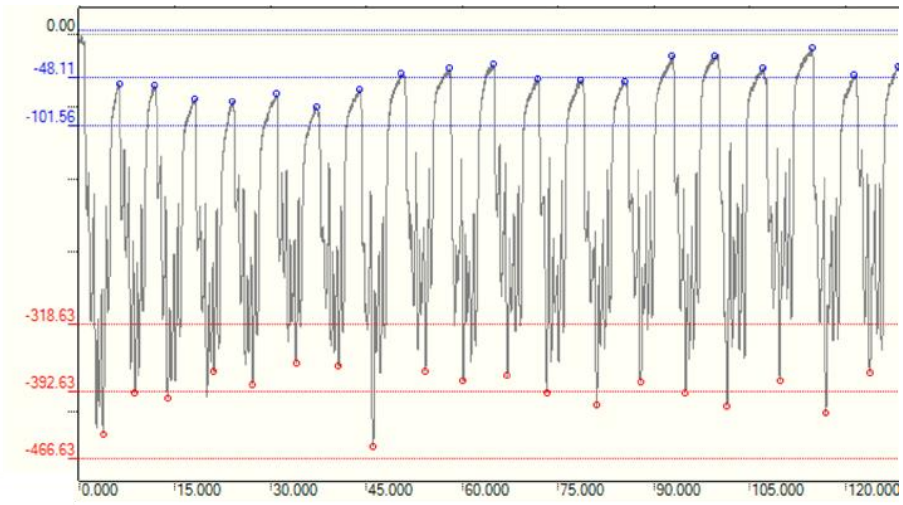


Figure 7: Determining Process Capability of a Footwear/Flooring System Using ANSI/ESD STM97.2

2.5.2 Discharge of Ungrounded Conductors

When a charged conductor comes close to or contacts an ESDS item, a discharge can occur. If the ESDS item is grounded on at least one pin, the discharge was previously correlated with the machine model. If the ESDS item is floating, the discharge scenario is best described with a CDM-like event. To minimize these discharges, ensure that all conductive surfaces that come into contact or proximity with ESD sensitive devices are grounded. If grounding conductive surfaces is not possible, take measurements to ensure moving parts remain below a threshold voltage throughout the process. In ANSI/ESD S20.20, the threshold is defined at 35 volts.

CAUTION: THIS THRESHOLD LEVEL DOES NOT TRANSLATE INTO ANY MEASURED CHARACTERIZATION WITH A MACHINE MODEL (MM) TESTER. THESE MEASUREMENTS MUST BE TAKEN WITH THE PROPER EQUIPMENT, SUCH AS A CONTACT VOLTMETER OR A NON-CONTACT VOLTMETER. MOST ELECTROSTATIC FIELD METERS USED AS VOLTMETERS CANNOT MAKE THIS MEASUREMENT.

2.5.3 Events From Charged Devices and Static (Field) Induction (CDM)

In its pure form, a CDM event occurs when a charged ESD sensitive device is grounded or when a neutral device makes sudden contact to ground in the presence of an electrostatic field. A unique characteristic of these events is the involvement of a very fast rise time event between a device pin and another conductor at a different potential. CDM is the most relevant discharge model when single ICs are handled with automated equipment or manually using hand tools with conductive contact to the ESDS item. Thus, the CDM test method may also cover more general conductor-conductor discharges, such as touching a device lead with conductive tweezers. This includes many isolated conductor discharge events. An isolated conductor has no connection to ground or any other conductor.

Effective ESD control programs ensure that the voltage on an ESDS item, whether induced by process-essential insulators through electrostatic induction or triboelectricity, stays below a safe handling limit before contacting a conductive object. As CDM thresholds are lowered, it becomes more difficult to depend on voltage control alone to provide adequate device protection. Thus, eliminating conductor-conductor contact wherever possible and using dissipative materials to avoid hard grounding is becoming more important.

2.5.4 Charged Board Events (CBE)

ICs and other ESD sensitive devices remain at risk when mounted onto printed circuit boards and other assemblies. Evidence shows that many ESD failures in circuit and system assemblies occur at the board level. These types of failures are due to charged board events (CBE). Most ESD testing and device characterization is done on standalone parts. This type of data is summarized in the HBM and CDM roadmaps.

Further, IC failure analysis data, based on knowledge of failure signatures seen in standard HBM and CDM tests, has led many to conclude that ESD failures are relatively rare compared to other electrical failures commonly classified as electrical overstress (EOS). Recent data and experience reported by several companies and laboratories now suggest that many failures previously classified as EOS may instead result from ESD failures due to CBE or cable discharge events (CDE) discussed in the next section. A charged board stores more energy than a standalone part because its capacitance is larger. The charge energy transferred in the event may be large enough to cause EOS-like failures to the devices on the board.

ANSI/ESD S20.20 does not define minimum board robustness against CBE. Consider significantly reduced maximum charging or discharge currents, accounting for the more severe discharge of a board than a single IC. For some guidance, see ANSI/ESD SP17.1 [12]. For facilities handling parts with sensitivities below those stated in ANSI/ESD S20.20, you may need more controls or tighter limits. However, in most cases, these practices and requirements should be sufficient for protecting circuit boards (PCBs). Problems do arise when specific program implementations do not fully comprehend PCBs as ESD sensitive items. In these cases, the risk of failure due to CBE may be significant. Identifying CBE as the root cause of failure can be difficult. This may require tests that

replicate CBE-induced failures and distinguish these from other possible electrical stresses. EOS/ESD Association, Inc. has developed methods for conducting CBE tests in WG 25.0 (see Section 3.2.3).

2.5.5 Cable Discharge Events (CDE)

The insulation on a communication cable (USB, Ethernet, etc.) is easily triboelectrically charged by the movement of the cable over surfaces such as desktops, floors, clothing, and work surfaces. This charging, in turn, induces a potential on the cable's conductors. When the charged cable is plugged into a system, an ESD event occurs between a cable conductor(s) and one or more of the connector pins of the system receptacle, depending on the connector design. This discharge is referred to as CDE. The resulting current pulse depends heavily on cable length, impedance, connector type, and cable quality. Industry reports indicate that CDE can damage an interface device, create a system "lock-up," or cause a system upset. CDE is generally considered a charge equalization process between the victim unit or device and a charged cable. A CDE can also occur if the victim unit (laptop, cellphone, etc.) becomes charged with respect to an uncharged cable. In the latter case, the victim unit becomes triboelectrically charged through contact with a material or a charged person. Whether the cable is charged or the victim unit is charged, the result is a discharge involving current flowing into or out of a cable. Like CBE, the root cause of damage to a device from a CDE may be misdiagnosed as coming from some other form of electrical stress. Methods for conducting tests replicating a CDE are under development (see Section 3.2.4).

3.0 TRENDS IN ELECTRICAL STRESS TESTING

Device failure from a wide variety of electrical stresses is a major contributor to yield losses in manufacturing. ESD is one category of such stresses that can cause large yield-loss events and continuous background dropout. The HBM and CDM test methods have been the main enablers in the design of ESD-robust devices and are described in more detail in Section 3.1. These methods are often described as qualification methods because of the key role in the relationship between supplier and user. Stress tests can play other important roles, such as characterization or failure replication; these are discussed in Section 3.2.

3.1 Device-Level ESD Qualification

As described previously, decreasing ESD thresholds will put more pressure on the ESD control program to maintain high yields. To know where special procedures and scrutiny are required, one must know the device's susceptibility. As pin counts increase and pin spacing decreases, evaluating device ESD thresholds has become more challenging. As a result, the HBM and CDM test methods have continued to change, and additional changes are anticipated to track increasing device complexity. Increasing test costs and time also drive changes in these methods.

ESD control programs, such as ANSI/ESD S20.20, include minimum HBM and CDM levels in their scope, defining the ESD robustness range the document covers. This suggests that devices with lower ESD robustness may need additional controls to achieve high yield. Some organizations, such as the US Military and private companies, use the HBM and CDM classification levels in ANSI/ESDA/JEDEC JS-001 [15] and ANSI/ESDA/JEDEC JS-002 [17] to add further granularity to an ESD control program. ANSI/ESD SP17.1 describes using HBM and CDM voltage and current threshold levels for process assessment. Most significantly, device users and suppliers in the electronics industry use the thresholds obtained from HBM and CDM testing as part of the larger set of technical requirements for qualifying a device. For example, JEDEC JESD47 [14] includes the requirements for HBM and CDM testing. As a result, these methods are often called qualification test methods. Unlike most other qualification tests, ESD testing and threshold assignment cannot be done by technology, family, or package. Given the role these tests play in nearly every new design, considerable effort has gone into providing reproducible, reliable, and efficient methods. This section describes details and trends for these methods.

3.1.1 Human Body Model (HBM)

In 2010, the ESDA and JEDEC HBM test methods were merged into a single document, ANSI/ESDA/JEDEC JS-001-2010. The latest release was in 2024. Since its initial release, many changes have addressed testing concerns related to new device technologies, larger device pin counts, and possible tester interactions that could affect test results.

Changes were made to minimize wear-out concerns from over-stressing by minimizing the stress combination, allowing the use of sampling methods for signal pins, and, more recently, for power pins.

Recent changes included the following items:

- Introduced an alternative decay time calculation method.
- The exposed pad has been defined as a pin and shall be stressed according to its classification. The implications of this may require new hardware on the HBM tester to support the testing.
- Stress testing on the package, die, or wafer is fully allowed.
- An annex on optional pre-HBM current spike detection equipment has been added.

A true statistical sampling scheme standard practice has been developed to reduce the overstressing of pins relative to real-world environments without compromising the threshold assessment of the product. A similar statistical approach has been used to develop random testing combinations for supplies with resistance between pins higher than 1 ohm and lower than 3 ohms to reduce test time using a two-channel simulator. The HBM user guide ESDA/JEDEC JTR001 [16] has been completely revised to include the new allowances introduced over the years and was released in 2025. The next full release will focus on harmonizing the document and a few other allowances.

3.1.2 Charged Device Model (CDM)

CDM remains the electronics industry's primary real-world ESD model for assessing ESD risk in automated IC handling and manufacturing worldwide. CDM ESD must consider the scaling of the device process – IO pin technology, scaling down of minimum device size – pin pitch achievable in test, and CDM tester metrology limitations, in consideration of the CDM roadmap direction over the next five years.

3.1.2.1 Device Thresholds

Continuing trends in integrated circuit process technology advances, increasing package size and complexity, and increasing IO performance requirements point to lower minimum charged device model withstand thresholds, especially for high-performance pins. These trends will result in a larger percentage of high-performance pins on products forecasted to be below 125 volts by 2030. These pins may make up only a small fraction of the total pins in any one package.

3.1.2.2 Package Size/Pin Pitch

Two package-related limiting factors to CDM testing are the minimum package size and pin or ball pitch (distance between pins/balls on a package type). Minimum package x-y dimensions in 2020 were on the order of 400 µm by 600 µm, and this is expected to pose a challenge to small-package testing looking out to 2030. A pin pitch of 350 µm (the minimum achievable by FI-CDM testers in 2020) will not allow testing of packages with smaller pin pitch (including bare die pad spacings) with today's pogo-style discharge pin/ground plane FICDM probe assemblies. Thus, future CDM test capability requires probe technology like automated test equipment (ATE) for those die-form products. A comprehensive technical report (TR) on testing small form factor packages (including bare die and 2.5D/3D interfaces) and at low stress levels will be published by the end of 2026. It will compile results from papers published in recent years that discuss the issues and possible solutions.

3.1.2.3 CDM Testing Methodology

Three CDM testing methods are available today. The first method, field-induced CDM testing, is used by over 90% of the electronics industry. This is widely based on the harmonized ANSI/ESDA/JEDEC JS-002, published in 2015 and updated in 2025 [17], and its associated user guide published in 2022 [18]. This harmonization has helped the industry standardize on a single field induced CDM test platform that covers most of the industry's needs, but it is still limited. These limitations include the minimum device size and pin pitch physical limitations of the CDM test equipment (which can lead to multiple pin discharges for very small pitches), as well as the environmental variation of the discharge peak currents caused by the air discharge, which is dependent on device size, charge voltage, and relative humidity. The continued reduction in minimum CDM pin thresholds described limits the use of field induced CDM for many devices due to the increased variation in the discharge waveform at low voltage levels.

To overcome the limitations of field-induced CDM, two alternative methods have been developed. Early trials have shown that an alternative CDM testing method, low impedance contact CDM (LICCDM), achieves a more accurate discharge pulse, independent of humidity and the varying characteristics of the discharge spark in a field induced CDM event. Research on approximating the impedance of the field-induced discharge spark with a discharge impedance in the contact CDM metrology chain (through the transmission line and relay switching) has shown significant promise for providing repeatable, reproducible discharge waveforms below 50 volts with no humidity dependence. A standard practice [19] was published in 2018, describing this new test method. This method is expected to yield more accurate CDM testing at lower voltage levels for devices that need it. This contact approach also eliminates some of the challenges of testing smaller packages/pin pitches by allowing a sharper pogo tip to be used.

A second alternative CDM test method (capacitively coupled TLP (CC-TLP)), which also uses a contact approach, has been investigated. The standard practice [20], published in 2022, describes this test method. CC-TLP systems have been used much longer than LICCDM and have shown a good correlation with CDM results in many studies. The limitation of being unable to completely match the field induced CDM discharge waveform due to the higher source impedance can be compensated by a shorter pulse width. Thus, CC-TLP is also being considered as a possible wafer-level characterization technique for die-to-die interfaces that would provide important information on protection structures before packaging and could serve as a solid figure of merit at the wafer level to compare the ESD robustness of various protection structures. This is also a potential solution for characterizing chiplets used to enable more complex package systems.

Currently, the joint CDM WG is working on a round-robin (RR) to elevate the standard practices for CC-TLP and LI-CCDM to standard test methods (STM). The first RR study on CC-TLP using a real device will be published at the 2026 EOS/ESD Symposium, showing a small variation of less than 6.5% within the failure threshold, but still presenting two different groups of results. The RR also highlighted some criticisms in the standard practice related to system calibration, which should be addressed before moving it to an STM. LI-CCDM RR has focused on system calibration and verification, and the plan is to use the same parts as those used for the CC-TLP RR within a small group of laboratories. For both methodologies, the joint CDM WG plans to stress devices with a low voltage threshold.

Although these methods cannot match 100% of FICDM results, these will be the only solutions for testing at voltages below 100 volts and small form-factor packages (including die), without replacing the well-established FICDM methodology.

3.2 Characterization and Replication Methods

Stress tests can play other important roles, such as characterization or failure replication. Characterization using TLP gives ESD protection designers an early indication of the electrical response to ESD-like pulses, informing the ultimate protection strategy. Electrical stress tests can also support failure analysis and root-cause verification and provide comparative evaluations of corrective actions. These can be described as stress replication tests. The tests include transient latch-up (TLU), variations of CBE and CDE stresses, and other unintended electrical stresses. This section discusses these non-qualification methods in more detail. In the future, some stress

methods may become widespread and reliable enough to evolve into acceptance or compliance tests. Currently, none of the methods are in that category.

3.2.1 Transmission Line Pulse (TLP) Characterization

The TLP method is the de facto standard method for ESD characterization of standalone devices/components and pins of ICs. ANSI/ESD STM5.5.1 [21], fully revised in 2022, is the basis for this work and covers transmission line-based quasi-static characterization with pulse widths in the range of single nanoseconds to several microseconds and appropriate rise times. The User and Application Guide, ESD TR5.5-04-23 [22], provides additional information on the practical use of TLP systems and is updated regularly.

Technical report ESD TR5.5-05-20 [23], released in 2020, addresses the use of TLP systems for non-quasi-static analysis. The working group has started developing a standard practice that advises on best-known measurement practices to support analysis of the device response to fast transients, such as during CDM or system-level stressing.

With the increased use of automated TLP systems, collecting enough data for statistical analysis is now feasible. Therefore, the working group started compiling a technical report on using TLP to statistically characterize device behavior under ESD conditions. Examples include methods to characterize the distribution of parameters such as trigger voltage, failure current, and oxide breakdown voltage.

The increased use of TLP and the use of the results to develop ESD models for the SEED method [10,11] suggest the need for a standard definition for characterization and reporting in these applications. This may lead to a new technical report or an updated user and application guide. Finally, the working group may investigate extending the pulse-width and rise-time ranges of TLP methods.

3.2.2 Transient Latch-Up (TLU) Replication

Integrated circuits can contain latch-up sensitive structures (such as parasitic thyristors), which can cause reliability issues during operation. For this reason, most semiconductor devices must be qualified to a respective latch-up sensitivity. JEDEC JESD78 [24] is the most widely used latch-up qualification standard. However, this test has a slow rise time and long trigger pulse, which may not cover latch-up events sensitive to transient triggering. It is well known that fast transients, such as ESD, can trigger latch-up more efficiently.

Per the "static" JEDEC JESD78 latch-up standard, the ESDA WG 5.4 (Transient Latch-up) defines transient latch-up as a state in which a low-impedance path resulting from a transient overstress that triggers a parasitic thyristor structure or bipolar structure or combinations of both persists at least temporarily after removal or cessation of the triggering condition. The rise time of the transient overstress causing TLU is faster than 5 µs.

In 2014, to address industry needs, ESDA WG 5.4 started a new standard practice on TLU, which defines a universal TLU methodology that can be used for replicating transient effects seen in the field. The proposed TLU trigger pulses and the setup can be modified to match a specific application's requirements and constraints. The methodology can be applied to various applications, from simple test structures and discrete semiconductor devices to complex integrated circuits, standalone devices, or systems. The proposed methodology can reproduce all TLU events discussed in ESD TR5.4-04-13 [25]. An important building block of the document is the verification methodology of the TLU setup, which ensures correct pulse delivery to the device under test and a sufficiently fast response from the power supply. ESDA WG 5.4 released ANSI/ESD SP5.4.1 in 2017 [26] and reaffirmed the document in 2022.

It must be emphasized that the TLU test methodology proposed in the standard practice is not intended to be used as a qualification methodology, in contrast to the static latch-up test JEDEC JESD78, a mandatory device qualification test. The TLU methodology can be applied to pins that might be endangered by fast transients in the field to replicate certain types of electrical overstress. It intends to cooperate closely with the JEDEC JESD78 working group, as both standardization committees face similar technical challenges. While the JESD78 standard does mention the TLU

documents, it makes no further assessments. Therefore, a close link between the JEDEC JESD78 WG and ESDA WG 5.4 is planned.

3.2.3 Charged-Board Event (CBE) Replication

The ESDA has published a technical report, ESD TR25.0-01-16, giving general information about CBE phenomena [27]. The ESDA has also published a second technical report, ESD TR25.0-02-23, that guides the industry in replicating CBE threats [28]. It includes examples of how to set up a CBE test bench, conduct testing, and report results. The document also explains how to estimate CBE stress levels based on calculated and simulated data. ESD threats due to CBE are case-specific, and the technical report does not contain acceptance or target levels for CBE stress. Instead, it instructs how the user can specify the target level and estimate ESD risks based on the observed discharge waveforms in the process area and on the test bench.

3.2.4 Cable Discharge Events (CDE) Replication

ESDA WG 14 (System Level ESD) has collected data on real-world CDE events, gathering relevant information from case studies, publications, and industry inputs to create a well-defined test method. This test method is intended to guide the industry in enabling reproducible testing against CDE threats and to help determine the CDE immunity of a system, such as a laptop or handheld device (phones/cameras, etc.). While gathering this data, it became apparent that cable discharge events may be only one of many "events" that can cause operational or hardware failures on individual devices.

Cable discharge events can occur when a charged cable discharges into a system, or when a cable attached to another item (which adds additional capacitance) discharges into a system. This discharge can occur between the cable shell and the system connector, or directly between the cable pins and the system connector pins. This direct discharge between the cable pins and the system connector would be a "direct pin discharge". However, this test is not recommended in widely used system level test methods.

The number of variations in discharge events has made it difficult to establish a single representative waveform for a test method. The WG has written multiple articles on CDE with an emphasis on educating the industry about CDE, but also as a way of gathering information from sources outside of the committee

3.2.5 Replication of Other Electrical Stresses

Apart from electrostatic discharge, other events can cause devices to fail. These events are categorized as electrical overstress (EOS) [29]. An industry-wide initiative aims to reduce these kinds of failures. Given the broad scope of EOS, the main challenge is to reproduce the wide range of possible stresses systematically. WG 23 collected data and industry practices for producing these stresses based on waveform characteristics and other environmental factors and published it in a technical report [30].

4.0 TECHNOLOGY OUTLOOK

This section focuses on the drivers of technical advances in the semiconductor industry towards 2030. CMOS scaling continues, and packaging will advance significantly. Another driver is the broad use of III/V compound semiconductors, particularly in energy conversion and communication. This includes applying photonic technologies to enable the huge data bandwidths required by digital society. In this edition of the roadmap, we also added new topics such as system level ESD and latch-up to broaden the outlook beyond IC-focused ESD design challenges.

4.1 Advanced Logic Technology

This sub-section provides an in-depth exploration of advanced logic technology innovations and the associated ESD challenges. It covers the evolution of device architectures, the implications of backside power delivery networks (BS-PDN), advancements in back-end-of-line (BEOL) interconnect scaling, and the opportunities and challenges these developments present for ESD protection.

4.1.1 Evolution of Device Architectures: Transition to GAA and CFET

The evolution from FinFET to gate-all-around (GAA) architecture (Figure 8) marks a significant shift in device design, driven primarily by the need for improved electrostatic control and vertical scaling to increase drive current per layout area. In GAA structures, the gate fully surrounds the channel, enhancing control over short-channel effects. However, this architectural change also reduces the effective silicon cross-sectional area available for current conduction, leading to higher current densities under ESD stress conditions. As scaling progresses further, complementary FET (CFET) technology introduces vertical stacking of n-type and p-type devices, enabling even greater density and performance improvements. While this approach maximizes footprint efficiency, it further constrains the available device volume and current paths. The reduced physical dimensions significantly limit the structure's robustness under high transient currents and introduce new ESD reliability challenges. Smaller active silicon regions and higher current densities increase the risk of localized heating and device failure, making robust ESD protection design more critical than ever. The reduced silicon volume leads to lower ESD robustness, making devices more susceptible to damage under ESD stress.

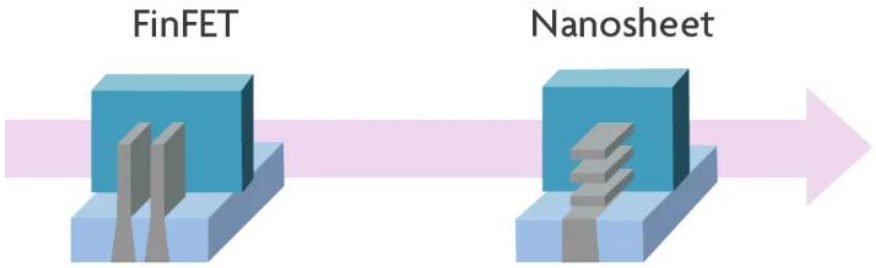


Figure 8: Comparison of FinFET and Nanosheet Device Architecture [31]

In CFET architectures (Figure 9), n-type and p-type transistors are vertically stacked rather than placed side by side, as in traditional planar or FinFET technologies. While this vertical integration greatly improves layout density and performance, it fundamentally alters the device topology. It eliminates the formation of lateral junctions that have historically enabled diode-based ESD protection elements. The absence of lateral diodes in CFETs creates a significant gap in conventional ESD protection strategies. Traditional diode clamps rely on lateral current paths between diffusion regions, which are no longer available in this vertically stacked configuration. As a result, designers must explore alternative device concepts and protection schemes that are compatible with the vertical structure while still providing efficient ESD discharge paths. Together, these factors highlight the need to rethink ESD protection methodologies in CFET technologies. New solutions must address both the lack of traditional diode elements and the heightened susceptibility to self-heating, ensuring reliable operation under increasingly constrained physical conditions.

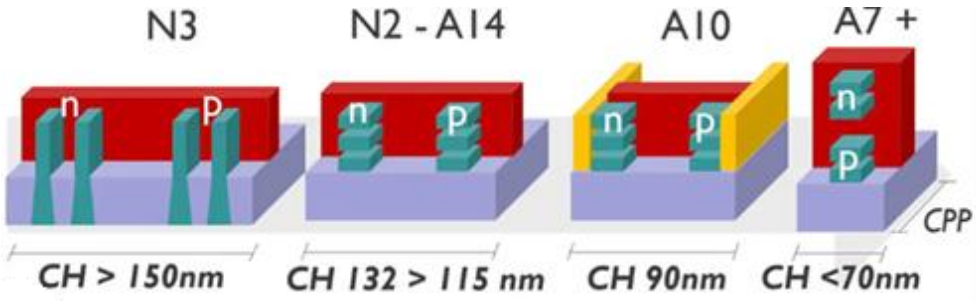


Figure 9: Evolution of Device Architectures From FinFET (N3) to CFET (N2 to A7+) [31]

4.1.2. Backside Power Delivery Network (BS-PDN) and Associated ESD Challenges

The introduction of BS-PDN architectures represents a fundamental departure from conventional bulk silicon designs, particularly by removing the thick silicon substrate traditionally used for lateral current spreading during ESD events. This structural modification significantly alters the ESD current flow paths, constraining these to more limited geometries and thereby reducing the effectiveness of natural current distribution mechanisms present in earlier technologies. In addition, adopting ultra-thin silicon layers with backside vias further restricts the available conduction volume. The reduced silicon thickness limits vertical current spreading, resulting in elevated current densities and enhanced self-heating under ESD stress (Figure 10). Concurrently, the elimination of shallow trench isolation (STI)-based diodes removes a critical front-end-of-line (FEOL) protection element, further complicating the implementation of conventional ESD protection schemes. The substantial reduction in substrate thickness also leads to a dramatic decrease in thermal mass. This diminishes the device's ability to absorb and dissipate transient thermal energy, causing a pronounced degradation in the second breakdown current, It2. As a result, devices become significantly more susceptible to thermal runaway and catastrophic failure during high-current ESD events.

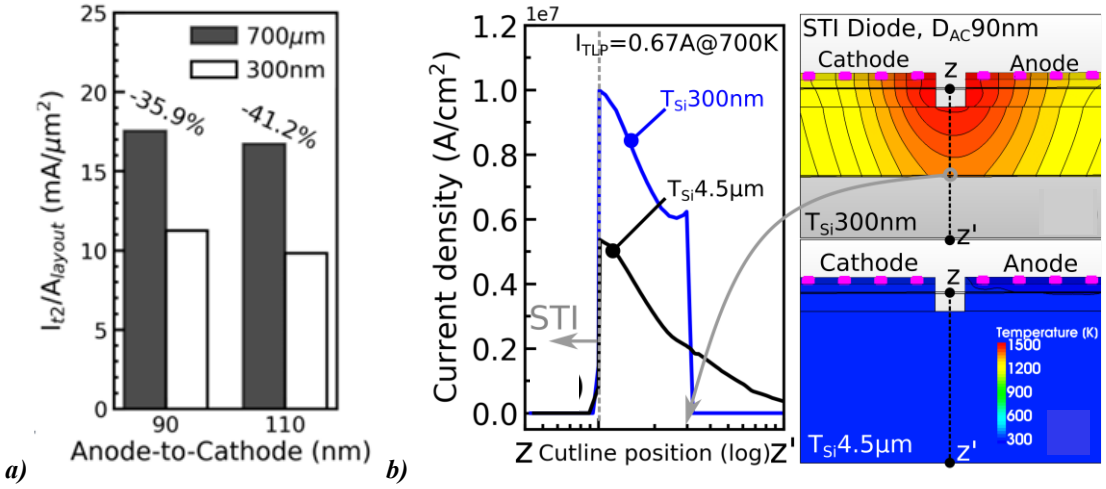


Figure 10: Impact of BS-PDN on ESD Performance

NOTE: a) Comparison of 100 ns TLP failure level of STI diodes with two Anode-to-Cathode spacing and Si thicknesses of 700 µm and 300 nm, b) TCAD simulation of the current density in a STI diode under 0.67 A 100 ns TLP stress for Si thicknesses T_i of 300 nm and 4.5 µm.

On the positive side, backside power delivery architectures introduce several inherent advantages for ESD robustness. The use of backside routing enables significantly shorter and more direct metal connections between the I/O pad and the power rails (VDD/VSS). This reduction in current path length directly lowers the effective series resistance encountered during an ESD event, thereby improving the efficiency of current discharge and reducing voltage overstress across sensitive front-end devices. As a result, faster and more uniform current spreading can be achieved, which is critical for mitigating localized electrical overstress during high-current transients. In addition, incorporating thick backside metal layers substantially improves current-handling capability compared to highly scaled frontside BEOL interconnects. These backside metals exhibit much lower sheet resistance, enabling them to sustain large ESD currents with reduced Joule heating. This enhanced conductivity is particularly beneficial under ESD stress conditions, where the ability to transport high transient currents without excessive resistive heating is essential to maintain device integrity and prevent premature failure. Furthermore, implementing backside vias introduces a distributed vertical current-injection mechanism that is highly advantageous for ESD protection. Unlike traditional planar current flow, these vertical pathways allow ESD current to be injected and dissipated more uniformly across the device structure. This helps alleviate current crowding and mitigates the formation of localized thermal hotspots, which are especially problematic in ultra-thin silicon substrates. Consequently, backside via networks can play a critical role in improving both the electrical and thermal robustness of advanced technologies under ESD stress.

4.1.3. Advanced BEOL Materials and Implications for ESD Reliability

Continued scaling of CMOS technologies has driven exploration of alternative BEOL interconnect materials, with ruthenium (Ru) emerging as a strong candidate to replace conventional copper (Cu). From an ESD perspective, Ru offers several advantages (Figure 11), including improved electromigration resistance and enhanced thermal stability. The superior resistance to electromigration is particularly important under high-current ESD stress conditions, where localized current crowding can accelerate material degradation. Additionally, Ru's higher thermal robustness can help sustain transient thermal excursions during ESD events, thereby potentially improving interconnect reliability. Another key advantage of Ru is its reduced reliance on thick diffusion barrier layers, owing to its inherently lower diffusion characteristics than Cu. This not only simplifies process integration but also allows for more compact interconnect geometries, which can indirectly influence ESD performance by modifying parasitic resistances and thermal dissipation pathways. Furthermore, Ru demonstrates improved compatibility with low-k dielectric materials, reducing diffusion-induced degradation and stress-related reliability concerns. However, from an ESD standpoint, the interaction between Ru interconnects and surrounding dielectric materials must be carefully characterized to ensure robust performance under high transient stress.

Feature	Copper (Cu)	Ruthenium (Ru)
Electromigration Resistance	Moderate resistance	**Superior resistance** to electromigration, reducing reliability concerns
Thermal Stability	Good thermal stability, but may degrade at high temperatures	**Better thermal stability**, suitable for advanced nodes
Barrier Layer Requirements	Requires barrier layers (e.g., Ta, TaN) to prevent diffusion into Si	Often needs less robust barrier layers due to **better diffusion properties**
Performance in Low-k Dielectrics	Compatible, but can create reliability issues due to diffusion and stress	Potentially **better performance with low-k dielectrics** due to lower diffusion rates
Mechanical Properties	Relatively ductile, but can suffer from stress-induced voiding	**Dense and strong**, thus may reduce mechanical stress and voiding risks

Figure 11: Comparison of Material Properties of Copper and Ruthenium

Alongside material innovations, air-gap structures have been introduced in BEOL stacks to reduce parasitic capacitance and improve signal performance. These structures lower interconnect capacitance, enabling faster switching speeds and reduced power consumption (Figure 12). From

an ESD perspective, the reduced dielectric constant environment and improved thermal isolation can influence the distribution of ESD-induced heat, potentially mitigating lateral thermal coupling between adjacent interconnects. However, these benefits must be balanced against the altered thermal conduction pathways inherent to air-gap integration. Despite their advantages, air-gap structures introduce significant challenges for ESD robustness. The mechanical fragility of air-gap dielectrics makes them particularly susceptible to damage under high-current ESD pulses, where rapid thermal expansion and localized heating can induce structural failure. Moreover, increased process complexity raises the likelihood of defects that may act as weak points during ESD stress. Ensuring mechanical integrity under repetitive thermal cycling and packaging-induced stress further complicates their adoption in ESD-sensitive designs.

Consequently, advanced BEOL materials and structures, including Ru interconnects and air-gap dielectrics, require comprehensive validation under ESD stress conditions. Their impact on key ESD performance metrics, such as the second breakdown current (It2) and the normalized It2-to-capacitance ratio (It2/C), must be thoroughly assessed. While preliminary considerations suggest that air-gap structures may improve It2/C by reducing parasitic loading, systematic experimental and modeling studies are essential to confirm these effects and establish reliable ESD design guidelines for next-generation technologies.

Aspect	Benefits	Challenges
Parasitic Capacitance	Reduced capacitance leads to faster signal speeds and lower power consumption.	**Requires precise design** to maximize effectiveness across various configurations.
Performance Improvement	Enhances overall circuit performance, especially in high-speed applications.	Not all designs will benefit equally; performance can be design-specific.
Thermal Management	Better heat dissipation due to air's insulating properties, minimizing thermal coupling.	**Mechanical stability** under thermal cycling and packaging stress can be problematic.
Mechanical Stability	Lighter structures potentially enhance thermal management and reduce stress.	Maintaining structural integrity under **thermal and mechanical stress** can be challenging.
Process Complexity	May allow for innovative designs that optimize material use and performance.	Increased processing steps **complicate manufacturing** and can lead to **defects**.
ESD	**It2/C expected to increase**	**?**

Figure 12: Benefits and Challenges When Introducing Ruthenium in the BEOL

4.1.4. Summary - Not Only ESD Challenges but Also New Opportunities

Despite these challenges, the shifting technological landscape opens new opportunities for ESD innovation. As the role of FEOL diode-based protection diminishes, the industry is clearly shifting toward BEOL-dominated or BEOL-independent ESD protection strategies, including the resurgence and adaptation of GGNMOS- and GPPMOS-like devices. Furthermore, integrating backside routing in BS-PDN architectures provides a potential platform for novel backside-integrated ESD solutions. Collectively, these approaches represent promising directions to restore ESD robustness in future technologies, but they require careful co-optimization of device physics, materials, and layout to address the unique constraints of highly scaled and vertically integrated systems.

4.2 Sub-10 nm Technologies for Automotive Applications

It is predicted that the value of ICs in the car will increase at a compounded annual growth rate of ~7% out to 2030. The value of ICs increases even more in electrified vehicles. Four major trends drive this growth in semiconductor content in vehicles: electrification, autonomous driving, connectivity, and shared mobility. Besides efficient power conversion, next-generation cars will need much more computational power, enabled by highly scaled CMOS technologies.

The semiconductor industry has long-term experience using highly scaled technologies like FinFET for consumer electronic applications and products. A strong ecosystem of semiconductor foundries,

IP block providers, and IC manufacturers has been established and supports the use and further scaling of these technologies. In the automotive industry, autonomous driving and connectivity, in particular, can only be enabled by these advanced technologies. Typical applications include advanced driver-assistance systems (ADAS), microcontrollers, and microprocessors.

The high-reliability requirements of automotive applications conflict with some of the physical limitations of highly scaled technologies. This also opens new challenges for ESD and latch-up protection design because consumer-grade protection solutions must be adapted to the higher requirements of automotive applications. This can cause some designs to fail to meet higher automotive reliability requirements. Data in White Papers 1 and 2 [4, 5] of the Industry Council on ESD Target Levels, advances in ESD control, and consumer market experience have led the Automotive Electronics Council (AEC) to re-evaluate ESD target levels. For high-speed pins and sub-28 nm technologies, the same levels as in the consumer market are adopted, and a reduction of the ESD target level has been added in AEC Q100 Rev. J [7], along with an associated expectation of improved ESD control throughout the handling and assembly of such components as, for example, described in ANSI/ESD S20.20. The same counts for latch-up design and testing, where much lower supply voltages and currents and high-temperature profiles bring additional challenges.

4.3 Advanced BCD Technology Trends

Bipolar-CMOS-DMOS (BCD) technologies have grown rapidly in recent years. Several key factors are driving this innovation path, such as the increasing diffusion of electric vehicles (EVs) and hybrid electric vehicles (HEVs) [32], the rapid spread of smart devices and IoT applications, and the strong push for energy-efficient solutions. These trends in applications are reflected in a continuous advancement in process technology, which is characterized by several factors:

- Improved power density and reduced power consumption, which is addressed with innovative and customized MOS architectures.
- Higher digital complexity and larger embedded non-volatile memories, requiring the adoption of advanced lithography nodes (40 nm and beyond).
- A strong focus on higher operating voltage ranges (above 100 volts) to implement dedicated power management integrated circuits (PMICs) for automotive and industrial fields.
- The development of innovative packaging technologies to allow system-in-package integration, combining BCD integrated circuits with large power transistors (for example, SiC or GaN power MOS) and passive elements (capacitors and/or inductors).

Each trend brings different ESD challenges. The innovative high-voltage and high-power transistors recently developed are characterized by the use of custom solutions (for example, poly and/or metal field plates, stepped oxides, mixing of different isolation strategies, etc.), which makes these transistors potentially more prone to snapback effects, thus limiting the ESD window. Moreover, the tight control of gate parasitic capacitance needed to achieve high-efficiency designs makes implementing ESD active clamps more complex.

Increased digital complexity and the use, even in advanced BCD nodes, of multi-domain architectures that mix digital and precise low-voltage analog blocks will likely impact the CDM robustness of future BCD ICs, potentially reducing the reachable CDM target levels.

New applications in the high-voltage operating range above 100 volts will require careful design of dedicated CDM protection, as the ESD diodes in this regime are strongly impacted by physical effects such as the forward recovery effect, which makes these intrinsically slow and therefore more exposed to voltage overshoot in the sub-ns time scale.

Finally, the evolution of system-in-package solutions will require close control of inner nodes, especially when large power transistors are used. These power MOS may have large parasitic capacitance, which may therefore pose a threat to the driver IC, usually designed in BCD technology. The definition and characterization of the correct ESD robustness level of these internal nodes, needed to implement an effective and at the same time robust application, is therefore going to be a very critical factor.

4.4 Heterogeneous Integration and Advanced Packaging

Heterogeneous integration is the process of designing the functionality of a system onto separate dies that may come from different technology nodes and even materials and then connecting these in a single package. The individual dies in such systems are also known as chiplets. Both lateral connectivity (2.5D IC stack) and vertical connectivity (3D IC stack) are used (see Figure 13). Advanced packaging refers to technologies that enable heterogeneous integration and combine approaches to optimize cost, performance, power, and size in ICs interconnection. It also includes supporting elements for each other and the system, including flip-chip, wafer, panel-level packaging, and interposers with and without through-silicon vias (TSV) [33]. TSV establishes the electrical connection from the bottom to the front side of a die.

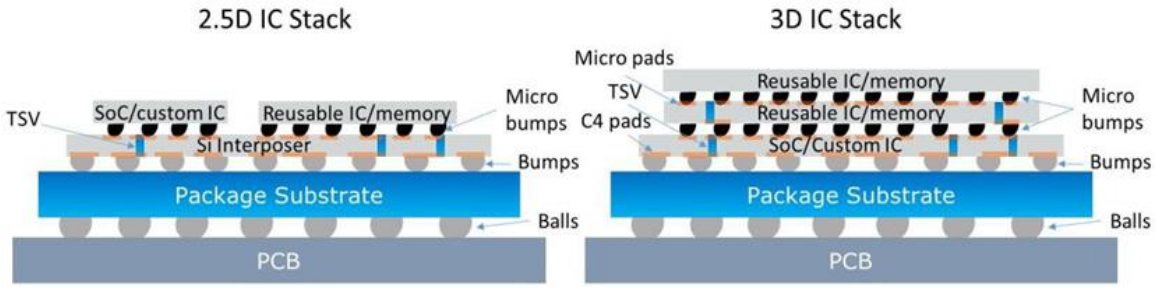


Figure 13: 2.5D Stack (left) and 3D Stack (right) ICs

The ESD challenges associated with these advances in packaging technology are directly related to shrinking technology nodes and the increasing number of microbumps or hybrid bonds on chiplets. By 2030 and beyond, minimum pitches for hybrid bonds are expected to be 10 µm or less [6], leaving little real estate for ESD protection circuits. This is driven by the need for increased bandwidth and signal speed of high-speed SERDES applications. Figure 14 (from [7]) shows the relationship between bandwidth density, signal speed, and bump pitch.

Generation Number →		1	2	3	4	5	6	7	8
Raw Areal Bandwidth Density (GBps/mm^2)		125	250	500	1000	2000	8000	32000	200000
Package Technology	Minimum Bump Pitch (µm)	40	30	20	15	10	5	2.5	1
	Areal Escape Density (IO/mm^2)	625	1111	2500	4444	10000	40000	160000	1000000
Signaling Speed (Gbps)		1.6	1.8	1.6	1.8	1.6	1.6	1.6	1.6

Figure 14: Physical IO Scaling Roadmap for 3D Architectures that Use Both Solder and Hybrid Interconnects

The increased signal speed required for these advanced applications and the reduction of bump pitch will significantly impact the level of ESD protection that can be placed on each microbump or

hybrid bond. In addition, both the supply and breakdown voltages of the advanced nodes of technology are decreasing. The typical breakdown voltage for the 2-nm transistor is around 3 volts. This reduction in breakdown voltage is part of the reason for the reduction in CDM targets (see Figure 1), since the expectation is that little to no explicit ESD control circuitry can be implemented. With a hybrid bond pitch of 10 µm or less, there is very limited space for even small ESD diodes. For these interfaces, whatever ESD withstand protection may need to be provided by "ESD hardening" design practices. This refers to applying appropriate circuit layout practices to allow the circuit to withstand the current transients associated with the expected CDM threats.

Another aspect of the ESD roadmap for heterogeneous integration and advanced packaging is the miniaturization of the substrate or interposer technology. The expectation is that by 2030 and beyond, a 1-µm line and space (L/S) will be in use (see Figure 15). In addition, there will be increased passive device integration into substrates. While this will increase the ESD sensitivity of the substrates themselves, the largest impact may be the threats to the chiplets being stacked. With more passive devices such as capacitors and inductors, the substrate may become a greater ESD aggressor in the packaging assembly process.

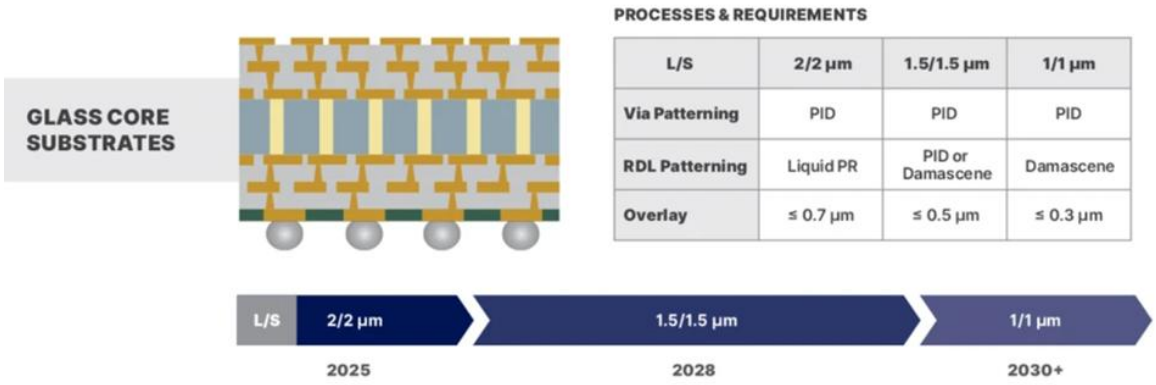


Figure 15: Industry Roadmap for Transition of Substrates from Organic to Glass and Path to 1 µm L/S

Assembly facility ESD process control capability is a final consideration for advanced packaging manufacturing. With a CDM target level capability of 3 volts to 5 volts capability for 2030 and beyond, the portion of the assembly process that handles these very sensitive components will require enhanced ESD controls. A thorough process assessment of the ESD control capability of the facility will need to be completed to verify that the facility can handle these extremely sensitive ESD parts. ANSI/ESD SP17.1 provides the framework for such an assessment.

4.5 Gallium Nitride for Power and RF Applications

The acceleration of gallium nitride (GaN) technology over the last two decades continues to exceed predictions. The applications driving this technology are wireless communication and power conversion. These are also key to energy conversion in electric vehicles. As GaN technologies mature, ESD solutions that enable large-scale manufacturing will become increasingly important. State-of-the-art GaN technology is built on Si substrates, leveraging the mature manufacturing infrastructure in silicon fabs. These state-of-the-art technologies will also enable the design and manufacture of GaN ICs that meet commonly used ESD target levels. This will also require designing and developing ESD protection circuits for GaN ICs.

Different challenges lie in the use of discrete GaN components. In a 2021 industry survey [34], ten GaN semiconductor suppliers provided ESD ratings for selected components, including RF and power transistors. The ESD ratings included several parts with very sensitive ESD ratings of Class 1a (250 volts < 500 volts HBM) and some with high ESD ratings (> 2 kilovolts HBM). This highlights the challenges in meeting safe manufacturing levels for discrete GaN transistors. The GaN devices

can withstand high voltage but have little avalanche current robustness. Discrete (non-integrated) GaN FETs have weak, exposed gates and no ESD capability [35, 36], causing erratic system behavior and device failures. Monolithic integration of GaN drivers [37] and the multi-chip module integration of silicon drivers with GaN FETs in a single package have the opportunity for much higher final product ESD robustness.

4.6 Photonics

Silicon photonics technologies (SPT) are widely used for high-bandwidth signal transmission between chips. Emerging architectures such as co-packaged optics (CPO) and optical I/O aim to further shorten electrical paths through highly integrated assembly, enabling even higher bandwidth delivery with improved energy efficiency (measured in pJ/bit) and reduced capital expenditure (in $/Gbps) compared to traditional pluggable optics, as shown in Figure 16 [38].

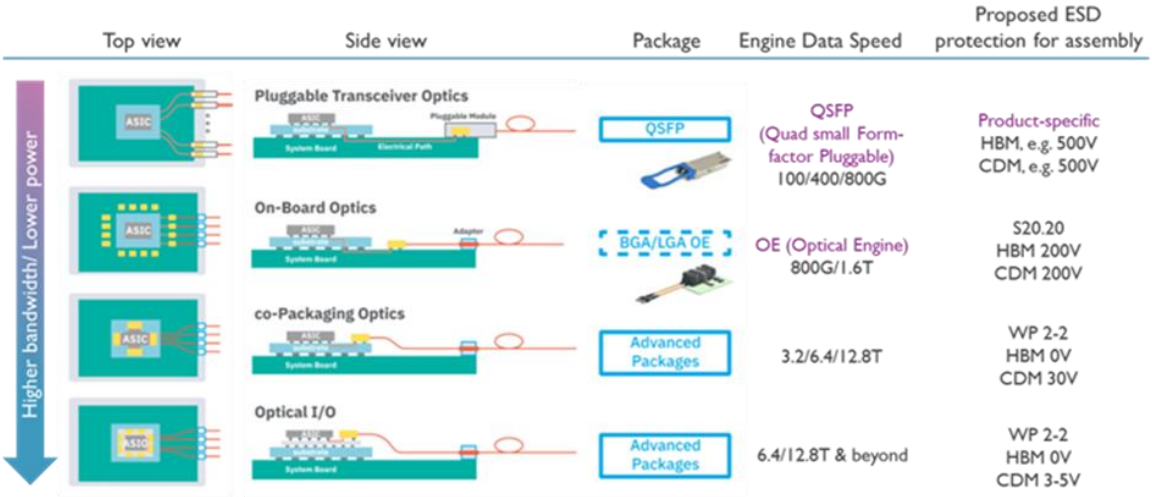


Figure 16: The Evolution of Optics Integration [38]

In these advanced architectures (based on 2.5D and 3D heterogeneous packaging), the key photonic components (lasers, modulators, photodetectors, and waveguides) are co-integrated with CMOS logic or driver chips. Among these components, the laser acts as the light source that carries modulated signals; the modulator converts electrical signals into optical signals, while the photodetector performs the reverse operation by converting optical signals back into electrical form. Figure 17 illustrates this process. These components are typically fabricated using silicon-on-insulator (SOI) technology.

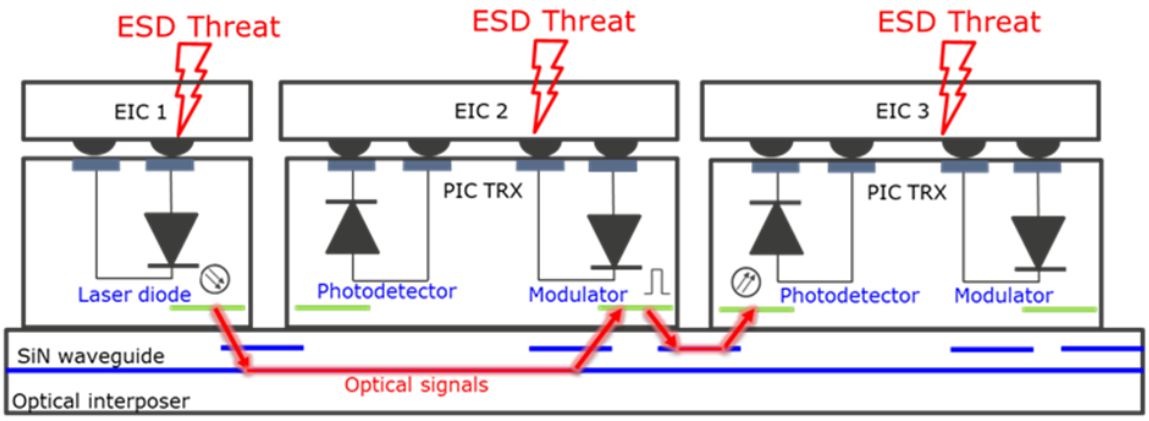


Figure 17: Schematic of Optical Interposer Functionality Containing Laser, Modulator, Waveguide, and Photodetector With ESD Threat at Bond Pads

In CPO and optical I/O systems, silicon photonic components such as lasers, modulators, and photodetectors are integrated closely with electronic chips. These sensitive photonic elements are susceptible to ESD events during assembly and packaging, particularly at the bond pads where electrical connections are established. The very high data rates of these applications [39] limit the pad capacitance budget, making ESD protection especially challenging, as photonic devices typically offer low self-protection. As optical packaging continues to evolve, ESD targets in silicon photonics must align with advancements in heterogeneous integration and advanced packaging technologies.

4.7 System-Level ESD

Recent developments in system level ESD have increased attention to topics such as system level direct pin discharge (SL-DPE) and transient absolute maximum rating (tAMR). These emerging areas have attracted considerable interest within the ESD community. The Industry Council on ESD Target Levels continues to facilitate discussion and research to advance the industry's understanding and best practices.

The IEC 61000-4-2 ESD stress [8] needs to be applied to the grounded shield of a connector cable. Nevertheless, many users stress the connector pins directly to evaluate system level ESD robustness. The Industry Council on ESD Target Levels conducted a survey [40] to understand current ESD internal testing across interface types, test levels, and industries. The system level direct pin ESD survey targeted the use of stress pulses directly to system or subsystem pins of a system port like USB. IC suppliers and end customers across multiple industries and regions provided survey responses.

75% of participants report that system level direct pin discharge is done because it is a customer requirement, and about 60% regard it as a competitive advantage. Approximately two-thirds reported real-world failures, primarily at customer sites, which means that protecting the system against ESD is meaningful. System-level testing is predominantly performed using IEC 61000-4-2 generators, with human metal model (HMM) events being the main scenario of interest. Relatedly, 37% use the ISO 10605 test [9], which also uses an ESD generator with different current pulse shapes. Every respondent used contact discharge, and roughly half used air discharge. More than 60% rate the tests as repeatable. This is surprising, given that air discharge is shown to be non-reproducible and pulse-shape variation is so high that pulses can only be grouped into categories [41].

Testing is often customer-driven, with stress levels ranging from 2 kilovolts to 15 kilovolts for externally accessible pins. About two-thirds of survey respondents consider SL-DPE a design criterion, with design decisions largely based on TLP test results. However, less than half of

respondents report that there is a correlation between the field returns and the ESD robustness of the device. There might be different reasons. This could be due to the wide variety of applications. It may also result from a lack of a common test procedure in the industry. More than 40% use breakout boards or cables to test exposed pins, even though reports indicate that the layout of these breakout structures can affect pulse shape [42]. A changed pulse form can lead to misunderstandings and misaligned requirements between system designers and IC suppliers. Therefore, the industry needs a summary of current findings to build a common understanding. The Industry Council on ESD Target Levels will offer consolidated recommendations in a future report that is currently in preparation.

Absolute maximum ratings (AMR) are specified physical limits for storing, handling, and applying electronic or electrical products. The AMR provided in IC datasheets is often specified as a constant (time-independent) value, which can leave system designers in a quandary when their system involves unavoidable transient stress. Thus, system integrators and component vendors can work together to determine an acceptable maximum rating for a specific transient event. tAMR can be considered as a complement to the time-independent AMR. It is being introduced to better understand the short-term limitations in component behavior beyond normal operating voltages and currents. tAMR encompasses a very wide time range, from the sub-nanosecond to the static range (Figure 18). Creating a safe operating area (SOA) over this wide time range is time-consuming. In addition, different stress factors may apply, such as maximum voltage at a pin or the current flowing into a pin of the device. The matter is further complicated because the time-dependent stress profile is unknown. The application itself may also influence it. Therefore, even if the SOA of a device is known, the real-world stress and its translation to what the IC is exposed to is not straightforward. Therefore, the Industry Council on ESD Target Levels plans to publish an extension of White Paper 4 addressing the tAMR in greater detail.

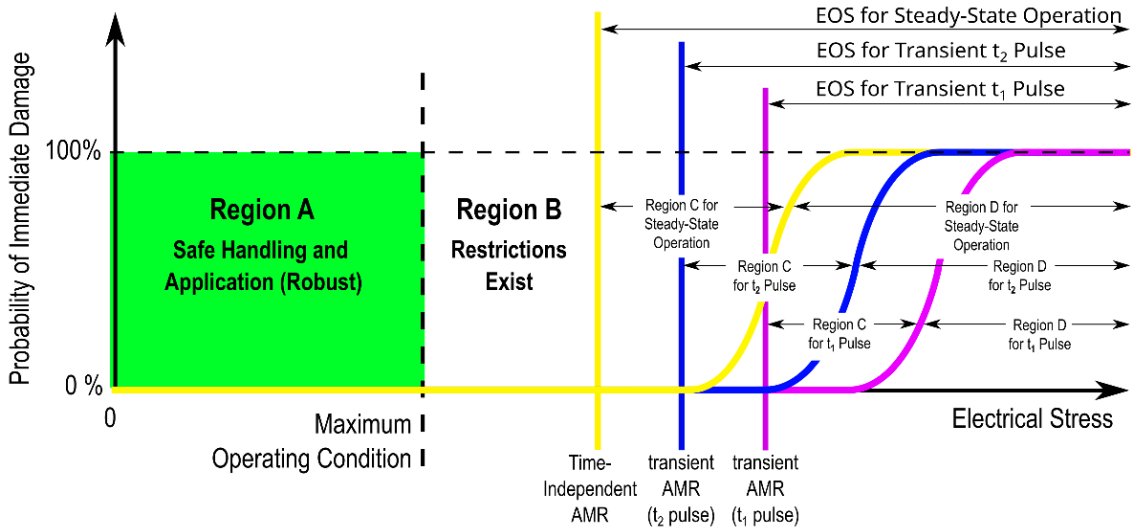


Figure 18: A Depiction of the Probability of Immediate Damage Versus the Pulse Duration With t1 < t2 [43]

4.8 Challenges for Latch-up Testing and Prevention

4.8.1 Latch-up Testing

4.8.1.1 Complexity of Test Standard

The JEDEC JESD78 latch-up test standard [24], which is the most widely used latch-up test for product qualification, recognizes four pin categories: supply pins, ground pins, input pins, and output pins. The test standard describes applicable test procedures and pin-biasing requirements based on these pin categories. However, some ICs may have pins that don't belong exactly to one

of these categories or that interact with other pins in ways that require special treatment to ensure that the underlying intention of the latch-up test is maintained. Examples include differential signal pins, pins with multiple digital or analog functions, antenna/RF pins, reference pins, and regulator pins. These special-pin scenarios will continue to challenge latch-up testing in the future. The existing “Special Pins” Annex A of JESD78 already gives some guidance on this topic. However, a planned JESD78 User Guide will significantly improve the guidance on special pins.

Since JESD78 introduced the concept of a “maximum stress voltage” (MSV) to account for hard technology and process limits by allowing reductions in applicable stress voltage limits, MSV applicability has been a major industry discussion point. A somewhat loose definition of MSV in the JESD78 spec has prompted some IC vendors to regard any damage that occurred during latch-up testing as being a result of exceeding the MSV - even if that damage was caused by a design weakness and not due to reaching a hard technology or process limit. Some vendors have even applied voltage limits defined by the AMR of an IC directly as the MSV, as highlighted in a recent latch-up survey conducted by the Industry Council on ESD Target Levels. This broad application of MSV poses a challenge because it may increase the risk of field failures. Determining the correct MSV for a given pin failure scenario can be cumbersome and error prone. The planned JESD78 User Guide will supplement the MSV coverage in the main JESD78 document. It will provide much-needed clarification for determining and using the MSV.

4.8.1.2 High-Current and High-Voltage Supplies

As power consumption continues to rise due to larger ICs and the need for higher computing power, maximum supply currents have also increased. More high-voltage devices are also entering the market. Commercial JESD78 latch-up test systems may be unable to provide such high currents or voltages. This poses a challenge for latch-up testing.

Some companies use standalone external power supplies to overcome these tester limitations. However, their lack of controllability by the test system has caused issues with power ramp synchronization, voltage/current readout, and performing the required supply test (also known as “50% overvoltage stress”). Latch-up, indicated by a significantly higher current draw after a stress pulse, typically needs to be checked independently on such external standalone supplies. Manual control also risks failing to meet the timing specifications of JESD78, poor test repeatability, and missing a latch-up event.

Test system vendors have started to address this issue, for example, by offering system extensions that allow selected, pre-approved external power supplies capable of handling much larger voltages and currents. However, embedding external supplies into a test system, with full control over the timing of the power-up/power-down ramps and the trigger pulse sequence, as well as the ability to measure the applied external voltage and current values, can be difficult.

No matter how external power supplies are controlled and monitored, the test board must also provide access to the DUT. The board connectors and traces must be robust enough to sustain the high current or voltage without risking hardware damage.

4.8.1.3 Temperature Control

The latch-up testing must be done at a specific temperature. For example, for JESD78 Class II testing, the DUT junction temperature should be held at the maximum operating junction temperature specified for the product. This typically requires heating of the DUT, for example, through heated airflow or a direct contact heat transfer method. However, measuring the junction temperature (such as the die temperature), let alone controlling it precisely, has become increasingly difficult.

For practical reasons, it is often easier to control the case temperature or the ambient temperature, but this requires calculating the effective junction temperature using the thermal resistance network of the package and considering the dissipated power of the DUT (self-heating). JESD78 includes some guidance for junction temperature calculations, but this method could be inaccurate due to unaccounted heat flow through the package pins or socket and the unknown or unstable temperature of the test board.

Due to the ever-increasing power demand of modern ICs, especially in the high-performance computing (HPC) market, the self-heating effect can be especially strong, requiring a cooling system to keep the part from exceeding the maximum junction temperature during latch-up testing. Without cooling, the risk of a “thermal runaway” effect, where the supply current increases and the self-heating effect feeds upon itself, could be high.

On-die temperature sensors or thermocouples attached to the DUT package can help with temperature control. However, reading them out during the latch-up test execution and directly integrating them into the thermal control loop can be difficult.

4.8.1.4 Low-Voltage Product Testing

The continuous supply voltage downscaling in modern nano-scale logic ICs and mobile SoCs has significantly affected latch-up testing of signal pins. The conventional JESD78 signal pin test (also known as “current injection test”) attempts to inject, for example, ±100 milliamperes into a pin assuming that the JESD78 “Immunity Level A” is being pursued. The test standard allows trigger pulse voltage limits that are 50% above and 50% below a signal pin’s maximum operating voltage swing. For I/O pins using a traditional ESD protection method, the injected current usually flows through a diode to VDD or VSS. However, silicon diodes typically require at least 1 volt to fully turn “on” and conduct the 100-milliampere current. This means that if a product's supply voltage is below ~2 volts, the applied trigger voltage limits start decreasing the actual injection currents below the 100-milliampere target level. For parts with a maximum operating voltage below ~1 volt, the injected current may be essentially zero, but the “Immunity Level A” would still be achieved per JESD78 specification.

The reduction or total lack of injection current during JESD78 testing of such low-voltage (LV) signal pins may not pose a latch-up risk in most system applications. One justification for the reduced JESD78 voltage limits, as perceived by the industry, is that reflections on a signal line due to impedance mismatch could lead to the 50% voltage “overshoot” or “undershoot” at a signal pin. Therefore, the voltage limits should indeed scale with the voltage range of the signal pin. However, while this may be true for signals exchanged within a closed system, external LV pin applications driven by growing needs to reduce power and increase signal speed may be subject to higher stress events from the outside.

The latch-up survey has shown that some chip vendors already consider applying stress levels to LV signal pins that are higher than required by the JESD78 standard - either for evaluation purposes or even as part of company internal qualification requirements. This may become increasingly important, given that a strict interpretation of LV pin injection limits already drives relaxation of latch-up design rules in advanced technology nodes (as discussed in a later section). Latch-up qualification testing of LV signal pins will be challenging, as it must balance what the current JESD7 standard requires with what is a reasonable exceedance to minimize latch-up failures in the field. A future revision of JESD78 may also address this topic.

4.8.1.5 High-Voltage Product Testing

The highest-voltage ICs are shifting from silicon to SiC or GaN, which don’t carry a classic SCR-based latch-up risk. But silicon ICs with a 100-volt to 500-volt supply voltage range using, for example, BCD or HVIC technologies, remain in great demand for automotive (electric vehicles), industrial (robotics, smart grids, and telecom), and many other applications. Beyond the potential latch-up tester limitations for high-voltage (HV) pins mentioned above, test challenges also stem from technology limitations.

HV circuits typically operate relatively closer to the safe operating area (SOA) than, for example, CMOS circuits at 5 volts or below. While lower-voltage ICs often tolerate the 50% over-voltage and under-voltage limits that the JESD78 test standard requires during supply pin test and signal pin test without suffering damage, HV ICs usually don’t have such a large “headroom”. Since an earlier version of JESD78, this limitation has been recognized and addressed by introducing the concept of an MSV. The latch-up test standard allows replacing the classic voltage limits with the MSV based on the assumption that system designs must take precautions anyway to limit excess

voltages that could damage a product. However, the applicability and determination procedure of the MSV have been controversial, and some have perceived the MSV as a potential product-qualification “loophole.”

The existing latch-up test routine for HV pins requiring the application of the MSV has proved challenging. Determining MSV can be complex and time-consuming and, in practice, must be repeated for each different HV pin type. As mentioned above, a future revision of JESD78 may address this by revisiting and possibly updating the voltage limits applicable to HV pins, so a more straightforward test approach could be taken that does not always require applying MSV.

4.8.1.6 Multi-Chip Modules and System-In-Package

Since traditional chip scaling (per “Moore’s Law”) has become harder, the semiconductor industry has been moving toward advanced packaging methods such as multi-chip modules (MCM), system-in-package (SiP), or 2.5D/3D integration. Using multiple “chiplets” in a packaged product has raised questions about latch-up testing. Ultimately, the final product must pass the latch-up test standard. However, this approach may not always be the most practical, and latch-up qualification of individual chiplets, if feasible, may suffice.

Theoretically, only the pins of a chiplet that connect to external pins of the SiP package need to be subjected to LU testing. However, determining which pins will be purely internal pins for communication between chiplets may be challenging and may not be the same for all possible SiP use cases. The placement of discrete devices (for example, resistors, capacitors, inductors, BJTs, and MOSFETs) inside a SiP may also impact the latch-up susceptibility. SiPs have a major advantage because these use a variety of chip technologies ideally suited for certain tasks like computing, analog, I/O, RF, etc. This may increase the complexity of latch-up testing. This is especially true if some technologies have a low intrinsic risk of latch-up, such as SOI technologies. New and potentially unknown interactions between chiplets may also require special attention during latch-up testing.

Latch-up testing of individual chiplets may be straightforward if these are available as a packaged part for board-level testing. For bare die, the situation is different - currently there are no known commercial latch-up testers that support probe-level testing. Therefore, such chiplets must either be put into an engineering package for latch-up testing, or latch-up robustness must be assessed in every SiP that uses the chiplets.

4.8.1.7 High Pin Count Devices

Devices with a very large number of pins are becoming more popular because these need more data and higher integration. Available latch-up testers may not support such high pin counts. To solve this problem, some chip vendors have started using pin partitioning methods for product qualification, for example, using two different test boards with two corresponding latch-up test programs. The challenge is to partition the pins so that no latch-up scenario is being overlooked or suppressed. Although JESD78 does not currently support such a “split-board” method, it could be acceptable and yield results identical to “full-board” testing. However, understanding all possible interactions between latch-up emitters, or “aggressors” (diffusion areas coupled to signal pads), and nearby SCR structures, or “victims”, on the chip requires in-depth knowledge of the SoC design. Depending on the demand for such “split-board” testing, a future revision of the JESD78 standard may address this topic.

4.8.1.8 Large Number of Supply Domains

Latch-up testing of larger chips that need external supplies at many different voltage levels has always been challenging because commercial latch-up test systems have hardware limitations. This has led to using external power supplies (with similar concerns as mentioned in an earlier section) or consolidating supplies at similar, but not identical, voltage levels, at the risk of different latch-up test results.

While the number of external power supplies seems to have stayed flat, there has been a strong shift toward more complex chip architectures with many internal voltage domains to meet power-versus-performance needs. In complex SoC architectures, different internal blocks may need different supply voltage levels to optimize operation, and these may benefit from workload-based voltage scaling. Some blocks may even be turned off completely when not in use.

The latch-up test standard requires that, as part of the DUT pre-conditioning, all external and internal supplies and all functional blocks be powered up to maximum operating voltage levels. This often poses a challenge since such a power mode may be for latch-up testing only and considered purely "artificial", not resembling a real SoC usage scenario. To address this, chip vendors have started including dedicated latch-up test states in their internal SoC design requirements and SoC verification flows. This may even require adding dedicated test mode selection pins to internal IP blocks. If a SoC does not support powering up all power domains at the same time, latch-up testing must be performed in multiple power states to ensure full coverage and avoid overlooking potential latch-up scenarios.

Although less likely in advanced chip generations, static pre-conditioning that holds certain external pins (for example, a RESET pin) in predefined logic states may suffice. If vector patterns are required to program the DUT for pre-conditioning, the vector length must be supported by the latch-up test systems, which may have limitations. SoCs containing secure modules may require very long vector patterns to satisfy the JESD78 pre-conditioning requirements. Therefore, some vendors have switched to regular automated test equipment (ATE) for latch-up testing, which comes with its own challenges because ATE testers are typically not designed for this task and latch-up test engineers may not be familiar with ATE operation.

4.8.2 Transient Latch-up

The latch-up survey [44] has shown that many real latch-up failures in the semiconductor industry were related to insufficient coverage of the JESD78 test standard. One prominent example is transient latch-up, where a device is subjected to very brief external voltage or current stress, for example, during a system-level ESD/EFT event or a cable discharge event. The JESD78 standard checks only for DC latch-up, with a typical stress duration in the millisecond range and a relatively slow trigger-pulse rise time.

The ESDA has published a standard practice on transient LU testing at the device level, ANSI/ESD SP5.4.1 [26], in 2017, which was reaffirmed in 2022. While this standard practice provides valuable insights into transient latch-up testing, it also presents practical challenges. For example, ANSI/ESD SP5.4.1 does not provide clear pass/fail criteria; thus, test results must be interpreted and compared with other products. Results also strongly depend on the test conditions, namely the pulse shape/width/rise time and the pulse source type (forcing current versus voltage). In the real world, many different stress conditions may be hard to characterize and may not be covered by a single test setup. The integrity/stability of power supplies and system parasitics may also play major roles. Results may be poorly reproducible across different labs, testers, and companies. Many labs may not be able to create precise and repeatable stress pulses that can be accurately measured.

4.8.3 Latch-up Prevention

4.8.3.1 Advanced CMOS Technologies

Advanced technology nodes, namely FinFET and GAA, are changing the latch-up landscape. Source/drain implants and N-well and P-well regions are becoming increasingly shallow, and metal and via interconnect layers are becoming much more resistive. From a latch-up risk perspective, shallower anode and cathode regions help suppress parasitic SCRs. However, shrinking layout geometries reduce the anode-to-cathode spacing and therefore increase the latch-up risk. This is countered by the reduction in supply voltage, which reduces the latch-up risk.

Guard rings are an important design element to prevent latch-up by improving well strapping. This makes it less likely for the parasitic NPN and PNP devices that form an SCR ("victim" devices) to turn on. The lighter well doping used in advanced technologies can increase the bipolar gains of parasitic NPNs and PNPs, making it easier for an SCR to turn on (due to a lower triggering voltage)

and to sustain (due to a reduced holding voltage). Wafer thinning, by contrast, makes the base regions of NPNs and PNPs thinner and can help reduce latch-up risk. Furthermore, advanced backside power delivery (BPD) technologies can help provide a low-resistive well contact from the backside of the thinned wafer.

When placed around latch-up emitters (“aggressors”), such as ESD diodes or output drivers, guard rings serve as collectors to absorb most injected carriers and prevent them from triggering nearby SCRs. Since the introduction of FinFETs, guard rings have become segmented and therefore less effective. More importantly, increasing interconnect resistance, especially in lower backend layers, has required strapping guard rings across multiple metal layers to achieve a reasonably low connection resistance to power and ground pins. Quite often, guard rings around latch-up emitters require parallel metal strapping all the way up to a thick metal layer. This may block precious signal routing space and require careful floorplanning and a suitable bus-frame architecture for an I/O pad cell.

Although SOI technologies are considered latch-up immune due to the complete isolation of NMOS and PMOS devices by the buried oxide (BOX) layer, some advanced SOI technologies may still carry a latch-up risk. A modern fully depleted SOI (FDSOI) technology, for example, may take advantage of the “back gate” effect where a well region under the BOX layer is used to modulate the threshold voltage of the SOI MOSFET above. This can be useful for low-power chips, as the core leakage can be traded off versus speed. In a triple-well process, this can lead to the formation of grounded N-wells and powered isolated P-wells, which can act as strong cathodes and anodes, respectively, to form an SCR. Besides well junctions, there could also be other PN junctions formed by direct implants into the bulk layer where the BOX has been removed or omitted, such as implementing ESD protection devices like diodes, GGNMOS, or SCRs. These PN junctions could contribute to latch-up, as in conventional bulk technology. A solid understanding of SOI technologies is required to gauge the latch-up risks.

4.8.3.2 Design Rules

Due to a reduced I/O pad voltage in advanced CMOS technologies (see above section “Low-Voltage Product Testing”), the conventional JESD78 latch-up test may inject little or no current during a signal pin test. This has led to a relaxation of latch-up design rules by semiconductor fabs, for example, the omission of guard rings around emitters or the elimination or reduction of so-called emitter “hot zones” (such as regions where “victims” need to follow stringent guard ring or well tie spacing rules to suppress parasitic SCRs). While such a design rule relaxation may reduce silicon cost due to a more compact chip layout, it is specifically targeting JESD78 qualification. This may introduce a risk of latch-up field failures, for example, due to potential external system stress that may not scale down proportionally with the system supply voltage. This risk would need to be mitigated by more sophisticated system design methods. Also, in the absence of an industry standard for transient latch-up, passing the JESD78 qualification (also known as “DC” latch-up testing) has so far been quite effective in addressing transient latch-up risks as well. However, it remains to be seen if this will continue for low-voltage systems.

4.8.3.3 EDA Checks

Automated latch-up checks have become a crucial part of EDA checks for advanced ICs and are mandatory for chip tape-out sign-off. Advanced EDA tools are expected to become even more widespread in the industry. As computing power rises, EDA checks can afford to become more complex. However, latch-up checks for very large chips can still take many days to complete, which may challenge a product tape-out schedule.

Most latch-up checking is done by DRC, primarily by checking emitter guard rings and well ties around “victim” structures that fall within an emitter “hot-zone”. More advanced standalone EDA tools can also look for parasitic SCRs and provide scores to gauge the specific latch-up risk of each SCR. Field solver techniques may be used, for example, to calculate the two-dimensional distribution of injected minority carriers into a chip substrate by a latch-up emitter or even by multiple emitters triggered in parallel. The actual injected current, type and size of the emitter, size of the guard rings, and the presence of other collectors between the emitter and a victim SCR could be

considered. This calculation could be done on a real chip layout and provide a more accurate assessment of latch-up risk in nearby parasitic SCR structures, essentially replacing the simple "hot zone" concept that uses a constant radius around individual emitters.

Due to the aforementioned stringent metal strapping requirements for guard rings in advanced CMOS technologies, new DRC-type checks may consider the point-to-point (P2P) resistance from each spot of a guard ring's active region (for example, the silicon contacts) and the power or ground pins of the chip. While this can be computationally expensive - especially if performed at the full SoC level - it can give valuable insight into the effectiveness of a guard ring.

5.0 COMPUTATIONAL METHODS

This section reviews the evolution of computational methods for ESD design, verification, modeling, and reliability analysis, and outlines the expected roadmap for future developments. The main drivers include electronic design automation (EDA) verification tools, SPICE-based electrical analysis, compact modeling, ESD test-data evaluation, high-performance computing, and emerging artificial intelligence (AI) and machine learning (ML)-assisted methodologies. Figure 19 summarizes the historical evolution and projected roadmap of these computational methods for ESD applications.

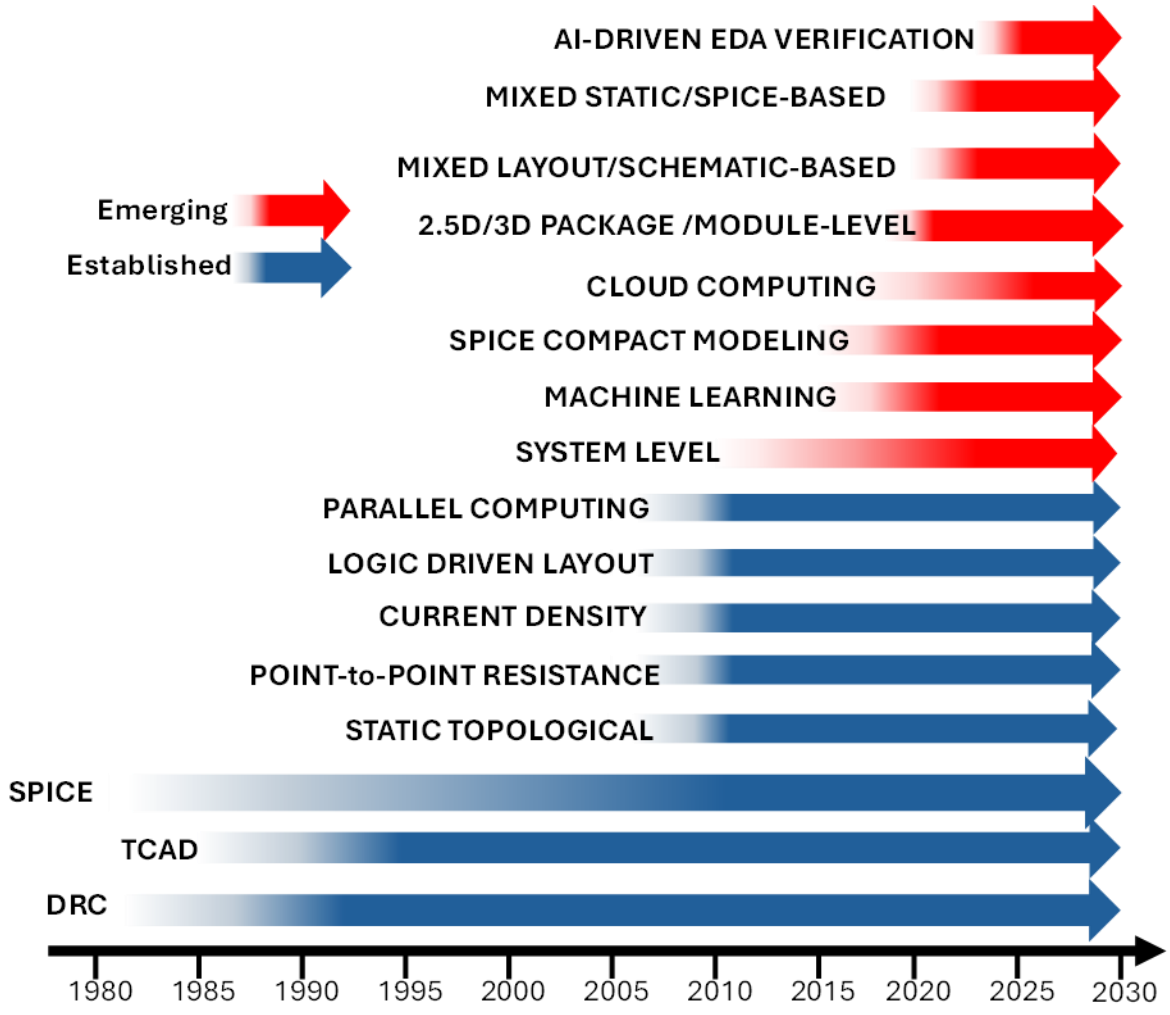


Figure 19: History and Roadmap of Electronic Design Automation (EDA) Tools

5.1 Established Methods (Late 1980s – Today)

Beginning in the late 1980s, standard IC design tools such as design rule check (DRC), technology computer-aided design (TCAD), and SPICE simulation started to be employed for ESD device development, protection design, and verification of ESD rules. During the 1990s and early 2000s, these tools became progressively integrated into ESD design methodologies, although complete ESD network verification was still largely performed manually.

SPICE-based circuit-level simulation has been a foundation of modern IC design for decades, and efforts to apply SPICE simulation to ESD design and verification began in the 1980s. Early work focused on modeling protection structures and understanding ESD behavior in emerging semiconductor technologies. However, despite decades of development, ESD protection design still relies heavily on trial-and-error methodologies and cookbook approaches derived from prior art and engineering experience. In contrast to mainstream IC design, widespread adoption of SPICE-based ESD verification has been limited by the lack of accurate, robust, and easy-to-use ESD-capable compact device models [45].

In parallel, ESD reliability qualification methodologies have also become well established. Various ESD stress pulses and qualification tests have been routinely applied to integrated circuits to assess device robustness and reliability behavior. Although these testing methodologies have matured significantly over time, interpreting and analyzing ESD test results has remained highly dependent on expert knowledge and engineering experience. Even today, ESD reliability evaluation often requires senior specialists to determine the true impact and root causes of observed failures or parameter shifts.

In the late 2000s, dedicated ESD verification tools became commercially available and enabled automated verification at both schematic and layout levels. These methodologies included static topological verification, point-to-point resistance analysis, current density analysis, and logic-driven layout checks. Over time, these techniques became highly customized and broadly adopted as standard ESD verification flows within major semiconductor companies.

During the first decade of the 2000s, parallel computing also emerged as an important computational accelerator for ESD verification. The increasing complexity of IC designs and larger verification datasets drove the adoption of multi-core and distributed computing infrastructures to reduce runtime and improve scalability. Today, parallelized execution is a standard capability of most industrial ESD verification environments.

In the 2010s, ESD verification methodologies expanded to support increasingly complex SoCs containing multiple supply domains, mixed-voltage circuitry, RF blocks, analog circuitry, and advanced packaging technologies. During this period, layout-extracted netlist verification became increasingly established for sign-off-level analyses. Layout-based methodologies enabled more accurate assessment of parasitic resistances and inductances associated with ESD current paths, improving correlation between verification results and silicon behavior.

At the same time, the boundary between static verification and SPICE-based electrical simulation progressively narrowed. Static topological analyses began generating relevant SPICE netlists for complex ESD scenarios, such as power-domain crossings and mixed-voltage interfaces. Simplified SPICE simulations were increasingly integrated into topological verification flows to better evaluate the severity of violations and reduce false positives. These mixed static/SPICE-based methodologies are now becoming standard practice in advanced ESD verification flows.

The semiconductor industry has increasingly recognized the importance of compact modeling for SPICE-based ESD simulation [46,47]. Compact device models form the backbone of SPICE simulations and must accurately reproduce device behavior under high-current and high-voltage ESD stress conditions beyond the normal operating regime. One of the most critical and difficult effects to model is the snapback behavior observed in SCRs, bipolar transistors, and MOS devices during ESD events. Because conventional industry-standard SPICE models were not originally capable of reproducing snapback behavior, researchers have developed customized ESD compact models using several approaches, including proprietary C-code implementations, Verilog-A behavioral descriptions, macro-models composed of standard devices, and wrapper modules attached to standard compact models.

Beyond snapback, other ESD-specific physical effects also require dedicated modeling approaches. For example, diode behavior during ESD stress involves voltage overshoot, current saturation, forward and reverse recovery, conductivity modulation, and self-heating effects that standard SPICE diode models do not adequately represent. Compact models that can predict thermal ESD failure or dielectric breakdown have also been reported.

To address the growing need for standardization, the Compact Model Coalition (CMC), associated with the Silicon Integration Initiative (Si2), initiated an ESD compact modeling program about a decade ago. The CMC ESD subcommittee established requirements for standard ESD compact models capable of balancing simulation accuracy with practical deployment and computational efficiency. The standardization effort adopted flexible and adjustable topologies, including parameterized Verilog-A solutions.

Verifying the ESD protection design of increasingly complex ICs containing multiple supply domains, mixed-voltage circuitry, RF blocks, analog circuitry, and advanced packaging technologies remains a major driver for new EDA tool capabilities [48]. More recently, support for advanced packaging technologies such as 2.5D and 3D integration has become an established requirement. Existing EDA tools have evolved to assist in the co-design and verification of dies, packages, interposers, and modules. Initial standardization efforts, including CDXML [49] and 3Dblox [50], have emerged to improve interoperability between heterogeneous EDA environments and simplify the setup of complex multi-die ESD verification flows.

Although some semi-automated ESD test-analysis methods have emerged over the last decade, interpreting qualification data and failure analysis still largely relies on manual expert assessment. This limitation has become a key motivation for introducing ML methodologies into future ESD workflows.

5.2 Artificial Intelligence and ESD

ESD engineering has reached an inflection point where traditional design and verification methodologies are becoming insufficient for emerging technology challenges. Advanced nodes, 3D ICs, and die-to-die interfaces are exploding ESD complexity beyond what manual expert judgment can effectively manage. Traditional ESD design relies heavily on expert judgment and late discovery, often identifying critical issues only after significant design investment. A single ESD-driven re-spin can cost $5-10M and delay time-to-market by 6-12 months. AI offers a transformative path to early risk prediction, faster convergence, and scalable expertise that can shift ESD risks left in the design process, enabling risk identification before silicon commitment.

AI can augment ESD engineering workflows across the design cycle. Early and shift-left ESD risk prediction could use ML models trained on historical design, simulation, and silicon data to predict CDM and HBM risks before tape-out. Automated verification could employ AI to triage rule violations, identify weak current paths, and detect missing clamps, with the capability to recommend or auto-generate known fixes for common issues. High-complexity IP management, particularly for die-to-die interfaces with thousands of pins, could leverage AI to cluster pins by electrical characteristics and learn stress patterns. ML-assisted surrogate models could speed SPICE and TCAD exploration, enabling faster design iteration with quantified risk visibility. Large language model (LLM)-based copilots could democratize ESD expertise by surfacing design guidelines, prior failure modes, and best practices throughout the design cycle.

Despite promising applications, AI implementation in ESD design faces significant challenges. Highly nonlinear physics, nanosecond-scale transients, snapback behavior, and parasitic coupling challenge generic ML models. Data scarcity and inconsistency create fundamental training limitations, as ESD failures are rare events and datasets are fragmented across proprietary databases. Interpretability is mandatory for safety-critical ESD applications; black-box predictions that cannot be validated against physics-based understanding are unacceptable for sign-off decisions. Generalization risk across technology nodes, package types, and foundry processes limits model transferability. AI must serve as a decision-support tool for ESD experts, not an autonomous replacement.

Looking ahead, EOS/ESD Association, Inc. is uniquely positioned to lead the industry's AI transition through standardization and validation. As these technologies mature, the ESDA can define

anonymized, vendor-neutral ESD benchmark data formats that enable industry-wide model training. AI validation guidelines will establish what "AI-qualified" means for ESD sign-off, defining requirements for model accuracy, interpretability, and robustness. An EDA collaboration framework can guide how AI integrates with existing ESD verification tools and design flows. LLM training and governance initiatives can curate ESD examples, standardize terminology, and establish guardrails to prevent incorrect recommendations. Community alignment through a shared roadmap across semiconductor companies, foundries, and EDA tool vendors will coordinate development priorities. AI will not replace ESD engineers, but ESD engineers who effectively use AI will replace those who do not.

5.3 Emerging Methods and Future Roadmap (2025 – 2035)

5.3.1 Near-Term Developments (2025 – 2030)

Over the next five years, ESD computational methodologies are expected to continue evolving toward highly integrated, automated, and compute-intensive verification and reliability-analysis environments.

One major development area is the broader deployment of mixed layout/schematic-based verification methodologies. Partial layout parasitic extraction will increasingly be introduced into schematic-level verification flows earlier in the design cycle, enabling more accurate prediction of ESD voltage drops and current distributions before full layout completion. This approach is expected to improve design convergence and reduce late-stage redesign iterations.

At the same time, layout-extracted ESD verification will continue to grow in importance as IC complexity increases. Because layout-based netlists are significantly larger than schematic netlists, EDA vendors are expected to further adopt cloud computing infrastructure, distributed execution, and hardware acceleration technologies such as GPUs and xPU-based architectures to maintain acceptable runtime and scalability.

Another important near-term trend is the increasing convergence of static and dynamic verification techniques. Full-chip topological analyses will progressively integrate embedded SPICE simulation capabilities, enabling context-aware verification and improved electrical accuracy within automated EDA flows. These hybrid methodologies are expected to reduce manual debugging effort and improve prioritization of reported violations.

SPICE-based ESD simulation itself is expected to become substantially more important in future ESD design methodologies. As advanced semiconductor technologies continue to scale, traditional rule-based verification alone is becoming insufficient to accurately predict complex transient ESD behavior. Industry-standard ESD compact models are therefore expected to play a central role in enabling broader adoption of SPICE-based dynamic ESD verification [46,47].

Following the release of the ASM-ESD diode model, the Compact Model Coalition (CMC) has begun developing a standard ESD MOSFET compact model. Multiple candidate model architectures are currently under evaluation. The future standard ESD MOSFET model is expected to combine conventional MOSFET compact models for normal operating conditions with Verilog-A wrapper models that can reproduce high-current bipolar and snapback behavior during ESD stress events. The model is expected to be completed within approximately three years.

By approximately 2030, multiple industry-standard ESD compact models are expected to become available [46, 47]. These models will likely capture not only primary ESD parameters such as trigger voltage (V_{t1}), holding voltage (V_h), and on resistance (R_{on}), but also important secondary effects including:

- voltage overshoot,
- rise-time dependence of Vt1,
- conductivity modulation,
- self-heating,
- current saturation,
- forward and reverse recovery effects in diodes,
- and transient bipolar conduction effects.

Simplified SPICE compact models may also be developed specifically for integration into topology-based EDA verification flows, where simulation speed and scalability are critical requirements.

Verification setup automation is also expected to significantly improve during this period. EDA environments will increasingly automate the inclusion of design initialization information such as pad functionality definitions, ESD stress classifications, and AMRs. In parallel, ESD verification flows are expected to become more unified and homogeneous across schematic, layout, package, and module-level verification domains.

For advanced packaging applications, the industry is expected to further develop standardized ESD specification formats and interoperable verification infrastructures. Standards such as CDXML [49] and 3Dblox [50] may evolve into broader ecosystems supporting seamless data exchange between foundries, package designers, and EDA vendors.

ML and AI are also expected to become important contributors to ESD verification and reliability workflows during this timeframe. One of the first major applications is expected in ESD test-data analysis and qualification support. ML approaches could help diagnose failures at the earliest indication of symptoms, recognize recurring failure patterns, and reduce duplicate testing for already identified root causes. Emphasis is expected on learning how to interpret ESD qualification data and identifying meaningful correlations between test signatures and underlying physical failure mechanisms.

ML is also expected to support the analysis of functional parameter shifts resulting from ESD stress. Automated recognition of abnormal parameter trends could significantly improve evaluation efficiency and reduce uncertainty in qualification results.

Another important application area is AI-assisted ESD protection design. These methodologies will require establishing reliable “ground truths” derived from large volumes of historical ESD test data and silicon-debug information. Once trained, ML systems may help engineers identify recurring design weaknesses, recognize failure patterns more rapidly, and accelerate root-cause analysis during product development.

ML is also expected to become an enabling technology for SPICE compact model development. AI-assisted modeling methodologies may significantly reduce model-development time compared with conventional parameter extraction and physics-based calibration approaches, particularly for complex ESD phenomena that are difficult to represent analytically.

Commercial EDA platforms have already started integrating AI agents capable of orchestrating complex verification flows, assisting in rule coding, dynamically adapting verification strategies, and recommending corrective actions for violations. To further accelerate research and adoption, the availability of open and standardized ESD test-result datasets may become increasingly important for academic and industrial ML development.

5.3.2 Long-Term Vision (2030 – 2035)

Beyond 2030, ESD computational methodologies are expected to evolve toward highly autonomous, data-driven verification and reliability ecosystems.

AI-driven EDA environments may progressively transition from assistive tools toward semi-autonomous verification systems capable of:

- generating verification plans,
- adapting rule decks dynamically,
- optimizing verification strategies,
- predicting high-risk ESD structures,
- automatically correlating test results with design weaknesses,
- and proposing design modifications with minimal human intervention.

ML may eventually enable continuous feedback loops between silicon qualification, failure analysis, SPICE modeling, compact model generation, and ESD design optimization. In such frameworks, qualification data from production devices could continuously improve future verification models and protection methodologies.

Future SPICE compact models are expected to become increasingly comprehensive, scalable, and interoperable across multiple EDA environments [46,47]. AI-assisted compact modeling approaches may eventually generate predictive behavioral models directly from silicon measurement data while minimizing manual calibration effort. However, achieving widespread industrial deployment will require substantial progress in reducing the computational cost, memory requirements, and training complexity associated with large-scale ML algorithms and high-fidelity transient simulations.

Future ESD verification flows may also become increasingly physics-aware and multi-domain, combining:

- electrical simulation,
- thermal analysis,
- electromagnetic modeling,
- reliability prediction,
- AI-assisted failure diagnosis,
- compact-model generation,
- and package-system co-simulation within unified computational environments.

Large-scale cloud-native infrastructures and heterogeneous compute clusters with advanced memory and storage architectures are expected to become essential components of next-generation ESD verification platforms. As verification datasets continue to grow, scalable AI training databases and high-performance computing resources will likely become strategic requirements for both EDA vendors and semiconductor companies.

In parallel, further standardization across tools, foundries, packaging technologies, and verification environments is expected to enable highly interoperable and automated ESD signoff methodologies spanning the entire semiconductor system hierarchy, from device level to module and system level.

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