EOS/ESD Association, Inc.

Electrostatic Discharge (ESD) Technology Roadmap

EOS/ESD Association, Inc.
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Rome, NY 13440

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The following individuals contributed to the development of the EOS/ESD Association, Inc. Technology Roadmap:

Mirko Scholz Chair of Advanced Topics Committee		Shubhankar Marathe Vice Chair of Advanced Topics Committee
Andres Bong Micron	Andrea Boroni STMicroelectronics	Gianluca Boselli Texas Instruments, Inc.
Brett Carn Intel (retired)	Lorenzo Cerati STMicroelectronics	Shih-Hung Chen AMD
Ann Concannon Texas Instruments, Inc.	Reinhold Gaertner Infineon Technologies AG	Robert Gauthier IBM
Eleonora Gevinti STMicroelectronics	Michael Khazhinsky Silicon Labs	Michelle Lam IBM
Ian Lin Imec	Alain Loiseau Globalfoundries	Tom Meuse Thermo Fisher
Souvick Mitra Micron	Mohamed Moosa NXP Semiconductors	Nathaniel Peachey Qorvo
Nicolas Richaud Intel	Scott Ruth AMD	Marko Simicic Imec
Theo Smedes NXP Semiconductors	Wolfgang Stadler Intel (retired)	Michael Stockinger NXP Semiconductors
Pasi Tamminen Danfoss	Heinrich Wolf Fraunhofer EMFT	Paul Zhou Analog Devices

EOS/ESD Association, Inc.'s Electrostatic Discharge (ESD) Technology Roadmap

1.0 SYNOPSIS

This document is divided into four main sections. The first provides estimates of future ESD thresholds of semiconductor devices and the potential impact on ESD control practices. These levels are strongly technology and design-dependent and need to be periodically revised in the context of advances in the electronics industry. The threshold estimates discussed in this roadmap are intended to reflect the prevailing trends in semiconductor technology as viewed by selected industry leaders. As in previous versions of this document, the integrated circuit (IC) industry is emphasized. Other major electronics industry segments are also experiencing increased ESD sensitivities (lowering ESD thresholds). Some examples are optoelectronics (light-emitting diodes, lasers, and photodiodes), printed circuit board assemblies, and thin-film transistor-based displays and circuits. However, ESD trend information is not usually readily available for these devices, and the standardized ESD tests are not defined or broadly applied.

This document presents the thresholds as "roadmaps" of estimated threshold changes until 2030. These projections provide a view of future device protection limitations driven by circuit performance requirements and technology scaling effects. It also provides a common view of expected device ESD performance variations as viewed by device (IC) suppliers, original equipment manufacturers (OEMs), and other users of ICs. Finally, these trends point to the need for continued improvements in ESD control procedures and compliance. Some linkage of these trends to process capability is also discussed, as is progress in other ESD events characterization, such as system-level, charged-board events, and cable discharge events.

The document's second part contains information on device testing trends and characterization from the ESDA and ESDA/JEDEC teams working on these methods. It is followed by an outlook on important trends in the semiconductor industry looking towards 2030. The roadmap closes with a section on electronic design automation (EDA), an important contributor to reliable and robust ESD and latch-up design.

2.0 DEVICE THRESHOLD TRENDS

2.1 Overview

In the late 1970s, ESD became a problem in the electronics industry. Low threshold level ESD events from people were causing device failures and yield losses. As the industry learned about this phenomenon, device design improvements and process changes were made to make the devices more robust and the processes more capable of handling these devices.

During the 1980s and early 1990s, device engineers were able to create protection structures that could withstand higher levels of ESD stress and thus made devices less sensitive to ESD events. Both device engineers and circuit designers were able to identify key technology parameters and design techniques that helped them develop more robust devices.

However, in the mid to late 1990s, the requirements for increased performance and the increase in the density of circuits predicted by Moore's Law on a device caused problems for traditional ESD protection circuits because they require additional area and add capacitance. This was exacerbated by the continued scaling of the technologies toward sub-100 nm feature sizes to achieve higher density and performance. The situation worsened with the advent of IC chips with sub-50 nm technologies rapidly going into production. Large, high pin count (> 1000 pins), packaged devices containing high-speed SERDES (HSS) input/outputs (IOs) that need to operate at 10-15 gigabit per second (Gbps) were introduced to fulfill the demand for high-speed internet operations. These IOs reached 20-30 Gbps at the 22 nm and 16 nm technology nodes, and with today's advanced technology nodes at 5 nm and 3 nm and beyond, HSS IOs in the 112 Gbps to 224 Gbps range are more prevalent. Consequently, the human body model (HBM) and charged device model (CDM) target levels had to be adjusted to accommodate these new IO performance levels.

The wireless connectivity of the world has driven both an increase in radio frequency (RF) applications and higher bandwidth requirements. In the mobile space, 4G LTE utilizes frequency bands up to 5.8 GHz. With the introduction of millimeter-wave 5G technology, the frequency bands go into the 28 GHz to 60 GHz regime. ESD protection must be balanced with performance for these RF applications since these higher frequencies cannot tolerate additional capacitive loads on signal nodes. Any ESD robustness built into the RF pins is often co-designed with the matching network for the application. This almost invariably leads to reduced HBM and CDM withstand voltages. The expectation is that these trends will continue as increased circuit performance will take precedence over ESD protection levels. HBM and CDM requirements must comprehend these technology trends for future device qualification.

2.2 Device ESD Threshold Roadmaps

The following sections show the ESD sensitivity trends based on the two ESD models used by device manufacturers in the device qualification process: HBM and CDM. The sensitivity limits are projections by engineers from leading semiconductor manufacturers.

2.2.1 Human Body Model (HBM) Roadmap

The forward-looking projections for HBM design through 2030 are indicated in Figure 1. The maximum levels represent what is typically possible from technology scaling, and the minimum levels represent the constraints from meeting the circuit performance demands. Figure 1 also shows the estimated ESD control capability for HBM during the same time based on the levels of HBM controls that may be in place. Significantly, HBM control methods in today's production areas have reduced the HBM target level from 2 kilovolts to 1 kilovolt [1]. This reduction in failure level is also justified by statistical data from nearly 21 billion devices that showed no significant difference in ESD related field returns versus the achieved HBM qualification level [1].

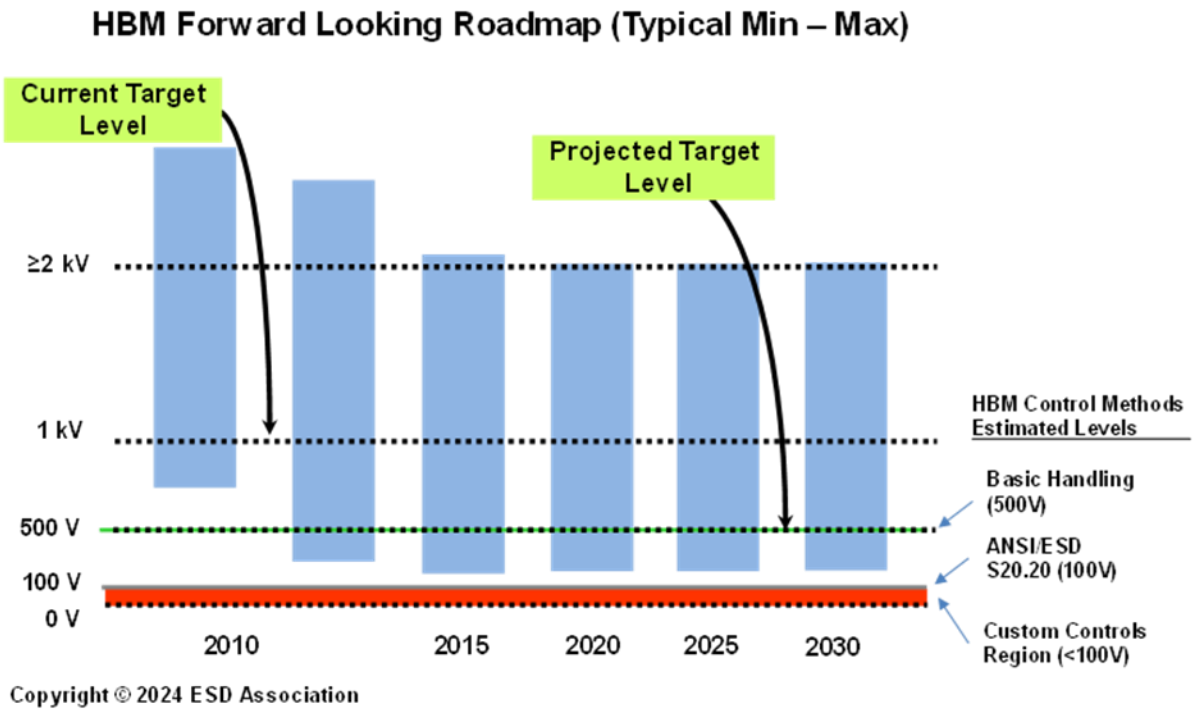

Figure 1: 2010 to 2030 Human Body Model Sensitivity Limits Projections

Even with this de facto target, some high-performance devices may only have 100 to 200 volts threshold. In the 2020 roadmap, it was suggested that a 500 V limit might be necessary.

Looking ahead to 2030, another drop in the HBM target level below 250 volts will be only necessary for some high-performance IO, such as 224 Gbps SERDES and RF applications. Implementation of improved HBM controls using the limits and requirements in ANSI/ESD S20.20 [2], IEC 61340-5-1 [3], or JEDEC JESD625 [4] will continue to be important to mitigate the risks of lower HBM protection levels. As shown in Figure 1, below 100 volts is a "custom controls" region in which non-standard process-specific controls are required. These controls are very specific to the manufacturing environment and may include, but are not limited to, tighter ESD control limits and increased frequency of compliance verification. Performing process capability assessments, as discussed in Section 2.5, has become even more important to address high-performance IO risks in manufacturing.

2.2.2 Charged Device Model (CDM) Roadmap

Today, 250 volts CDM is safe for production areas [5]. The technological impact on CDM comes from the required IO speeds and package size effects. Larger packages will experience higher discharge currents at a given stress voltage level. The observed impact becomes somewhat independent of the technology node starting around 22 nm as the reduction in oxide breakdown voltages is saturating. It becomes more dependent on the IO performance demands dictated by the loading capacitance. This map will change as package sizes become even larger. For example, for today's packages of 3000 pins (~3000-3500 mm^2) or more in a land grid array (LGA) or ball grid array (BGA), very high-speed IOs might barely meet a CDM target level of 125 volts. There is often a delicate balance between CDM robustness and RF performance in the RF space. Exacerbating this CDM sensitivity is that capacitors, frequently damaged by CDM transients, are widely used in RF designs for DC blocking, matching networks, filtering, and other applications related to the application functionality. Any circuit that would be used to protect these capacitors will ultimately degrade linearity, insertion loss, or otherwise impact the integrity of the RF signal. As higher bandwidth RF applications become more widespread, the achievable CDM performance will likely decrease further.

The projections for CDM sensitivity levels until 2030 are indicated in Figure 2. The figure shows that the current CDM target is 250 volts, reduced from the previous 500 volts from the early 2000s. The projected target of 125 volts is needed for some pins already today, primarily driven by the need for very high-performance IOs. The ESD control capability for CDM is also shown. Implementation of advanced CDM control methods and a more thorough process assessment are not only more critical but have become nearly mandatory for many products.

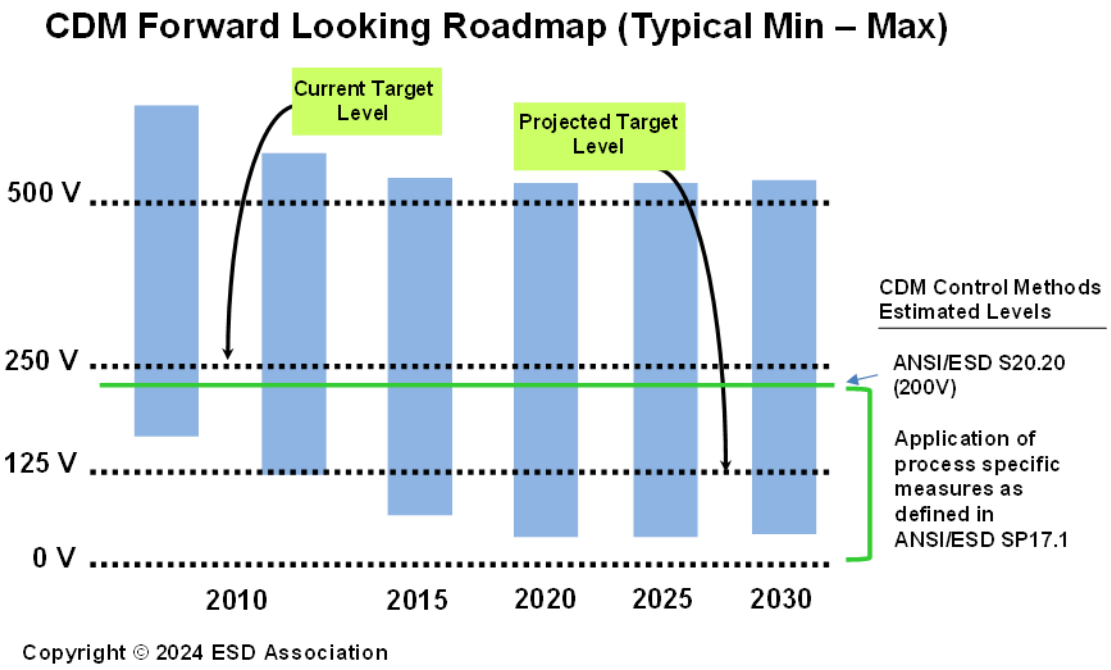

Figure 2: 2010 to 2030 Charged Device Model Sensitivity Limits Projections

The introduction of 2.5D and 3D integrated IC required the definition of additional CDM target levels for the internal die-to-die (D2D) interfaces. The provided range is based on the area constraints for these internal IO that only allow the use of very little to no additional area to enable minimal CDM robustness. Often, this minimal CDM robustness is only achieved by the self-protection capability of the connected circuitry. A detailed outlook on the technical challenges and achievable CDM target level is provided in Section 4.0.

2.3 Device ESD Thresholds and System Level ESD (IEC 61000-4-2): No Correlation

For several years, there has been a general perception that device-level ESD (for example, HBM) is a predictor or prerequisite for good system-level ESD robustness. This misconception has caused many OEMs to put special increased HBM requirements on devices, thinking it will improve the chances of passing the IEC 61000-4-2 system-level test [7]. This misconception was addressed in Industry Council White Paper 3 Part I [6]. As shown in Figure 3, from that study, it has been demonstrated that the **IEC 61000-4-2 system-level ESD and device-level ESD are not correlated with each other.**

At the system level, ESD robustness is a much more complex issue requiring a deeper understanding to address the ESD protection requirements for electronic systems such as laptops, cell phones, printers, home computers, and those in the automotive and industrial segments. These system complexities are due to the protection of external interfaces, such as the universal serial bus (USB), to the outside world. Such systems can lead to hard or soft failures after encountering the more severe ESD pulses, such as those specified by the IEC 61000-4-2 [7] or ISO 10605 [8] test methods.

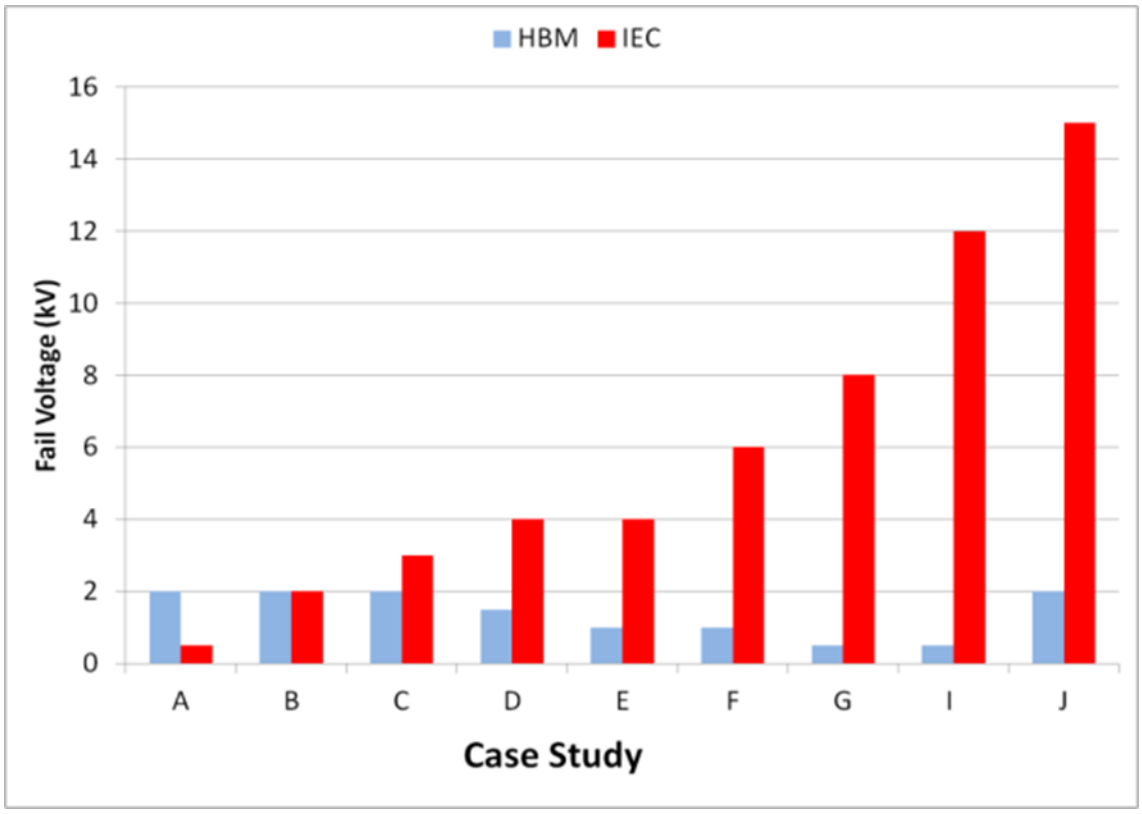

Figure 3: Comparison of IC Device Level and System Level ESD Failure Threshold of Various Systems (A-J) Showing that HBM Protection is not Related to System Level ESD Robustness [6]

As introduced in White Paper 3 Part I, a co-design approach is required. A basic version of the so-called system-efficient ESD design (SEED) has been proposed, which addresses hard failures related to IC pins with a direct external interface. More advanced co-design approaches are needed for soft (reversible) failures, which are more frequently reported. These are more challenging to understand and overcome and require an extension of the SEED approach to other failure mechanisms, including latch-up and electromagnetic interference (EMI) effects. These challenges and approaches are discussed in Part II of White Paper 3 [9]. The adoption of SEED within the Industry has begun, but adoption has been limited as the industry best determines how to supply the needed data and simulate the events. The trend of adopting SEED, though slower than expected through 2025, is expected to grow as the risk to external IO ports has not changed.

The important point for the present discussion is that no system-level failures are improved or reduced by increased HBM or CDM device threshold levels. Thus, the technology scaling effects for both HBM and CDM, as shown in Figures 1 and 2, would not have implications for system-level ESD.

2.4 ESD Control Programs

ESD control programs have been in place for many years. One of the earliest programs was implemented to help with the production of gunpowder. This simple program effectively kept the powder wet during manufacturing and handling. This kept the static charge low enough that the gunpowder would not ignite.

In the 1950s and 1960s, electronic devices were less sensitive to ESD events. The devices of the time could withstand most events without a problem. Even if the devices did fail for ESD events, the failures were a very small portion of the overall failure rates.

In the late 1970s, with the introduction of large-scale integration (LSI), ESD became a significant problem. A group of industry experts realized this and organized the first US ESD Symposium in 1978. Technical papers and workshops on problems and solutions were exchanged at the time. Companies also started to implement ESD control programs at this time. Each company had its unique program and did not share the information. The need for standardized programs was not recognized at that time.

The US Military was one of the first organizations to recognize the problems with static electricity and ESD. The first standard to address ESD process control was MIL-STD-1686, released in May 1980. This standard, along with its companion handbook MIL-HDBK-263, represented the first ESD control standard in the industry. All electronics suppliers to the military were required to comply with this standard. However, most of the private sector still followed the company-developed procedures. It should be noted that today, the US Military is using ANSI/ESD S20.20 for its ESD control program.

These early standards were focused on people and packaging. The controls in place for insulators were left mostly to the end-user without much consideration, except for the removal of non-required insulators. Tools, machines, and automated equipment were not addressed or considered, as most processes were manual. The basic instructions were to keep everything and everyone handling the devices at the same potential.

An additional issue with these early ESD control programs was that the materials used to control static electricity did not have standards to qualify the materials. This led to many different types of testing, different methods, and different instrumentation that caused different results. In some cases, materials measured by these methods did not perform well in controlling static. In the early 1980s, a professional association, EOS/ESD Association, Inc. (ESDA), was formed to resolve material testing issues. The first standards from the ESDA were simple material tests for items such as wrist straps, work surfaces, and flooring. The standards created a way to compare one product to another. Suppliers of these materials were able to use the standards to improve products. For example, the simple wrist strap has undergone many industry changes. What started as a simple metal bead band has evolved into a system that makes better contact with a person and, in some cases, allows for continuous monitoring. Wrist straps provide a much more reliable connection than before and last longer. The standards also provide a way to test the wrist straps consistently so that a wrist strap that becomes defective can be removed and replaced. Before this, materials were used until physically damaged without regard to its electrical properties.

In the 1980s and 1990s, the electronics manufacturing industry changed from each company having all manufacturing within the company to a model that included many contract manufacturers (CMs) or electronic manufacturing suppliers (EMSs). At the same time, the military and the European standard, CECC-00015:1991, were not evolving with technology and with changes in manufacturing supply chains. The standards were either too restrictive or did not address all aspects of a control program.

In 1995, the ESDA was tasked with replacing MIL-STD-1686 with an industry standard. The standard, ANSI/ESD S20.20-1999, replaced company-developed ESD process control programs. Following the release of this standard, a third-party certification program was established to demonstrate compliance with the standard and has been successfully applied to factory certifications worldwide, as shown in Figure 4. ANSI/ESD S20.20 has been periodically updated to keep pace with device technology, emerging information about ESD failures, and improvements in ESD control technologies and measurement methods, with the latest version being ANSI/ESD S20.20-2021 [2]. In parallel, the IEC has created and periodically updated a similar control document, IEC 61340-5-1 [3], which is technically equivalent to ANSI/ESD S20.20. There are also other standards, such as JEDEC JESD625, dealing with ESD control that are not technically equivalent.

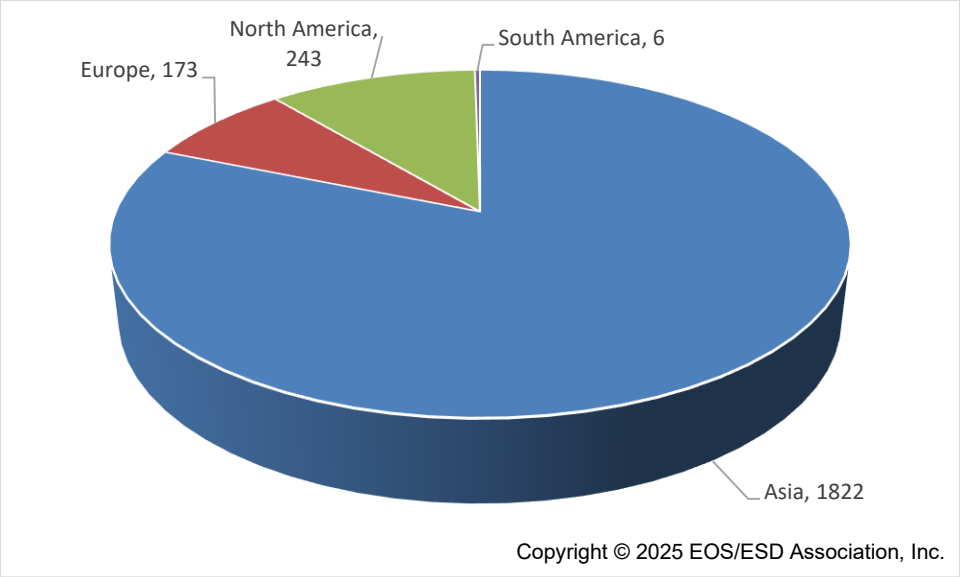

Figure 4: ANSI/ESD S20.20 Certificates Issued Through August 2025

2.5 ESD Stress in Processes

The ESD sensitivity trends discussed in Section 2.2 will significantly impact manufacturing process yields over the coming years. Companies must increase efforts to verify that processes can handle these devices and, where necessary, improve ESD control programs. This could include changes in the ESD control item limits, compliance verification frequency, and other ESD monitoring forms, such as ESD event detection.

Recently, the ESDA released a standard practice on ESD process assessment. ANSI/ESD SP17.1 [10] describes a set of methodologies, techniques, and tools that can be used to characterize a process where ESD sensitive (ESDS) items are handled. The process assessment in ANSI/ESD SP17.1 covers risks by charged personnel, ungrounded conductors, charged ESDS items, and ESDS items in an electrostatic field. The basic approach is to compare parameters measured in the manufacturing process, for example, an electrostatic voltage on an ESDS item, with the limits derived from the HBM or CDM robustness of the ESDS item. The procedures in this document are for use by personnel possessing advanced knowledge and experience with electrostatic measurements. Assessing the results from the measurements described in this document requires significant experience and knowledge of the physics of ESD and the manufacturing process.

2.5.1 Discharge of Personnel

It has been shown that for a person grounded by a wrist strap system, the person's resistance to ground is directly correlated to the maximum voltage on a person. Tests on a person wearing a wrist strap using standard shoes on non-ESD protective flooring have shown that a total resistance to ground through a wrist strap of 40 x 10^6 ohms or less is necessary to limit body voltage to less than 100 volts. 100 volts is the minimum HBM sensitivity of ESD sensitive (ESDS) items being handled in an ESD control program such as ANSI/ESD S20.20, and, therefore, the maximum body voltage of personnel handling ESDS items should be limited to below 100 volts. The testing was done by taking a wrist strap with a 1-megohm resistor in the cord and adding series resistance to the wrist strap system. The resistance was placed between the end of the wrist strap cord and the ground connection. Then the person wearing the wrist strap walked on the non-ESD floor while their voltage was measured. Figure 5 shows the relationship between the body voltage of personnel wearing standard shoes on a non-ESD floor connected by a wrist strap to ground as a function of the total resistance to ground through the wrist strap. The limit for wrist straps provided within ANSI/ESD S20.20 is 35 x 10^6 ohms, which is approximately a 10% safety margin.

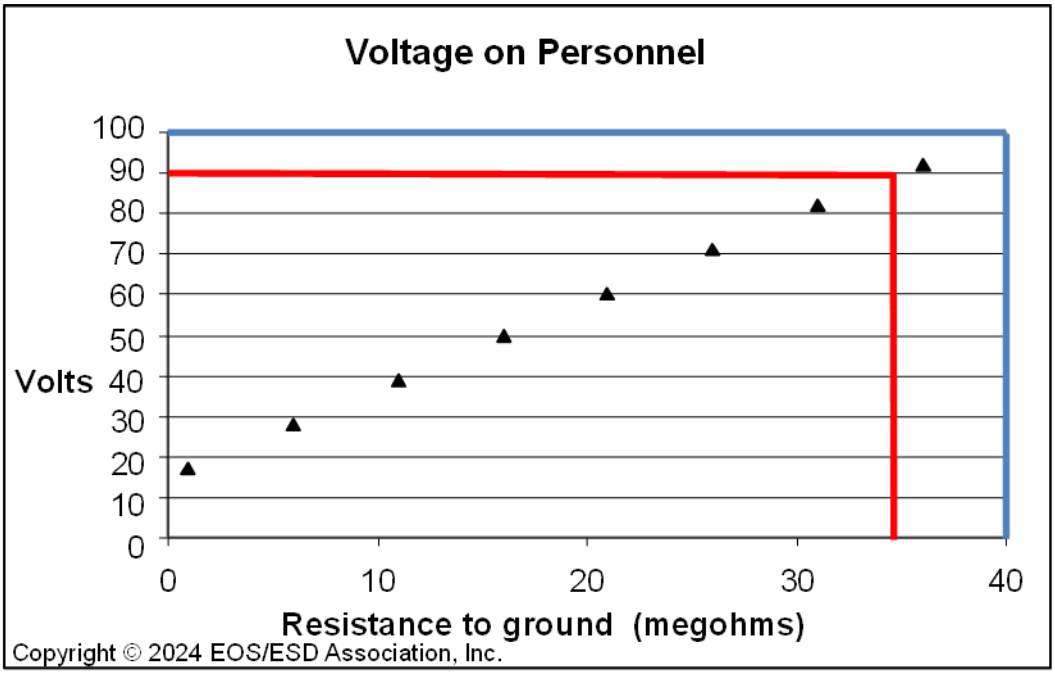

Figure 5: Relationship Between Body Voltage and Resistance to Ground [1]

NOTE: Red: body voltage limit of 90 volts for handling ESDS when grounded with a wrist strap according to ANSI/ESD 20.20. Blue: body voltage limit of 100 volts for handling ESDS when grounded with a wrist strap according to ANSI/ESD 20.20.

The situation is more complex for an ESD control program that uses a footwear/flooring system to ground personnel. As people walk across a floor while wearing footwear designed to keep personnel grounded, it is difficult to predict the voltage on a person's body due to the constantly changing body capacitance and the continuous charging and discharging of the person.

ANSI/ESD STM97.2 [11] can be used to determine the process capability of the footwear/flooring system. An example of the information provided can be seen in Figure 6.

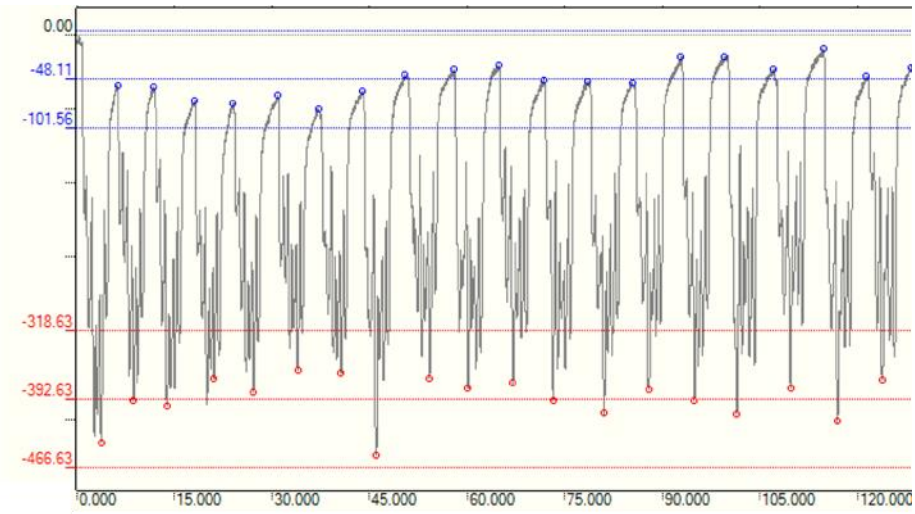

Figure 6: Determining Process Capability of a Footwear/Flooring System using ANSI/ESD STM97.2

2.5.2 Discharge of Ungrounded Conductors

When a charged conductor comes close to or contacts an ESDS item, a discharge can occur. If the ESDS item is grounded on at least one pin, the discharge was previously correlated with the machine model. If the ESDS is floating, the discharge scenario is best described with an CDM-like event. To minimize these discharges, ensure that all conductive surfaces that come into contact or proximity with ESD sensitive devices are grounded. If it is impossible to ground conductive surfaces, then measurements should be made to ensure that moving parts remain below a threshold voltage throughout the process. In ANSI/ESD S20.20, the threshold is defined at 35 volts.

CAUTION: THIS THRESHOLD LEVEL DOES NOT TRANSLATE INTO ANY MEASURED CHARACTERIZATION WITH AN MM TESTER. THESE MEASUREMENTS MUST BE TAKEN WITH THE PROPER EQUIPMENT, SUCH AS A CONTACT VOLTMETER OR A NON-CONTACT VOLTMETER. MOST ELECTROSTATIC FIELD METERS USED AS VOLTMETERS CANNOT MAKE THIS MEASUREMENT.

2.5.3 Events from Charged Devices and Static (Field) Induction (CDM)

In its pure form, a CDM event occurs when a charged ESD sensitive device is grounded or when a neutral device is grounded in the presence of an electrostatic field. A unique characteristic of these events is the involvement of a very fast rise time event between a device pin and another conductor at a different potential. CDM is the most relevant discharge model when single ICs are handled with automated equipment or manually using hand tools with conductive contact to the ESDS item. Thus, the CDM test method may also cover the more general cases of conductor-conductor discharges, such as touching a device lead with conductive tweezers. This includes many isolated conductor discharge events. An isolated conductor has no connection to ground or any other conductor.

Effective ESD control programs ensure that the voltage on an ESDS, either induced by process-essential insulators due to electrostatic induction or triboelectricity, is below a safe handling limit before contacting a conductive object. As CDM thresholds are lowered, it becomes more difficult to depend on voltage control alone to provide adequate device protection. Thus, it is becoming more important to eliminate conductor-conductor contact wherever possible and use dissipative materials to avoid hard grounding.

2.5.4 Charged Board Events (CBE)

ICs and other ESD sensitive devices remain at risk when mounted onto printed circuit boards and other assemblies. Evidence shows that many ESD failures in circuit and system assemblies occur at the board level. These types of failures are due to charged board events (CBE). Most ESD testing and characterization of devices are done on standalone parts. This type of data is summarized in the HBM and CDM roadmaps.

Further, IC failure analysis data, based on knowledge of failure signatures seen in standard HBM and CDM tests, has caused many to conclude that ESD failures are relatively rare compared to other electrical failures commonly classified as electrical overstress (EOS). Recent data and experience reported by several companies and laboratories now suggest that many failures previously classified as EOS may instead result from ESD failures due to CBE (or cable discharge events (CDE) discussed in the next section). A charged board stores more energy than a standalone part because its capacitance is larger. The charge (energy) transferred in the event may be large enough to cause EOS-like failures to the devices on the board.

Minimum robustness of boards against CBE is not defined in ANSI/ESD S20.20. It might be that significantly reduced maximum charging or discharge currents must be considered, accounting for the more severe discharge of a board compared to a single IC. For some guidance, see ANSI/ESD SP17.1 [10]. For facilities that find that they are handling parts with sensitivities below those stated in ANSI/ESD S20.20, more controls or tighter limits than those defined may be needed. However, in most cases, these practices and requirements should be sufficient for protecting circuit boards (PCBs). Problems do arise when specific program implementations do not fully comprehend PCBs as ESD sensitive items. In these cases, the risk of failure due to CBE may be significant. Identifying

CBE as the root cause of failure can be difficult. This may require conducting tests that can replicate failures due to CBE and distinguish them from other possible electrical stresses. Methods for conducting CBE tests have been developed in EOS/ESD Association, Inc. WG 25.0 (see Section 3.2.3).

2.5.5 Cable Discharge Events (CDE)

The insulation on a communication cable (USB, Ethernet, etc.) is easily triboelectrically charged by the movement of the cable over surfaces such as desktops, floors, clothing, and work surfaces. This charging will, in turn, induce a potential on the cable's conductors. When the charged cable is plugged into a system, an ESD event occurs between a cable conductor(s) and one or more of the connector pins of the system receptacle, depending on the connector design. This discharge is referred to as CDE. The resulting current pulse highly depends on the length, impedance, type of connector, and cable quality. Industry reports indicate that CDE can cause an interface device to be damaged, create a system "lock-up," or cause a system upset. CDE is generally considered a charge equalization process between the victim unit or device and a charged cable. A CDE can also occur if the victim unit (laptop, cellphone, etc.) becomes charged with respect to an uncharged cable. In the latter case, the victim unit becomes triboelectrically charged via contact with some material or via a charged person. Whether the cable is charged, or the victim unit is charged, the result is a discharge involving current flowing into or out of a cable. Like CBE, the root cause of damage to a device from a CDE may be misdiagnosed as coming from some other form of electrical stress. Methods for conducting tests replicating a CDE are under development (see Section 3.2.4).

3.0 TRENDS IN ELECTRICAL STRESS TESTING

Failure of devices due to a wide variety of electrical stresses is a major contributor to yield losses in manufacturing. ESD represents one category of such stresses that can cause large yield loss events and continuous background dropout. The HBM and CDM test methods have been the main enablers in the design of ESD-robust devices and are described in further detail in Section 3.1. These methods are often described as qualification methods because of the key role in the relationship between supplier and user. Stress tests can play other important roles, such as characterization or failure replication; these are discussed in Section 3.2.

3.1 Device-Level ESD Qualification

As described previously, decreasing ESD thresholds will put more pressure on the ESD control program to maintain high yields. To know where special procedures and scrutiny are required, one must know the device's susceptibilities. With pin counts increasing and pin spacings decreasing, evaluating device ESD thresholds has become more challenging. As a result, the HBM and CDM test methods have continued to change, and additional changes are anticipated to track increasing device complexity. The increasing test costs and time drive changes in these methods as well.

ESD control programs, such as ANSI/ESD S20.20, include minimum HBM and CDM levels in their scope, defining the ESD robustness range covered by the document. This suggests that additional controls may be needed for high yield for devices with lower ESD robustness. Some organizations, such as the US Military and private companies, use the HBM and CDM classification levels in ANSI/ESDA/JEDEC JS-001 [13] and ANSI/ESDA/JEDEC JS-002 [14] to add further granularity to an ESD control program. HBM and CDM voltage and current threshold levels are used for process assessment, as described in ANSI/ESD SP17.1. Most significantly, device users and suppliers in the electronics industry use the thresholds obtained from HBM and CDM testing as part of the larger set of technical requirements for qualifying a device. For example, JEDEC JESD47 [12] includes the requirements for HBM and CDM testing. As a result, these methods are often referred to as qualification test methods. It is also important to note that, unlike most other tests required for qualification, ESD testing and threshold assignment cannot be done on a technology, family, or package basis. Given the important role played by these tests in nearly every new design, considerable effort has been made to provide reproducible, reliable, and efficient methods. Details and trends for these methods are described below.

3.1.1 Human Body Model (HBM)

In 2010, the ESDA and JEDEC HBM test methods were merged into a single document designated as ANSI/ESDA/JEDEC JS-001-2010. The latest release was in 2024. Since its initial release, many changes have been made to address testing concerns with new device technologies, larger device pin counts, and possible tester interactions that could affect testing results.

Changes were made to minimize wear-out concerns from over-stressing by minimizing the stress combination, allowing the use of sampling methods for signal pins, and recently for power pins.

Recent changes included the following items:

- Introduced an alternative decay time calculation method.
- The exposed pad has been defined as a pin and shall be stressed according to its classification. The implications of this may require new hardware on the HBM tester to support the testing.
- Full allowance to stress parts on a package, die, or wafer.
- Addition of an annex on optional pre-HBM current spike detection equipment.

A true statistical sampling scheme standard practice has been developed to reduce the overstressing of pins relative to real-world environments without compromising the threshold assessment of the product. A similar statistical approach has been used to develop random testing combinations for supplies having resistance between pins higher than 1 ohm and lower than 3 ohms to allow test time reduction using a two-channel simulator. The HBM User Guide ESDA/JEDEC JTR001 has been completely revised to include the new allowances introduced over the years and will be published soon. Focus for the next full release will be on harmonizing the document and a few other allowances.

3.1.2 Charged Device Model (CDM)

CDM continues to be recognized in the electronics industry as the primary real-world ESD model for assessing ESD risk in automated IC handling and manufacturing worldwide. CDM ESD must consider the scaling of the device process – IO pin technology, scaling down of minimum device size – pin pitch achievable in test, and CDM tester metrology limitations in consideration of the CDM roadmap direction over the next five years.

3.1.2.1 Device Thresholds

The continuing trends of integrated circuit process technology advances, increasing package size and complexity, and increasing IO performance requirements all point to lower minimum charged device model withstand thresholds, especially for the high-performance pins. These trends will result in a larger percentage of high-performance pins on products forecasted to be below 125 volts by 2030. These pins may only comprise a small fraction of the total number of pins in any one package.

3.1.2.2 Package Size/Pin Pitch

Two package-related limiting factors to CDM testing are the minimum package size and pin or ball pitch (distance between pins/balls on a package type). Minimum package x-y dimensions in 2020 were on the order of 400 µm by 600 µm, and this is expected to pose a challenge to small package testing looking out to 2030. A pin pitch of 350 µm (the minimum achievable by CDM testers in 2020) will not allow testing for packages with smaller pin pitch (including bare die pad spacings) for today's pogo-style discharge pin/ground plane style CDM probe assemblies. Thus, future CDM test capability requires probe technology like automated test equipment (ATE) for those die-form products.

3.1.2.3 CDM Testing Methodology

Three methods of CDM testing are available today. The first method, field-induced CDM testing, is used by over 90% of the electronics industry. This is widely based on the harmonized ANSI/ESDA/JEDEC JS-002, published in 2015 and updated in 2025 [14] and its associated user

guide published in 2022 [15]. This harmonization has helped the industry to standardize on a single field induced CDM test platform, but it is still limited. These limitations include the minimum device size and pin pitch physical limitation of the CDM test equipment (which leads to multiple pin discharges for very small pitches), as well as the environmental variation of the discharge peak currents caused by the air discharge, which is dependent on device size, charge voltage, and relative humidity.

The continued reduction in minimum CDM pin thresholds described limits the use of field induced CDM for many devices due to the increased variation in the discharge waveform at low voltage levels. An alternative CDM testing method, low impedance contact CDM (LICCDM), has been shown in early trials to achieve a more accurate discharge pulse, independent of humidity and the varying characteristics of the discharge spark in the field induced CDM event. Research in approximating the impedance of the field-induced discharge spark with a discharge impedance in the contact CDM metrology chain (through the transmission line and relay switching) has shown significant promise to provide repeatable, reproducible discharge waveforms below 50 volts with no humidity dependence. A standard practice [16] was published in 2018, describing this new test method. Testing using this method is expected to yield more accurate CDM testing at lower voltage levels for those devices needing it. This contact approach also eliminates some of the challenges of testing smaller packages/pin pitches by allowing a sharper pogo tip to be used.

A second alternative CDM test method (capacitively coupled TLP (CC-TLP)), which also uses a contact approach, has been investigated. The standard practice [17] was published in 2022, describing this test method. CC-TLP systems have been used much longer than LICCDM and have shown a good correlation with CDM results in many studies. The limitation of being unable to completely match the field induced CDM discharge waveform due to the higher source impedance can be compensated by a shorter pulse width. Thus, CC-TLP is also being considered as a possible wafer-level characterization technique for die-to-die interfaces that would give important information on protection structures before any packaging and could be used as a solid figure of merit at the wafer level to compare the ESD robustness of various protection structures. This is also a potential solution for the characterization of chiplets that are used to enable more complex package systems.

Currently the WG is working on a Round Robin (RR) to elevate CC-TLP and LI-CCDM SPs to STM. Despite that they cannot match 100% FICDM results, they will be the only solutions for testing at voltages below 100 V and small form-factor packages (including die).

3.2 Characterization and Replication Methods

Stress tests can play other important roles, such as characterization or failure replication. Characterization using TLP gives ESD protection designers an early indication of the electrical response to ESD-like pulses, informing the ultimate protection strategy. Electrical stress tests can also aid failure analysis and root cause verification and provide comparative evaluations of corrective actions. These can be described as stress replication tests. The tests include transient latch-up (TLU), variations of CBE and CDE stresses, and other unintended electrical stresses. These non-qualification methods are discussed in more detail. In the future, some stressing methods may become widespread and reliable enough to evolve into acceptance or compliance tests. Currently, none of the methods are in that category.

3.2.1 Transmission Line Pulse (TLP) Characterization

The TLP method is the de facto standard method for ESD characterization of standalone devices/components and pins of ICs. ANSI/ESD STM5.5.1 [18], fully revised in 2022, is the basis for this work and covers transmission line-based quasi-static characterization with pulse widths in the range of single nanoseconds to several microseconds and appropriate rise times. The User and Application Guide, ESD TR5.5-04-22 [19], provides additional information on the practical use of TLP systems and is updated regularly.

Technical report ESD TR5.5-05-20 [20], released in 2020, addresses using TLP systems for non-quasi-static analysis. The working group has started working on a standard practice, advising on

the best-known practices for measurements to support the analysis of the device response to fast transients, such as during CDM or system-level stressing.

With the increased use of automated TLP systems, collecting sufficient data for a statistical analysis becomes feasible. Therefore, the working group started compiling a technical report on using TLP to statistically characterize device behavior under ESD conditions. Examples are methods to characterize the distribution of parameters such as trigger voltage, failure current, and oxide breakdown voltage.

The increased usage of TLP and the use of the results for developing ESD models for the SEED method [6,9] suggests the development of a definition of a (minimum) standard way of characterization and reporting for such applications. This may lead to a new technical report or user and application guide update. Finally, the working group may investigate the need to extend the pulse width range and rise time range of the TLP methods.

3.2.2 Transient Latch-Up (TLU) Replication

Integrated circuits can contain latch-up sensitive structures (such as parasitic thyristors), which can cause reliability issues during operation. For this reason, most semiconductor devices must be qualified to a respective latch-up sensitivity. JEDEC JESD78 [21] is the most used latch-up qualification standard. However, this test has a rather slow rise time and long trigger pulse, which does not cover many latch-up events. It is well known that fast transients, such as ESD, can trigger latch-up more efficiently.

Per the "static" JEDEC JESD78 latch-up standard, the ESDA WG 5.4 (Transient Latch-up) defines transient latch-up as a state in which a low-impedance path resulting from a transient overstress that triggers a parasitic thyristor structure or bipolar structure or combinations of both, persists at least temporarily after removal or cessation of the triggering condition. The rise time of the transient overstress causing TLU is faster than 5 µs.

In 2014, to address industry needs, ESDA WG 5.4 started a new standard practice on TLU, which defines a universal TLU methodology that can be used for replicating transient effects seen in the field. The proposed TLU trigger pulses, and the setup can be modified to match a specific application's requirements and constraints. The methodology can be applied to various applications, from simple test structures and discrete semiconductor devices to complex integrated circuits as standalone devices or systems. The proposed methodology can reproduce all TLU events discussed in ESD TR5.4-04-13 [22]. An important building block of the document is the verification methodology of the TLU setup, which ensures a correct pulse delivery to the device under test and a sufficiently fast response from the power supply. ESDA WG 5.4 released ANSI/ESD SP5.4.1 in 2017 [23], reaffirmed the document in 2022.

It must be emphasized that the TLU test methodology proposed in the standard practice is not intended to be used as a qualification methodology, in contrast to the static latch-up test JEDEC JESD78, a mandatory device qualification test. The TLU methodology can be applied to pins, which might be endangered by fast transients in the field, to replicate certain types of electrical overstress. It intends to cooperate closely with the JEDEC JESD78 working group, as both standardization committees face similar technical challenges. The relevance of TLU compared to purely "static" latch-up will certainly increase in the future, according to JEDEC JESD78. Therefore, a close link between the JEDEC JESD78 WG and ESDA WG 5.4 is planned.

3.2.3 Charged-Board Event (CBE) Replication

ESDA has published a technical report, ESD TR25.0-01-16, giving general information about CBE phenomena [24]. ESDA has also published a second technical report, ESD TR25.0-02-23, that guides the industry in replicating CBE threats [25]. It contains examples of how to set up a CBE test bench, carry out testing, and report test results. The document also contains information on estimating CBE stress levels based on calculated and simulated data. ESD threats due to CBE are case-specific, and the technical report does not contain acceptance or target levels for CBE stress. Instead, it instructs how the user can specify the target level and estimate ESD risks based on the observed discharge waveforms in the process area and on the test bench.

3.2.4 Cable Discharge Events (CDE) Replication

ESDA WG 14 (System Level ESD) has collected data on real-world CDE events, gathering relevant information from case studies, publications, and industry inputs to create a well-defined test method. This test method is intended to help guide the industry to allow reproducible testing against CDE threats and to help determine the CDE immunity of a system, such as a laptop or handheld device (phones/cameras, etc.). While gathering this data, it became apparent that cable discharge events may only be one of many "events" that may cause operational system failures or hardware failures on individual devices.

Cable discharge events can occur when a charged cable by itself discharges into a system or when a cable attached to another item (which adds additional capacitance) discharges into a system. This discharge can occur between the shell of the cable and the connector on the system or directly between the cable's pins and the pins on the connector on the system. This direct discharge between the cable's pins and the system connector would be a "direct pin discharge". However, this test is not recommended within widely used system level test methods.

The number of variations in discharge events has made it difficult to establish a single representative waveform for a test method. The WG will focus on developing a technical report that will provide information to the industry on the different direct pin injection types, including CDE events. The report will show different levels of events based on cable types for CDE events while offering insight to system designers on possible design and protection recommendations for CDE and other direct pin injection events. The WG has written multiple articles on CDE with an emphasis on educating the industry about CDE but also as a way of gathering information from sources outside of the committee.

3.2.5 Replication of Other Electrical Stresses

The development of defined methods for replicating other electrical stresses is also interesting. This arises from the industry-wide initiative to reduce device failures, often characterized as EOS [26]. The main challenge is to find a way to reproduce a wide range of possible stresses systematically. WG 23 collected data and industry practices for producing these stresses based on waveform characteristics and other environmental factors and published it in a technical report [27].

4.0 TECHNOLOGY OUTLOOK

This section focuses on the drivers of the technical advances in the semiconductor industry until 2030. The scaling of CMOS technologies continues, and significant advances in packaging will happen. Another driver will be the broad use of III/V compound semiconductors, particularly in energy conversion and communication. This includes the application of photonic technologies to enable the required huge data bandwidths of the digital society.

4.1 CMOS Technology Scaling – What Comes After FinFET

Soon, the core device architecture will change from FinFET to new device architectures like gate-all-around field-effect transistors (see Figure 7) [28]. This technology scaling also requires new materials and interconnect schemes, such as backside power delivery networks. These changes will impact both ESD and latch-up protection design. Previously unknown technical limitations in ESD and latch-up protection design could be reached. Implementing ESD and latch-up protection designs at the product level will be more challenging. Because of the complexity of these highly scaled technology platforms, developing and using 3rd-party IP is essential to enable ESD and latch-up robust products in these very advanced technology nodes cost-efficiently.

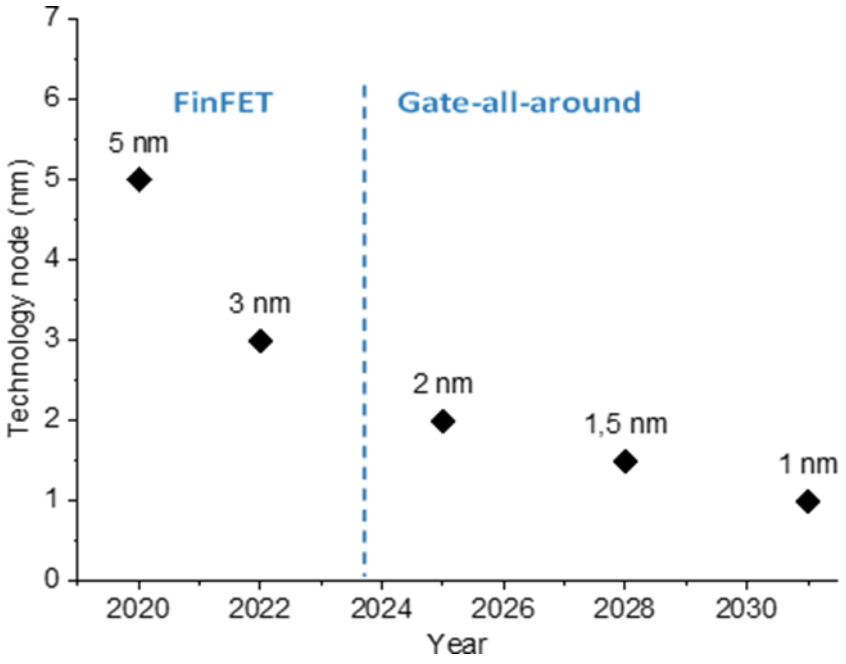

Figure 7: Roadmap for Logic Device Scaling Until 2031

4.2 Sub-10 nm Technologies for Automotive Applications

It is predicted that the value of ICs in the car will increase at a compounded annual growth rate of ~7% out to 2030. The value of ICs increases even more in electrified vehicles. This growth in semiconductor content in vehicles is caused by four major trends: electrification, autonomous driving, connectivity, and shared mobility. Besides efficient power conversion, next-generation cars will need much more computational power, enabled by highly scaled CMOS technologies.

The semiconductor industry has long-term experience using highly scaled technologies like FinFET for consumer electronics applications and products. A strong ecosystem of semiconductor foundries, IP block providers, and IC manufacturers has been established and supports the use and further scaling of these technologies. In the automotive industry, autonomous driving and connectivity, particularly, can only be enabled by using these advanced technologies. Advanced driver- assistance systems (ADAS), microcontrollers, and microprocessors are typical applications.

The high-reliability requirements of automotive applications conflict with some of the physical limitations of highly scaled technologies. This also opens new challenges for ESD and latch-up protection design because consumer-grade protection solutions must be adapted to the higher requirements of automotive applications. This can lead to some designs not meeting the higher automotive reliability requirements. Data in White Papers 1 and 2 [1, 5] of the Industry Council on ESD target levels, advances in ESD control, and experience in the consumer market have led to a re-evaluation of the ESD target levels in the Automotive Electronics Council (AEC). For high-speed pins and sub-28 nm technologies the same levels as in the consumer market are now adopted and a reduction of the ESD target level has been added in AEC Q100 Rev. J [29], along with a an associated expectation of improved ESD control throughout the handling and assembly of such components as, for example, described in ANSI/ESD S20.20. The same counts for latch-up design and testing, where much lower supply voltages and currents and high-temperature profiles bring additional challenges.

4.3 Advanced BCD Technology Trends

Bipolar-CMOS-DMOS (BCD) technologies have experienced remarkable growth in recent years. Several key factors are driving this innovation path, such as the increasing diffusion of electric

vehicles (EVs) and hybrid electric vehicles (HEVs) [30], the rapid spread of smart devices and IoT applications, and the strong push for energy-efficient solutions. These trends in the applications are reflected in a continuous advancement in process technology, which is characterized by several factors:

- Improved power density and reduced power consumption, which is addressed with innovative and customized MOS architectures.
- Higher digital complexity and larger embedded non-volatile memories, requiring the adoption of advanced lithography nodes (40 nm and beyond).
- A strong focus on higher voltage ranges (above 100 volts) to implement dedicated power management integrated circuits (PMICs) for automotive and industrial fields.
- The development of innovative packaging technologies to allow system-in-package integration, combining BCD integrated circuits with large power transistors (for example, SiC or GaN power MOS) and passive elements (capacitors and/or inductors).

Each of these trends is then associated with different ESD challenges. The innovative high-voltage and high-power transistors recently developed are characterized by the usage of custom solutions (for example, poly and/or metal field plates, stepped oxides, mixing of different isolation strategies, etc.), which makes these transistors potentially more prone to snapback effects, thus limiting the ESD window. Moreover, the close control on the gate parasitic capacitance, needed to realize high-efficiency design solutions, makes implementing ESD active clamps more complex.

The increased digital complexity and the usage even in advanced BCD nodes of multi-domain architectures, mixing digital and precise low-voltage analog blocks, will surely impact the CDM robustness of future BCD ICs, thus leading to a potential reduction of the reachable CDM target levels.

New applications in the high-voltage range above 100 volts will require a careful design of dedicated CDM protection, as the ESD diodes in this regime are strongly impacted by physical effects as the forward recovery effect, which makes them intrinsically slow and therefore more exposed to voltage overshoot in the sub-ns time scale.

Finally, the evolution of system-in-package solutions will require close control of inner nodes, especially when large power transistors are used. These power MOS may have a large parasitic capacitance, which therefore may represent a potential threat for the driver IC, usually designed in BCD technology. The definition and characterization of the correct ESD robustness level of these internal nodes, needed to implement an effective and at the same time robust application, is therefore going to be a very critical factor.

4.4 Heterogenous Integration and Advanced Packaging

Heterogeneous integration is the process of separating the functionality of a system onto separate dies that may come from different technology nodes and even materials and then connecting these in a single package. The individual dies in such systems are also known as chiplets. Both lateral connectivity (2.5D IC stack) and vertical connectivity (3D IC stack) are used (see Figure 8). Advanced packaging refers to the technologies that enable heterogeneous integration and are a combination of technologies to enable cost, performance, power, and size-optimized interconnection of ICs. It also includes supporting elements to each other and the system, including flip chip, wafer, panel-level packaging, and interposer with and without through silicon vias (TSV) [31]. TSV establishes the electrical connection from the bottom to the front side of a die.

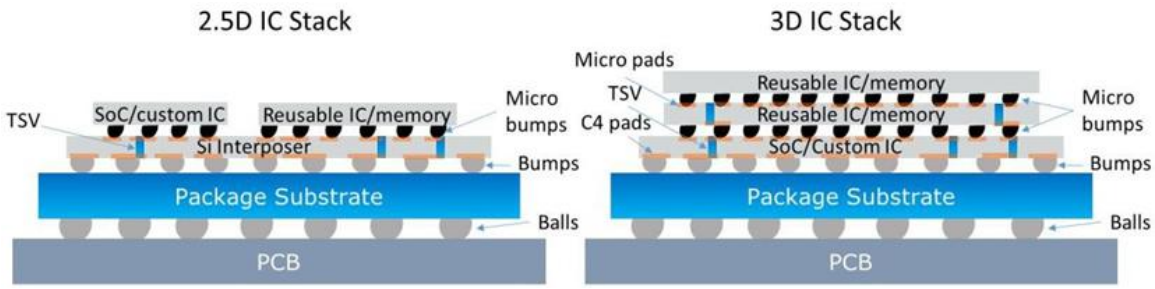

Figure 8: 2.5D Stack (left) and 3D Stack (right) ICs

The ESD challenges associated with these advances in packaging technology are directly related to the shrinking of the technology nodes, along with the associated increasing number of microbumps or hybrid bonds that exist on the chiplets. **It is expected that by 2030 and beyond, the minimum pitches for hybrid bonds will be 10 µm or less** [32], leaving little real estate for ESD control circuits. This is driven by the need for increased bandwidth and signal speed of high speed SERDES applications. A chart showing the relationship between bandwidth density and signal speed to bump pitch is given in Figure 9 (from [31]).

Generation Number →		1	2	3	4	5	6	7	8
Raw Areal Bandwidth Density (GBps/mm^2)[15, 24]		125	250	500	1000	2000	8000	32000	200000
Package Technology	Minimum Bump Pitch (µm)	40	30	20	15	10	5	2.5	1
	Areal Escape Density (IO/mm^2)	625	1111	2500	4444	10000	40000	160000	1000000
Signaling Speed (Gbps)[25]		1.6	1.8	1.6	1.8	1.6	1.6	1.6	1.6

Figure 9: Physical IO Scaling Roadmap for 3D Architectures that Use Both Solder and Hybrid Interconnects

The increased signal speed required for these advanced applications and the reduction of bump pitch will significantly impact the level of ESD protection that can be placed on each microbump or hybrid bond. In addition, both the supply and breakdown voltages of the advanced technology nodes are decreasing. The typical breakdown voltage for the 2-nm transistor is around 3 volts. This reduction of breakdown voltage is part of the reason for the reduction of the CDM targets (see Figure 10) since the expectation is that little to no explicit ESD control circuitry can be implemented. With a hybrid bond pitch of 10 µm or less, there is very limited space for even small ESD diodes. For these interfaces, whatever ESD withstand protection may need to be provided by “ESD hardening” design practices. This refers to applying appropriate circuit layout practices to allow the circuit to withstand the current transients associated with the expected CDM threats.

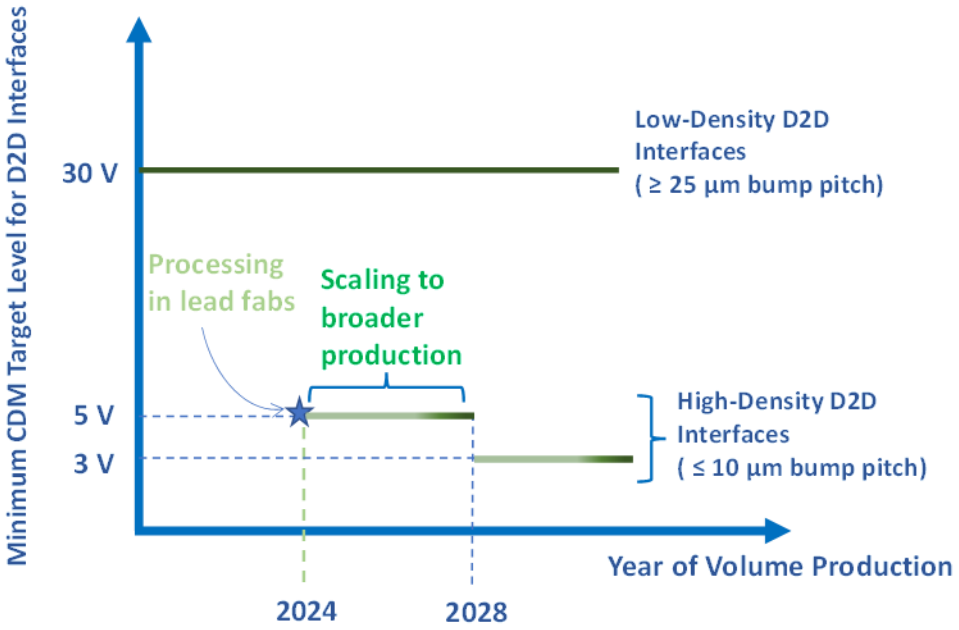

Figure 10: Roadmap of CDM Targets of Die-to-Die Interfaces [32]

Another aspect of the ESD roadmap for heterogeneous integration and advanced packaging is the miniaturization of the substrate or interposer technology. The expectation is that by 2030 and beyond, a 1-µm line and space (L/S) will be in use (see Figure 11). In addition, there will be increased passive device integration into substrates. While this will increase the ESD sensitivity of the substrates themselves, the largest impact may be the threats to the chiplets being stacked. With an increased number of passive devices such as capacitors and inductors, the substrate may become an increased threat as an ESD aggressor in the packaging assembly process.

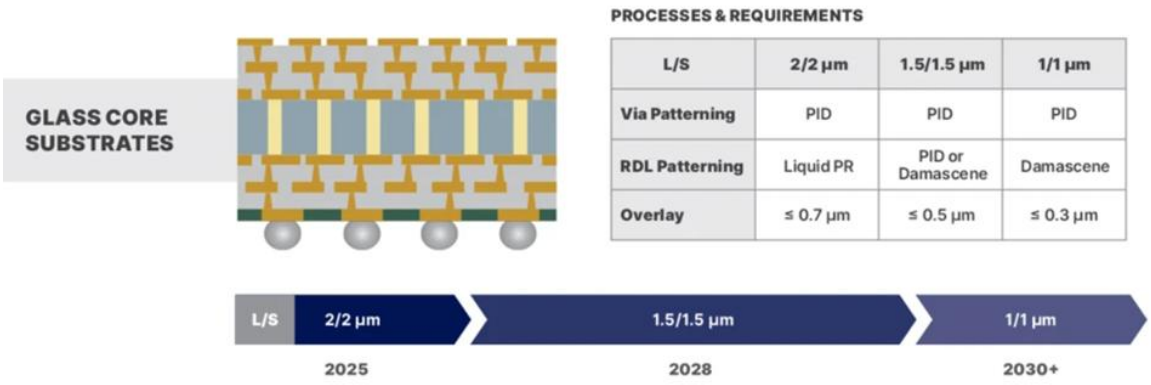

Figure 11: Industry Roadmap for Transition of Substrates from Organic to Glass and Path to 1 µm L/S

Assembly facility ESD process control capability is a final consideration for advanced packaging manufacturing. With a CDM target level capability of 3 volts to 5 volts for 2030 and beyond, the portion of the assembly process that handles these very sensitive components will require enhanced ESD controls. A thorough process assessment of the ESD control capability of the facility

will need to be completed to verify that the facility is capable of handling these extremely sensitive ESD parts. ANSI/ESD SP17.1 provides the framework for such an assessment.

4.5 Gallium Nitride for Power and RF Applications

The acceleration of gallium nitride (GaN) technology over the last two decades continues to exceed predictions. The applications driving this technology are wireless communication and power conversion. These are also key to energy conversion in electric vehicles. As these GaN technologies mature, the importance of ESD solutions to enable large-scale manufacturing will increase. State-of-the-art GaN technology is built on Si substrates, taking advantage of the mature manufacturing infrastructure in silicon fabs. These state-of-the-art technologies will also allow the design and manufacturing of GaN ICs where commonly used ESD target levels must be met. This will also require designing and developing ESD protection circuits for GaN ICs.

Different challenges lie in the use of discrete GaN components. In an industry survey in 2021 [33], ten different GaN semiconductor suppliers provided ESD ratings for selected components, including RF and power transistors. The ESD ratings included several parts with very sensitive ESD ratings of Class 1a (250 volts < 500 volts HBM) and some with high ESD ratings (> 2 kilovolts HBM). This highlights the challenges in meeting safe manufacturing levels for discrete GaN transistors. The GaN devices can withstand high voltage but have little avalanche current robustness. Discrete (non-integrated) GaN FETs have weak, exposed gates and no ESD capability [34, 35], causing erratic system behavior and device failures. Monolithic integration of GaN drivers [36] and the multi-chip module integration of silicon drivers with GaN FETs in a single package have the opportunity for much higher final product ESD robustness.

4.6 Photonics

Silicon photonics technologies (SPT) are widely used for high-bandwidth signal transmission between chips. Emerging architectures such as co-packaged optics (CPO) and optical I/O aim to further shorten electrical paths through highly integrated assembly, enabling even higher bandwidth delivery with improved energy efficiency (measured in pJ/bit) and reduced capital expenditure (in $/Gbps) compared to traditional pluggable optics, as shown in Figure 12 [37].

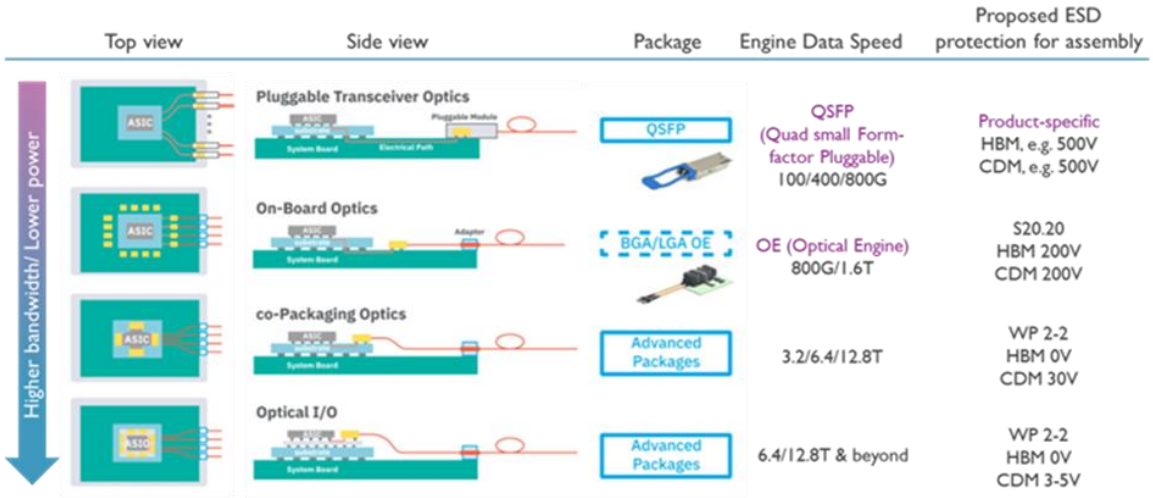

Figure 12: The Evolution of Optics Integration [37]

In these advanced architectures (based on 2.5D and 3D heterogeneous packaging), the key photonic components (lasers, modulators, photodetectors, and waveguides) are co-integrated with CMOS logic or driver chips. Among these components, the laser acts as the light source that carries modulated signals; the modulator converts electrical signals into optical signals, while the

photodetector performs the reverse operation by converting optical signals back into electrical form. This process is illustrated in Figure 13. These components are typically fabricated using silicon-on-insulator (SOI) technology.

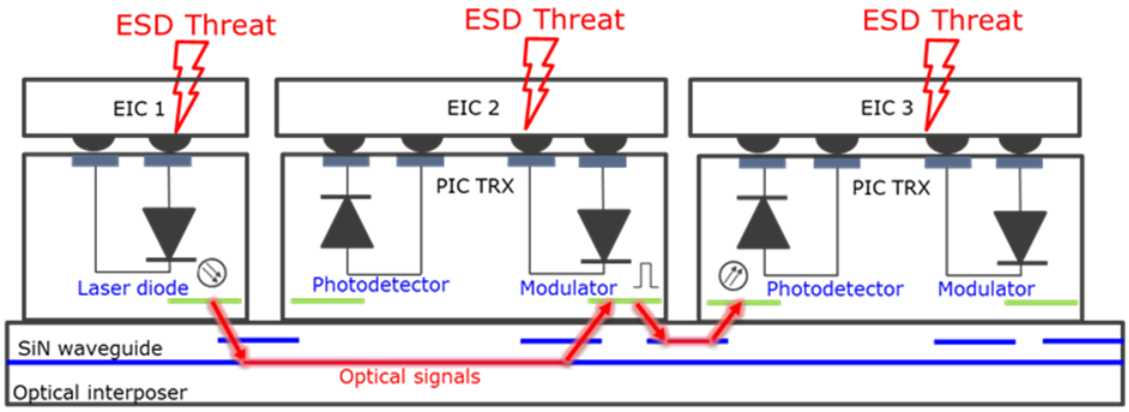

Figure 13: Schematic of Optical Interposer Functionality Containing Laser, Modulator, Waveguide, and Photodetector With ESD Threat at Bond Pads

In CPO and Optical I/O systems, silicon photonic components such as lasers, modulators and photodetectors are integrated closely with electronic chips. These sensitive photonic elements are susceptible to ESD events during assembly and packaging, particularly at the bond pads where electrical connections are established. The very high data rates of these applications [38] limit the capacitance budget of the pads, making ESD protection especially challenging, as photonics devices typically offer low self-protection. As optical packaging continues to evolve, ESD targets in silicon photonics must align with advancements in heterogeneous integration and advanced packaging technologies.

5.0 COMPUTATIONAL METHODS OUTLOOK

This section focuses on some of the drivers for ESD computational methods. First, there are EDA tools for design verification. Another driver is new machine learning methods. Finally, there is SPICE modeling for ESD design. To give a general overview as a starting point, the history and roadmap of all these different drivers for ESD computational methods are shown in Figure 14.

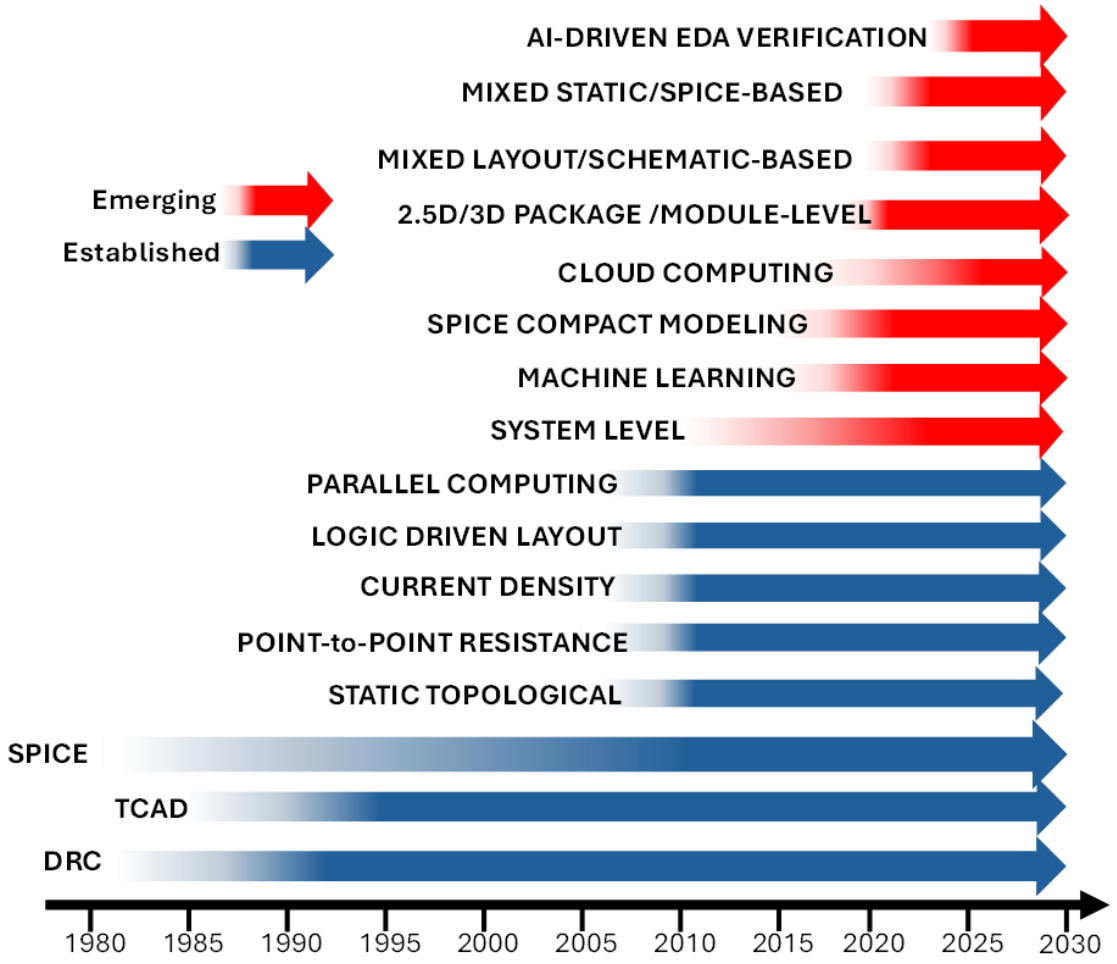

Figure 14: History and Roadmap of Electronic Design Automation (EDA) Tools

5.1 Electronic Design Automation (EDA) Tools

Verifying the ESD protection design of a complex IC design with many supply domains and voltage levels, various functional parts (RF, digital, analog), mixed-voltage circuitry, and advanced packaging will remain a challenge and a driver for the development of new EDA tool capabilities [39]. A few EDA tool areas are expected to experience significant development in the next five years. One of these areas is ESD EDA verification based on layout-extracted netlists. Layout-based netlists bring computational challenges since these netlists are significantly larger than the ones based on schematics views and are often only available late in the design cycle. The EDA industry approaches these challenges by introducing parallel, cloud computing, and hardware acceleration (xPU) to execute these checks. Sometimes, breaking the separation between layout-based and schematic-based verification may be necessary. Layout-based information such as parasitic ESD routing resistances and inductances can be extracted from partial layout and introduced inside schematic netlists for a more accurate evaluation of ESD voltage drops in a pure topological environment (arrow named "MIXED LAYOUT/SCHEMATIC-BASED" in Figure 14). These implementations will help to get an effective ESD verification process by using verification as much as possible during the design phase.

2.5D/3D packaging and module-level ESD verification have rapidly become another concern. Conventional ESD EDA tools are IC-focused, and each die technology tool needs a complex setup. A common format or syntax to set up verification tools is encouraged to improve the ease of use when dealing with complex IC die, packages, and modules involving multiple technologies and

EDA tools. EDA tools assist in the design of packages, dies, interposers, and modules. An ESD specification format is necessary to establish seamless communication and set-up of the various ESD EDA verification tools using common netlists and pin/pad definitions.

Some initial efforts exist to formalize and unify the need for this additional information across EDA tools like the joint project from ODSA and JEDEC-JEP30 with CDXML [40] and other industry efforts, like 3Dblox Standard [41]. The ESD community will benefit from an open format as it should simplify the manual setup task for flows and EDA tools that require this additional information. Each EDA tool will ideally also support such a format to easily automate a major part of the setup needed for verification tasks so that a single input file can be leveraged across multiple foundries and used in multiple EDA tools.

The boundaries between static and dynamic ESD verifications are disappearing. Existing ESD current density and point-to-point resistance analyses rely on simulation techniques. Full-chip static topological check analyses can be used to create relevant SPICE netlists for complex ESD protection scenarios such as power domain signal crossings. Simple SPICE simulations can be integrated into topological EDA checks to better assess the severity of reported violations (arrow named "MIXED STATIC/SPICE-BASED" in Figure 14). Another development area is to minimize any manual inclusion of initialization information necessary to enable the verification runs, for example, pad functionality definition, ESD stress requirement per pad, and pins' absolute maximum ratings (AMRs). Moreover, ESD EDA verification flows become more complex, containing sets of heterogeneous rules grouped in different tools (commercial and in-house) and applied to objects like IC schematic, IC layout, package view, etc. There is a rising need to align the ESD verification environments to reach homogeneity and considerably improve usability.

In addition, broad-range artificial intelligence (AI) is expected to become an important player in ESD EDA verification within the next five years (arrow named “AI-DRIVEN EDA VERIFICATION” in Figure 14), addressing, for example, support in rules coding or assistance in fixing complex violations. Applications of AI tools have the potential to bring more efficiency and ease-of-use to ESD designs and verification. This is an area where research needs to be pursued.

5.2 Machine Learning for ESD Data Analysis

The design and analysis of ESD protection for IC reliability are often done with well-established methods. Various ESD pulses are applied to IC devices for testing. However, the analysis of test results is time-consuming. Although some semi-automated test methods have been developed during the last decade, ESD reliability evaluations still involve highly skilled and senior experts to assess the true impact of the results. Therefore, machine learning applications could be desirable to bring more efficiency to ESD data analysis. The motivation is to develop machine learning approaches that can be implemented during ESD testing, data analysis, and the qualification process. These new paradigm-shifting approaches would appeal to the IC industry in dealing with the cumbersome ESD evaluation and in reducing uncertainties of the results. As observed in other fields, the first challenge could be creating an open ESD test results dataset to let academics develop and optimize their models.

Machine learning is expected to take place in two or three different aspects. The first one is diagnosing any failures at the first indication of symptoms and avoiding duplicate tests to uncover the same issues. The urgent need comes here to learn how to interpret the data. As the next step of this analysis, efficiency can be realized by applying machine learning to functional parameter shifts. The benefit from this type of practice would have tremendous potential and appeal.

The second application for machine learning would be IC ESD protection design implementations. This would require establishing certain rules known as "ground truths". The patterns are noted after observing a vast amount of data from ESD testing methods. The learning process will rely on identifying these symptoms with the next ESD data analysis. Once machine learning can identify the root causes with the defined ground truths, it can speed up the data evaluation process. In this manner, the engineer recognizes patterns faster and avoids repeating tests for the same symptoms since the root causes are already addressed.

The third application would be in SPICE modeling for ESD simulation [42]. The method can simplify model development and generate behavior models in less time than traditional modeling

approaches. It should be especially suitable for cases where physics is not fully understood or difficult to describe by traditional modeling equations. To fully take advantage of this new modeling approach, it is necessary to find ways to reduce computing power and memory needed in model training and CAD implementation.

5.3 SPICE Modeling for ESD Design and Verification

SPICE-based circuit-level simulation is one of the foundations of modern IC design. Efforts to apply SPICE simulation to ESD design and verification have existed for decades. The earliest literature reports appeared in the 1980s when device engineers began creating protection structures to address the emerging ESD problems in the electronics industry. However, up to today, trial-and-error or cookbook approaches based on prior art still dominate ESD protection design. Commercial EDA tools developed in recent years for ESD design verification have mostly focused on design rule check (DRC) and static analysis. Device compact models are the backbone of SPICE simulations. The lack of accurate and easy-to-use ESD-capable compact device models has prevented ESD simulations from widespread acceptance.

As ESD protection becomes more challenging in advanced technologies, it becomes a more urgent need to have SPICE simulation in ESD protection design and verification, just like in the regular IC design. ESD-capable compact models constitute the backbone of SPICE ESD simulation. These must be able to reproduce device behavior under high current and high voltage conditions beyond the normal operating region. Snapback in silicon-controlled rectifiers (SCR), bipolar transistors (BJT), and MOS devices is the most important effect of a SPICE ESD simulation. No industry standard models can reproduce the snapback phenomenon in SPICE simulations. Therefore, developing customized device models to include the snapback effect has been the focus and one of the most challenging tasks in ESD compact modeling. The snapback ESD models have been implemented in various ways: proprietary C code, behavioral language Verilog-A, macro-models comprised of standard component models, and Verilog-A modules attached to standard devices. Though no snapback is involved, diodes have special physical effects that are important to ESD events but are not included in standard SPICE models. Modeling the voltage overshoot and current saturation in diodes has been another focus in developing the ESD compact model. Compact models predicting thermal ESD failure or dielectric breakdown have also been reported.

The semiconductor industry has increasingly recognized the importance of compact modeling for SPICE ESD simulation [43,44]. The Compact Model Coalition (CMC) associated with the Silicon Integration Initiative (Si2) started an ESD compact modelling program about a decade ago. The CMC ESD subcommittee set the requirements for the standard ESD compact models, which should be able to balance faster enablement and desired accuracy. The model standardization adopts an adjustable topology (for example, parameterized Verilog-A solution). After several years of working together, CMC released the ASM-ESD diode model in December 2022. This diode model is the first industry-standard model to capture device behavior under ESD event conditions. Since the initial release, many updates have been implemented in the model, and CMC posted a second full model release in April 2025.

CMC has started the development of an ESD MOSFET model as the second standard ESD modeling project. Multiple model proposals have been solicited, and the project is currently evaluating the proposals and choosing one model developer from the candidates. The standard ESD FET model will be valid in both normal operation and ESD high current region. It will combine a regular FET model and a Verilog-A model code of the ESD FET wrapper model. The regular FET model should cover the normal operation model behavior, and the wrapper model describes high current bipolar behavior and will not impact the FET's normal operation behavior. The model will be completed in three years. It is expected that there will be multiple standard ESD compact models available by 2030. Those new standard models should not only include fundamental ESD parameters such as turn-on voltage Vt1, holding voltage Vh, and on-resistance Ron but also critical secondary effects like voltage overshoot, pulse rise-time dependence of Vt1, conductivity modulation, self-heating, forward and reverse recovery in diodes, etc. Industry-standard ESD compact models are intended to be comprehensive. ESD verification with SPICE simulation is a dynamic verification method. As mentioned in Section 5.1, dynamic SPICE simulations can be

integrated into topology-based static EDA checks. Accordingly, simplified SPICE models may be developed for such applications.

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