Electrostatic Discharge (ESD) Technology Roadmap

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EOS/ESD Association, Inc.'s Electrostatic Discharge (ESD) Technology Roadmap

1.0 SYNOPSIS
This document is divided into two main sections. The first provides estimates of future ESD thresholds of semiconductor devices and the potential impact on ESD control practices. These levels are strongly technology and design-dependent and need to be periodically revised in the context of advances in the electronics industry. The threshold estimates discussed in this roadmap are intended to reflect the prevailing trends in semiconductor technology as viewed by selected industry leaders. As in previous versions of this document, the emphasis is on the integrated circuit (IC) industry. Other major electronics industry segments are also experiencing an increase in ESD sensitivities (lowering of ESD thresholds). Some examples are magneto-resistive (MR) heads (disk read/write heads), optoelectronics (light-emitting diodes, lasers, and photodiodes), printed circuit board assembly handling sensitive ICs, and thin-filmed-transistor-based flat panel displays. However, ESD trend information is not usually readily available for these types of devices, and the standardized ESD tests are not defined or broadly applied.

The thresholds are presented in this document in the form of “roadmaps” of estimated changes in thresholds over the next five years. These projections are intended to provide a view of future device protection limitations driven by circuit performance requirements and technology scaling effects. It also provides a common view of expected device ESD performance variations as viewed by device (IC) suppliers and original equipment manufacturers (OEMs), like users. Finally, these trends point to the need for continued improvements in ESD control procedures and compliance. Some linkage of these trends to process capability is also discussed, as is progress in other ESD events characterization (system-level, charged-board events, and cable discharge events).

The second part of the document contains information on trends in device testing and characterization from the ESDA and ESDA/JEDEC teams working on these methods and finishes up with a discussion on novel technology trends.

2.0 DEVICE THRESHOLD TRENDS
2.1 Overview
In the late 1970s, ESD became a problem in the electronics industry. Low threshold level ESD events from people were causing device failures and yield losses. As the industry learned about this phenomenon, both device design improvements and process changes were made to make the devices more robust and the processes more capable of handling these devices.

During the 1980s and early 1990s, device engineers, after going through a learning curve, were able to create protection structures that could withstand higher levels of ESD stress and thus made devices less sensitive to ESD events. Both device engineers and circuit designers were able to identify key technology parameters and design techniques that helped them develop more robust devices.

However, in the mid to late 1990s, the requirements for increased performance (devices that operate at 1 GHz and higher) and the increase in the density of circuits (Moore’s Law) on a device caused problems for traditional ESD protection circuits. This was exacerbated by the continued scaling of the technologies toward sub-100 nm feature sizes to achieve higher density and performance. The situation became worse with the advent of IC chips with sub-50 nm technologies, which were rapidly going into production. With the demand for high-speed internet operations, large, high pin count (> 1000 pins), packaged devices containing high-speed SerDes (HSS) input/output (IOs) that need to operate at 10-15 gigabit per second (Gbps), were introduced. These IOs reached 20-30 Gbps at the 22 nm and 18 nm technology nodes, and with today’s advanced technology nodes at 10 nm and 7 nm, HSS IO in the 56 Gbps to 112 Gbps are more prevalent. Consequently, both the human body model (HBM) and charged device model (CDM) target levels had to be adjusted to accommodate these new IO performance levels.

The wireless connectivity of our world has driven both an increase in radio frequency (RF) applications as well as higher bandwidth requirements. In the mobile space, 4G LTE utilizes
frequency bands up to 5.8 GHz. With the introduction of millimeter-wave 5G technology, the frequency bands the FCC is allocating go into the 28 GHz to 60 GHz regime. For these RF applications, ESD protection must be balanced with performance since these higher frequencies cannot tolerate additional capacitive loads on signal nodes. Any ESD robustness built into the RF pins is often co-designed with the matching network for the application. This almost invariably leads to reduced HBM and CDM withstand voltages. The expectation is that these trends will continue as increased circuit performance will take precedence over ESD protection levels. For future device qualification, HBM and CDM requirements will need to comprehend these technology trends.

2.2 Device ESD Threshold Roadmaps
The following graphs show the device ESD design sensitivity trends based on the most relevant and important ESD models used by device manufacturers as part of the device qualification process: HBM and CDM. The sensitivity limits are a projection by engineers from leading semiconductor manufacturers.

2.2.1 Human Body Model (HBM) Roadmap
The projections for HBM design (typical min and max) are indicated in Figure 1. Although design improvements were made from 1978 through 1993, advanced circuit performance effects started to take place around the mid-’90s, eventually degrading the achievable HBM levels. The maximum levels represent what is typically possible from technology scaling, and minimum levels represent the constriction coming from meeting the circuit performance demands.

![HBM Roadmap (Typical Min – Max)](image)

Figure 1: Overall Human Body Model Sensitivity Limits Projections

Figure 2 presents a zoomed-in look at 2010 through 2025. Additionally, Figure 2 shows the estimated ESD control capability for HBM during the same time based on the levels of HBM controls, which may be in place. Significantly, HBM control methods that exist in today’s production areas have allowed for the reduction of the HBM target level from 2 kilovolts to 1 kilovolt [1]. Even with this de facto target in place, some high-performance devices may only have 100 volts to 200 volts threshold. In the 2020 roadmap, it was suggested that a 500-volt limit might be necessary.
Looking ahead to 2025, it is not clear that another drop in the HBM target level will be necessary for anything other than very high-performance IO, such as 224 Gbps SerDes and RF applications. Implementation of improved HBM controls using the limits and requirements in ANSI/ESD S20.20 [2], IEC 61340-5-1 [3], or JEDEC JESD625 [4] will continue to be important to mitigate the risks of lower HBM protection levels. As shown in Figure 2, below 100 volts is a “custom controls” region in which non-standard process-specific controls are necessary. These controls are very specific to the environment and may include, but not be limited to, tighter ESD control limits and tighter frequency on compliance verification. Performing process capability assessments, as discussed in Section 2.5, has become even more important to address higher performance IO risks in manufacturing.

**HBM Forward Looking Roadmap (Typical Min – Max)**

![HBM Forward Looking Roadmap](image)

**Figure 2: 2010 to 2025 Human Body Model Sensitivity Limits Projections**

In a closer observation of Figure 2, there appears to be little change in the typical range for HBM sensitivity limits looking ahead to 2025, as compared to 2020 or even 2015. While the range may not change dramatically by 2025, the distribution of products within this range will continue to vary. This is a result of some companies remaining on traditional technologies and those who continue to push for technological advancements through the need for higher performance IO in devices.

These technological advancements will be due to both technology scaling and application requirements, such as RF and HSS IO applications. Figure 3 shows the predictions for how this sensitivity distribution mix can look in 2025. As technology scaling and application-specific IO needs are constantly changing, this roadmap update also took a fresh look at the current situation. As a result, the 2020 sensitivity distribution mix has also been modified from the 2016 projections. In looking more closely at the 2020 sensitivity distribution mix, it is believed that the projections for 2020 were a little aggressive. Therefore the 2020 distributions have been adjusted down in the less than 500-volt range. When looking ahead to 2025, it is predicted that there will be small increases in the number of products in the less than 500 volts range and a small decrease in the number of products in the greater than 1000 volts range. Note that a greater than 1000-volt limit was chosen as the top bucket as any device meeting this target level or above for HBM is equally safe, even with the most basic control methods [1]. Furthermore, the only group of real concern would be the
bottom group at less than 500 volts HBM, where the distribution of devices is expected to have a slight increase in the next five years, mostly due to higher performance IO needs.

Figure 3: Forward Looking Human Body Model Sensitivity Distribution Groups

2.2.2 Charged Device Model (CDM) Roadmap

The technology impact on CDM not only comes from the required IO speeds but also from package size effects. Larger packages will experience higher discharge currents at a given stress voltage level. Larger packaging is also possible as a result of more companies exploring 2.5D and 3D technologies. Although the chart does not cover all IC package types, Figure 4 illustrates the combined IO design and package effect. This effect becomes somewhat independent of the technology node starting around 22 nm as the reduction in oxide breakdown voltages is saturating, but becomes more dependent on the IO performance demands which are dictated by the loading capacitance. The color scheme adopted in Figure 4 is based on the validation that 250 volts CDM is safe for production areas [5]. This map will change as package sizes become even larger. For example, note that for today's packages of 3000 pins (~3000-3500 mm²) or more (not uncommon for a microprocessor) in a land grid array (LGA) or ball grid array (BGA), very high-speed IOs might barely meet a CDM target level of 125 volts. An additional package effect, decreasing thickness, was not included here for simplicity but should be noted that this can also impact the peak currents seen by a device independent of the change in package area. In certain market segments, such as in the mobile market space, where the Z-height of the package is critical to market acceptance (for example, phones, watches, and laptops), this package thinning has more impact.

In the RF space, there is often a delicate balance between CDM robustness and RF performance. Exacerbating this CDM sensitivity is the fact that capacitors, which are frequently damaged by CDM transients, are widely used in RF designs for DC blocking, matching networks, filtering, and other application related to the application functionality. Any circuit that would be used to protect these capacitors will ultimately degrade linearity, insertion loss, or otherwise impact the integrity of the RF signal. As higher bandwidth RF applications become more widespread in the market, the achievable CDM performance is likely to decrease.
Thus, the projections for CDM sensitivity levels (typical min and max) are indicated in Figure 5. As shown in the figure, the current CDM target is 250 volts, reduced from the previous 500 volts from the early 2000s. A target of 125 volts will be needed in the future, primarily driven by the need for very high-performance IOs.
As with HBM projections, a magnified look at CDM for 2010 and beyond is presented in Figure 6. Also shown is the ESD control capability for CDM during the same period. Implementation of advanced CDM control methods and a more thorough process assessment are not only more critical but have become nearly mandatory for some products.

A closer observation of Figure 6 might suggest that when looking ahead to 2025, there will be no significant change in the typical range for CDM sensitivity limits as compared to 2020 or even 2015. While the belief is that the range may not change dramatically by 2025, the distribution of products within this range can vary with a change in the mix of companies remaining on today’s traditional technologies. This includes those who continue to push for technological advancements through the need for higher performance devices and growth in package size/complexity through multichip packages such as 2.5D and 3D.

Figure 7 is a first look into how this distribution of products could conceivably look by 2025. As technology scaling/application-specific IO/package scaling needs are constantly changing, this roadmap update also took a fresh look at the current situation. As such, the 2020 mix has also been modified from the 2016 projections. In looking more closely at the 2020 mix, it is believed that the projections for 2020 were a little aggressive. Therefore, the 2020 distributions were adjusted down in the less than 125 volts range. It is predicted that there will be a small increase in the number of products in the less than 125 volts range and small decreases in the number of products in the greater than 250 to 500 volts and greater than 500 volts ranges when looking ahead to 2025. In contrast to the HBM groups of Figure 3, the bottom two groups for CDM distributions are of deeper concern. Thus, the industry needs to continue efforts (such as improved process assessment capabilities) to be better prepared for this larger population of sensitive CDM devices by 2025.
2.3 Device ESD Thresholds and System Level ESD (IEC 61000-4-2): No Correlation

There has been a general perception for several years that device-level ESD (for example, HBM) is a predictor or prerequisite for good system-level ESD robustness. This misconception has caused many OEMs to put special HBM requirements on devices, thinking it will improve the chances of passing the IEC 61000-4-2 system-level test. This misconception was addressed in Industry Council White Paper 3 Part I [6]. As shown in Figure 8, from that study, it has been demonstrated that the IEC 61000-4-2 system-level ESD and device-level ESD are not correlated with each other.

Figure 8: Comparison of IC Device Level and System Level ESD Failure Threshold of Various Systems (A-J) Showing that HBM Protection is not Related to System Level ESD Robustness
At the system level, ESD robustness is a much more complex issue requiring a deeper understanding to address the ESD protection requirements for electronic systems such as laptops, cell phones, printers, home computers, and those in the automotive and industrial segments. These system complexities come about as a result of protecting the external interfaces, such as the universal serial bus (USB), to the outside world. After encountering the more severe ESD pulses such as those specified by the IEC 61000-4-2 [7] or ISO 10605 [8] test methods, such systems can lead to hard or soft failures.

As introduced in White Paper 3 Part I, a co-design approach is required. A basic version of this (called system-efficient ESD design (SEED)) has been proposed, which addresses hard failures related to IC pins with a direct external interface. For soft (reversible) failures, which are more frequently reported, more advanced co-design approaches are needed. These are more challenging to understand and overcome and require an extension of the SEED approach to other failure mechanisms that include latch-up and electromagnetic interference (EMI) effects. These challenges and approaches are discussed in Part II of White Paper 3 [9]. The adoption of SEED within the Industry has begun, but adoption has been limited as Industry best determines how to supply the needed data and simulate the events. It is expected that the trend of adopting SEED, though slower than expected through 2020, will continue to grow as the risk to external IO ports has not changed.

The important point for the present discussion is that none of these system-level failures are improved or reduced by increased HBM or CDM device threshold levels. Thus, the technology scaling effects for both HBM and CDM, as shown in Figures 2 and 6, would not have implications for system-level ESD.

2.4 Process Control

ESD control programs have been in place for many years. One of the earliest programs was implemented to help with the production of gunpowder. This simple program effectively kept the powder wet during manufacturing and handling. This kept the static charge low enough that the gunpowder would not ignite.

In the 1950s and 1960s, electronics were relatively insensitive to ESD events. The devices of the time could withstand most events without a problem. Even if the devices did fail for ESD events, the failures were a very small portion of the overall failure rates.

In the late 1970s, with the introduction of large-scale integration (LSI), ESD became a significant problem. A group of industry experts realized this and organized the first US ESD Symposium in 1978. At the time, technical papers were exchanged, and there were workshops on problems and solutions. Companies at this time also started to implement ESD control programs. Each company had its unique program and did not share the information. The need for standardized programs was not recognized at that time.

The US Military was one of the first organizations to recognize the problems with static electricity and ESD. The first standard to address ESD process control was MIL-STD-1686, released in May of 1980. This standard, along with its companion handbook MIL-HDBK-263, represented the first ESD control standard in the industry. All suppliers of electronics to the military were required to comply with this standard. However, most of the private sector still followed the company developed procedures.

These early standards were focused on people and packaging. The controls in place for insulators were left mostly to the end-user without much consideration except for the removal of non-required insulators. Tools, machines, and automated equipment were not addressed or considered as most of the processes were manual. The basic instructions were to keep everything and everyone handling the devices at the same potential.

An additional issue with these first ESD control programs was that the materials that were used to control static electricity did not have standards to qualify the materials. This led to many different types of testing, different methods, and different instrumentation that caused different results. In some cases, materials measured by these methods did not perform well in controlling static. In the early 1980s, a professional association, EOS/ESD Association, Inc. (ESDA), was formed to resolve
some of the issues surrounding material testing. The first standards from the ESDA were simple material tests for items such as wrist straps, work surfaces, and flooring. The standards created a way to compare one product to another. Suppliers of these materials were able to use the standards to improve products. For example, the simple wrist strap has gone through many changes in the industry. What started as a simple metal bead band has evolved into a system that makes better contact with a person and, in some cases, allows for continuous monitoring. Wrist straps provide a much more reliable connection than before and last longer. The standards also provide a way to test the wrist straps consistently so that a wrist strap that becomes defective can be removed and replaced. Before this, materials were used until physically damaged without regard to the electrical properties.

In the 1980s and 1990s, the electronics manufacturing industry changed from each company having all manufacturing reside within the company to a model that included many contract manufactures (CM) or electronic manufacturing suppliers (EMS). At the same time, the military standard and the European standard, CECC 00 015:1991, were not evolving with technology and with changes in manufacturing supply chains. The standards were either too restrictive or did not address all aspects of a control program.

In 1995, the ESDA was given the task of replacing Mil-Std-1686 with an industry standard. The standard, ANSI/ESD S20.20-1999, was the replacement for ESD process control. Following the release of this standard, a third-party certification program was established to demonstrate compliance to the standard and has been very successfully applied to factory certifications all around the world, as shown in Figure 9. ANSI/ESD S20.20 has been periodically updated to keep pace with device technology, emerging information about ESD failures, and improvements in ESD control technologies and measurement methods with the latest version being ANSI/ESD S20.20-2014 [2]. An update to ANSI/ESD S20.20 is in progress with an anticipated release in 2021. In parallel, the IEC has created and periodically updates a similar control document, IEC 61340-5-1 [3], which is nearly equivalent technically to ANSI/ESD S20.20.

2.5 Process Capability Assessment

These ESD sensitivity trends will have a major impact on manufacturing process yields over the coming years. Companies will need to increase efforts to verify that processes can handle these devices and, where necessary, make improvements in ESD control programs. This could include changes in the ESD control item limits, change in the frequency of compliance verification, and other forms of ESD monitoring, such as ESD event detection.
Recently, the ESD Association released a standard practice on ESD process assessment. ANSI/ESD SP17.1 [10] describes a set of methodologies, techniques, and tools that can be used to characterize a process where ESD sensitive (ESDS) items are handled. The process assessment in ANSI ESD SP17.1 covers risks by charged personnel, ungrounded conductors, charged ESDS items, and ESDS items in an electrostatic field. The basic approach is to compare parameters measured in the manufacturing process, for example, an electrostatic voltage on an ESDS item, with the limits derived from the HBM or CDM robustness of the ESDS item. The procedures in this document are for use by personnel possessing advanced knowledge and experience with electrostatic measurements. The assessment of the results from the measurements described in this document requires significant experience and knowledge of the physics of ESD and the manufacturing process.

2.5.1 Human Body Model (HBM)

It has been shown that the resistance of a person to ground has a direct correlation to the maximum voltage on a person. Tests on a person wearing a wrist strap using standard shoes on a non-ESD flooring have shown that a total resistance to ground through the wrist strap of $40 \times 10^6$ ohms or less is necessary to limit body voltage to less than 100 volts. Figure 10 shows the relationship between the body voltage of personnel wearing standard shoes on a non-ESD floor connected by a wrist strap to ground as a function of the total resistance to ground through the wrist strap. The limit for wrist straps provided within ANSI/ESD S20.20 is $35 \times 10^6$ ohms, which is approximately a 10% safety margin.

![Figure 10: Relationship Between Body Voltage and Resistance to Ground](image)

For an ESD control program that uses a footwear/flooring system to ground personnel, the situation is more complex. As people walk across a floor while wearing footwear design to keep personnel grounded, it is difficult to predict the voltage on a persons’ body due to the constantly changing body capacitance and the continuous charging and discharging of the person.

ANSI/ESD STM97.2 [11] can be used to determine the process capability of the footwear flooring system. An example of the type of information provided can be seen in Figure 11.
2.5.2 Machine Discharge Events

Machine discharges occur when charged conductive surfaces come into contact with ESD sensitive devices. To minimize machine discharges, ensure that all conductive surfaces that come into contact or proximity with ESD sensitive devices are grounded. If it is not possible to ground conductive surfaces, then measurements should be made to ensure that moving parts remain below a threshold voltage throughout the process. In ANSI/ESD S20.20-2014, the threshold is defined at 35 volts. Caution: this threshold level does not translate into any measured characterization with an MM tester. These measurements must be taken with the proper equipment, such as a contact voltmeter or non-contact voltmeter. Most field meters cannot make this measurement.

2.5.3 Events from Charged Devices and Static (Field) Induction (CDM)

In its pure form, a CDM event occurs when a charged ESD sensitive device is grounded or when a neutral device is grounded in the presence of an electrostatic field. A unique characteristic of these events is the involvement of a very fast rise time event between a device pin and another conductor at a different potential. CDM is the most relevant discharge model when single ICs are handled with automated equipment or manually by using hand tools. Thus, the CDM test method also indicates the more general cases of conductor-conductor discharges, such as touching a device lead with conductive tweezers. This includes many of the isolated conductor discharge events mentioned in the previous section.

Effective ESD control programs ensure that process required insulators will not induce a voltage onto the devices (static induction) being handled or that devices be triboelectrically charged, which could result in a damaging discharge of the device. As CDM thresholds are lowered, it becomes more difficult to depend on voltage control alone to provide adequate protection of devices. Thus, it is becoming more important to eliminate conductor-conductor contact wherever possible and use dissipative materials to avoid hard grounding.

2.5.4 Charged Board Events (CBE)

ICs and other ESD sensitive devices remain at risk when mounted onto printed circuit boards and other assemblies. There is evidence that many ESD failures in circuit and system assemblies occur at the board level. These types of failures are due to charged board events (CBE). Most ESD testing and characterization of devices are done on stand-alone parts. This is the type of data that is summarized in the HBM and CDM roadmaps.
Further, IC failure analysis data, which is based on knowledge of failure signatures seen in standard HBM and CDM tests, has caused many to conclude that ESD failures are relatively rare when compared to other electrical failures commonly classified as electrical overstress (EOS). Recent data and experience reported by several companies and laboratories now suggest that many failures previously classified as EOS may instead be the result of ESD failures due to CBE (or cable discharge events [CDE] discussed in the next section). A charged board stores more energy than a stand-alone part because its capacitance is larger. The charge (energy) transferred in the event may be large enough to cause EOS-like failures to the devices on the board.

The previous paragraph implies that some PCBs can have sensitivities outside the scope of ANSI/ESD S20.20. This, in turn, might require tightening some of the ESD control practices defined there. However, in most cases, these practices and requirements should be sufficient for protecting circuit boards. Problems do arise when specific program implementations do not fully recognize PCBs as ESD sensitive items. In these cases, the risk of failure due to CBE may be significant. Identifying CBE as the root cause of failure can be difficult. This may require conducting tests that can replicate failures due to CBE and distinguish them from other possible electrical stresses. Methods for conducting CBE tests are currently under development in ESDA WG 25.0 (see Section 3.2.3).

### 2.5.5 Cable Discharge Events (CDE)

The insulation on a communication cable (USB, Ethernet, etc.) is easily triboelectrically charged by the movement of the cable over surfaces such as desktops, floors, clothing, and work surfaces. This charging will, in turn, induce a potential on the conductors of the cable. When the charged cable is plugged into a system, an ESD event occurs between a cable conductor(s) and one or more of the connector pins of the system receptacle, depending on the connector design. This discharge is referred to as CDE. The resulting current pulse is highly dependent on the length, impedance, type of connector, and quality of the cable. Industry reports indicate that CDE can cause an interface device to be damaged, create system "lock-up" or system upset. CDE is generally thought of as a charge equalization process between the victim unit or device and a charged cable. Still, a CDE can also occur if the victim unit (laptop, cellphone, etc.) becomes charged by the cable. In the latter case, the victim unit becomes triboelectrically charged via contact with some material or via a charged person. Whether the cable is charged or the victim unit charged, the result is a discharge involving current flowing into or out of a cable. Similar to CBE, the root cause of damage to a device from a CDE may be misdiagnosed as coming from some other form of electrical stress. Methods for conducting tests that can replicate a CDE are under development (see Section 3.2.4).

### 3.0 TRENDS IN ELECTRICAL STRESS TESTING

Failure of devices due to a wide variety of electrical stresses is a major contributor to yield losses in manufacturing. ESD represents one category of such stresses that can cause large yield loss events, and continuous background drop out. The HBM and CDM test methods have been the main enabler to the design of ESD-robust devices and are described in further detail in Section 3.1. These methods are often described as qualification methods because of the key role in the relationship between supplier and user. Stress tests can play other important roles such as characterization or failure replication; these are discussed in Section 3.2.

#### 3.1 Device-Level ESD Qualification

As described previously, the decrease in ESD thresholds will put more pressure on the ESD control program to maintain high yields. To know where special procedures and scrutiny are required, one needs to know the device sensitivities. With pin counts increasing and pin spacings decreasing, the evaluation of devices for ESD thresholds has become more challenging. As a result, the HBM and CDM test methods have continued to change, and additional changes are anticipated to track increasing device complexity. The increasing test costs and time continue to drive changes in these methods as well.
This data is also used in specific ways. ESD control programs such as ANSI/ESD S20.20 include in the scope, minimum withstand threshold values below which it is suggested that additional controls maybe be needed to maintain high yield. Some organizations such as the US Military and private companies use the HBM and CDM classification levels in JS-001 and JS-002 to add further granularity to an ESD control program. HBM and CDM classification levels are used for process assessment, as described in ANSI/ESD SP17.1. Most significantly, device users and suppliers in the electronics industry use the thresholds obtained from HBM and CDM testing as part of the larger set of technical requirements for defining a qualification device. For example, JEDEC JESD47 [12] (Stress-Test-Driven Qualification of Integrated Circuits), includes both HBM and CDM testing. As a result, these methods are often referred to as qualification test methods. It is also important to note that unlike most other tests required for qualification, ESD testing and threshold assignment cannot be done on technology, family, or package basis. Given the important role played by these tests in nearly every new design, considerable effort has been made to provide reproducible and reliable methods that are as efficient as possible. Details and trends for these methods are described below.

### 3.1.1 Human Body Model (HBM)

In 2010, the ESDA and JEDEC HBM test methods were merged into a single document designated ANSI/ESDA/JEDEC JS-001-2010. After this, the joint ESDA/JEDEC working group issued 2011, 2012, 2014, and 2017 [13] versions. Over the years many changes have been made to the HBM standard including some key items below:

- A new pin combination table was introduced to reduce device failures due to wear-out from excessive stresses (by hundreds or thousands) that were required by the previous version. This introduced the Table 2A/2B pin combination options. A detailed discussion of these changes is available in the standard or the companion HBM User Guide, ESD JTR001-01-12 [14].
- Eliminating the IO to IO test pin combination for most pins, except for a small set of specialized coupled non-supply pins. The focused testing of IO pairs that could be weakly protected can provide an improvement over testing IO pins to all other IO pins tied together.
  - These efforts also helped to enable two-pin HBM testers. These systems eliminate the device-tester parasitics inherent in a relay-based test system.
- Defining and taking advantage of low impedance interconnection structures. This change allowed the representation of a supply or ground group of pins to be represented by a single pin according to the conditions described. The concept of a low-impedance above-passivation layer (APL), sometimes also known as a redistribution layer (RDL), was introduced.
- Verification of and Testing with Low-Parasitic Simulators. These changes add a test to determine when a tester has sufficiently low parasitics to allow the elimination of certain “pin reversal” two-pin combinations
- Introduction of a sampling method for “cloned” non-supply pins. This new procedure is applied to a special set of identical IO pins called cloned IO pins.
- Addition of a 50-volt test level in recognition of very low target level products.
- Introducing an Annex focused on failure windows and the need for understanding of this in HBM testing.

Further work being discussed in the HBM JWG includes evaluation of a true statistical sampling scheme intended to reduce the over-stressing of pins relative to real-world environments without compromising the threshold assessment of the product. Additionally, work is underway to require testing of any exposed pad on the package. The implications of this may require the need for new hardware on the HBM tester to support the testing. A significant update the HBM User Guide is also planned to reinforce guidance on some of the changes listed previously.
3.1.2 Charged Device Model (CDM)

CDM continues to be recognized in the electronics industry as a valuable ESD model for assessing ESD risk in automated IC handling and manufacturing around the world. CDM ESD must consider the scaling of device process – IO pin technology, scaling down of minimum device size – pin pitch achievable in test, and CDM tester metrology limitations in consideration of the CDM roadmap direction over the next five years.

3.1.2.1 Device Thresholds

The continuing trends of integrated circuit process technology advances, increasing package size and complexity, and increasing IO performance requirements all point to lower minimum charged device model withstand thresholds, especially for the high-performance pins. These trends will result in a larger percentage of high-performance pins on products forecasted to be below 125 volts by 2025. These pins may only comprise a small fraction of the total number of pins in any one package.

3.1.2.2 Package Size / Pin Pitch

Two package-related limiting factors to CDM testing are the minimum package size and pin or ball pitch (distance between pins/balls on a package type). Minimum package x-y dimensions in 2020 are on the order of 400 by 600 µm, and this is expected to pose still a challenge to small package testing looking out to 2025. A pin pitch of 350 µm (the minimum achievable by CDM testers in 2020) will not allow testing for packages with smaller pin pitch (including bare die pad spacings) for today’s pogo-style discharge pin/ground plane style CDM probe assemblies. Thus making future CDM test capability require the use of probe technology (similar to probe automated test equipment [ATE] today) for those die form products.

3.1.2.3 CDM Testing Methodology

Two types of CDM testing are in use today. The first type, field-induced CDM testing, is in use by over 90% of the electronics industry today. This is widely based on the harmonized ANSI/ESDA/JEDEC JS-002 CDM standard, published in 2015, and updated in 2018 [15]. This industry harmonization has helped the industry standardize on a single field-induced CDM test platform but still is left with limitations. These limitations include the minimum device size and pin pitch physical limitation of the CDM test equipment (which leads to multiple pin discharges for very small pitches), as well as the environmental variation of the discharge spark, which is dependent on device size, charge voltage, and relative humidity.

The continued reduction in minimum CDM pin thresholds described limits the use of field-induced CDM for many devices due to the increased variation in the discharge waveform at low voltage levels.

An alternative CDM testing method, low impedance contact CDM (LICCDM), has been shown in early trials to achieve a more accurate discharge pulse, independent of humidity, and the varying characteristics of the discharge spark in the field-induced CDM event. Research in approximating the impedance of the field-induced discharge spark with a discharge impedance in the contact CDM metrology chain (through the transmission line and relay switching) has shown significant promise to provide repeatable, reproducible discharge waveforms down below 50 volts with no humidity dependence. A standard practice (ANSI/ESDA/JEDEC SP5.3.3) was published in 2019, describing this new test method. Testing using this method is expected to yield more accurate CDM testing at lower voltage levels for those devices needing it. This contact approach also eliminates some of the challenges of testing smaller packages/pin pitches by allowing a sharper pogo tip to be used.

Additionally, a second alternative CDM test method (capacitively coupled TLP (CC-TLP, which also uses a contact approach), is being investigated with a standard practice document in development. CC-TLP systems have been used for a much longer time compared to LICCDM, but CC-TLP has the limitation of not being able to completely match the field-induced CDM discharge waveform rise time and pulse width specifications. However, CC-TLP is being considered as a possible wafer-
level characterization technique that would give important information on protection structures in advance of any packaging and could be used as a solid figure of merit at the wafer level to compare the ESD robustness of various protection structures.

It is expected that contact CDM test technology using these two methods will become standardized as a complementary, more attractive alternative to field-induced CDM testing over the next five years as contact CDM research leads to further standardization of contact CDM worldwide. Additionally, as with HBM, a reduced pin count sampling method for CDM may need investigation and development in the next five years to see if time and resource savings can be realized for high pin count products with no impact to the CDM threshold assessment.

3.2 Characterization and Replication Methods

Stress tests can play other important roles, such as characterization or failure replication. Characterization using Transmission-Line Pulse (TLP) gives ESD protection designers an early indication of the electrical response to ESD-like pulses, which in turn informs the ultimate protection strategy. Other roles that can be played by electrical stress tests are to aid failure analysis and root cause verification and to provide comparative evaluations of corrective actions. These can be described as stress replication tests. The tests include transient latch-up (TLU), variations of CBE and CDE stresses, and other unintended electrical stresses. These non-qualification methods are discussed in more detail below. It is possible that in the future, some stressing methods can become so widespread and reliable enough to evolve into acceptance or compliance tests. Currently, none of the methods are in that category.

3.2.1 Transmission Line Pulse (TLP) Characterization

The Transmission Line Pulse (TLP) method has become the de-facto standard method for ESD characterization of stand-alone devices/components and pins of ICs. ANSI/ESD STM5.5.1 [16], released in 2016, is the basis for this work and covers transmission line-based quasi-static characterization with pulse widths in the range of single nanoseconds to several microseconds. The User and Application Guide, ESD TR5.5-04-18 [17], provides additional information on the practical use of TLP systems. A technical report, ESD TR5.5-05-20 [18], addresses the use of TLP systems for non-quasi-static analysis and was released in 2020.

As interest in the analysis of the device response to fast transients, such as during CDM or system-level stressing, is increasing, work will likely continue after the publication of [18]. The possibility of proposing a standard practice will be explored. The increased usage of TLP and the use of the results for developing ESD models for the SEED method [6, 9] suggests the development of a definition of a (minimum) standard way of characterization and reporting for such applications. This may lead to a new technical report or extension of the user and application guide. Finally, the working group will investigate available options to extend the pulse width range and rise time range of the TLP methods.

3.2.2 Transient Latch-Up (TLU) Replication

Integrated circuits can contain latch-up sensitive structures (such as parasitic thyristors), which can cause reliability issues during operation. For this reason, most semiconductor devices must be qualified to a respective latch-up sensitivity. JEDEC JESD78 [19] is the most commonly used latch-up qualification standard. However, this test has a rather slow rise time and long trigger pulse, which does not cover many latch-up events. It is well known that fast transients, such as ESD, can trigger latch-up more efficiently.

Per the “static” JEDEC JESD78 latch-up standard, the working group defines transient latch-up as a state in which a low-impedance path, resulting from a transient overstress that triggers a parasitic thyristor structure or bipolar structure or combinations of both, persists at least temporarily after removal or cessation of the triggering condition. The rise time of the transient overstress causing TLU is faster than 5 µs.
In 2014, to address industry needs, ESDA WG5.4 started a new standard practice on TLU, which defines a universal TLU methodology that can be used for replicating transient effects seen in the field. The proposed TLU trigger pulses and the set-up can be modified rather simply to match the requirements and constraints in a specific application. The methodology can be applied to a broad range of applications, from simple test structures and discrete semiconductor devices to complex integrated circuits as standalone devices or in systems. Essentially, all TLU events discussed in ESD TR5.4-04-13 [20] can be reproduced by the proposed methodology. An important building block of the document is the verification methodology of the TLU set-up, which ensures a correct pulse delivery to the device-under-test as well as a sufficiently fast response of the power supply. ESDA WG 5.4 released ANSI/ESD SP5.4.1 in 2017 [21].

It must be emphasized that the TLU test methodology proposed in the standard practice is not intended to be used as a qualification methodology, in contrast to the static latch-up test JESD78, which is a mandatory device qualification test. The TLU methodology can be applied to pins, which might be endangered by fast transients in the field to replicate certain types of electrical overstress.

It is intended to establish close cooperation with the JEDEC JESD78 working group, as both standardization committees face very similar technical challenges. In the future, the relevance of TLU compared to purely “static” latch-up, according to JEDEC JESD78, will certainly increase. Therefore, a close link between the JEDEC JESD78 WG and ESDA WG 5.4 is planned.

3.2.3 Charged-Board Event (CBE) Replication
The ESDA has published a technical report, ESD TR25.0-01-16, giving general information about CBE phenomena [22]. ESDA is preparing a second technical report document that gives guidance to the industry for replicating CBE threats. It will contain examples of how to set up a CBE test bench, how to carry out testing, and how to report test results. The document also contains information on how to estimate CBE stress levels based on calculated and simulated data. ESD threats due to CBE are case-specific, and the upcoming TR will not contain acceptance or target levels for CBE stress. Instead, it instructs how the user can specify the target level and estimate ESD risks based on the observed discharge waveforms in the process area and on the test bench. A final version of the second CBE technical report is expected for release in 2021.

3.2.4 Cable Discharge Events (CDE) Replication
ESDA WG 14 (System Level ESD) has been collecting data on real-world CDE events, gathering relevant information from case studies and papers, to create a well-defined test method. In the context of this section on the testing of devices, this test could be a useful replication tool in the same vein as CBE. However, this method also has potential and perhaps more interest as a system-level test that could reproduce operational system failures as well as hardware failure of individual devices. WG14 plans to guide the industry to allow reproducible testing against CDE threats and to help in determining the CDE immunity of a system, such as a laptop or handheld device (phones/cameras, etc.). Cable discharge events can occur when either a charged cable by itself discharges into a system or when a cable that is attached to another item (which adds additional capacitance) discharges into a system. The amount of variation in the discharge events has made it difficult to establish a single representative waveform for a test method. The WG will be focusing on the development of a technical report that will provide information to industry on the different possible CDE events, different levels of events based on cable types while also offering insight to system designers on possible design and protection recommendations. The WG has written multiple articles on CDE with an emphasis on educating the industry about CDE but also as a way of gathering information from sources outside of the committee. The technical report on CDE is expected to be released in 2021 and then followed up by a standard practice outlining different testing recommendations.
3.2.5 Replication of Other Electrical Stresses

The development of defined methods for replication of other electrical stresses is gaining some interest. This arises from the industry-wide initiative to reduce device failures often characterized as electrical overstress (EOS) [23]. The main challenge is to find a way to reproduce a wide range of possible stresses systematically. WG 23 is collecting data and industry practices for producing these stresses based on waveform characteristics and other environmental factors to publish a technical report in 2021-2022.

4.0 NOVEL TECHNOLOGY TRENDS

4.1 2.5D and 3D ICs

Novel die stacking processes are characterized using through-silicon vias (TSV) and the stacking of dies connected by micro bumps (see Figure 12). The motivation for the use of these package techniques is a reduced footprint on the PCB and reduced wiring length, which leads to reduced capacitance and results in enhanced performances and lower power. 2.5D solutions, as well as specific 3D IC solutions, have already entered the market. 2.5D solutions are gaining an increased market share by offering a flexible disaggregation of the functionality of different dies and thermal advantages while maintaining a fully integrated solution. ITRS refers to it as a heterogeneous integration which will drive IC scaling in the coming years [24]. Also, wide IO applications for memory die integration will grow significantly in the number of products. The number of micro bumps between processor and memory die can amount to several thousand interfaces. Typically, only a very small percentage of the interfaces are connected to the external package ball.

This leads to a situation with a clear differentiation of internal micro bumps and external package balls. The external package balls need to be protected, and ESD qualified to the common IC ESD targets, as discussed previously. The aspects of micro bumps are presented below.

![2.5D IC Stack and 3D IC Stack](image)

**Figure 12**: 2.5D Stack (left) and 3D Stack (right) ICs

*NOTE*: TSV establishes the electrical connection from the bottom to the front side of a die. The contact between dies is formed by micro bumps (black circles). The connection from bottom die to package is via regular bumps (small grey circles). During board assembly, only package balls (large grey circles) are accessible and exposed to ESD events.

4.2 ESD Control Requirements for 2.5D and 3D ICs

2.5D IC technology, and to a greater extent 3D IC technology, introduces several new manufacturing steps as well as testing procedures, which can lead to charging and discharging of the die, such as in the die-to-die stacking process. One example of a testing procedure change is the need to verify good dies by testing both the front side and backside (TSV) contacts. A study of specific ESD control measures for 2.5D and 3D ICs is presented in [25]. A careful analysis of the process steps will highlight the risks that can be covered by known ESD control measures.
4.3 ESD Protection of Micro Bumps and On-Package IO (OPIO)

As shown in Figure 12, micro bumps exist in both 2.5D and 3D products, while many multi-chip package (MCP) products contain on-package IO (OPIO). OPIO are inter-die connections running through the package substrate used as communication between the MCP die. These interconnects offer a short, low capacitance and high speed interconnect path designed to improve overall product performance. There is limited data available for the required ESD protection level on products containing micro bumps or OPIO. It is clear from an economic standpoint that as a result of the enormous number of micro bump interfaces and the push for higher performance on these short interconnect paths, utilizing the same ESD protection as normal IOs exposed in the final package for micro bump IOs or OPIOs is not acceptable. Since micro bump or OPIO interconnect are only exposed to ESD discharges during a few die handling steps, it is also acceptable that the ESD target levels of micro bumps and OPIO can be significantly lower. Nevertheless, minimum input protection should be applied to the receiving gates, but this can be provided by the intrinsic diodes of junctions connected to the gate node, as shown by Nagata [26].

4.4 Challenges with ESD Testing of Micro Bumps

The size of the bump must be reduced to a minimum to enable the placement of a large number of micro bumps on a die. These micro bumps are in the range of 20 μm in diameter and smaller. Due to this very small diameter, ESD stress testing, especially in CDM testing, of bumped dies will not be feasible. Assembly of the die in a reference package, where all micro bumps are routed to package bumps, leads to an unacceptable change in the actual CDM robustness. This is due to the need for a fan-out die for the micro bumps and the package parasitics, not to mention the huge effort and cost of building such a test chip IC. Since most wide IO interfaces are typically built up of a common ESD protection structure, it is suggested to test representative IOs (like inputs, outputs, etc.) by forcing VF-TLP pulses with the use of microprobes. Alternatively, CC-TLP or wafer-level TLP may be a future option to consider.

4.5 Target Levels

While the package bumps of 2.5D or 3D IOs need to satisfy regular ESD targets, the micro bumps will follow a different specification. Since the likely characterization techniques discussed previously are current testing methods, target values must be specified in terms of current. Target peak currents for nanosecond pulses between 200 milliamperes and 1 ampere are discussed as being efficient and practical [23]. Recent recommendations of the Industry Council on ESD Target Levels provide a target peak current in the range of 100 to 800 milliamperes [27].

5.0 REFERENCES


[27] Industry Council on ESD Target Levels; White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements, Revision 3.0 – targeted for release Q4’20