EOS/ESD Symposium Best Student Paper Awards

2000 “Chip-Level Simulation for CDM failures in Multi-Power ICs"
Jaesik Lee, University of Illinois

2001 “Human Body Model Test of a Low Voltage Threshold SCR Device: Simulation and Comparison with the Transmission Line Pulse Test"
P. Galy, Pole Universitaire Leonard de Vinci

2002 "ESD Characterization of Grounded-Gate NMOS with 0.35 μm/18 V Technology Employing Tranmission Line Pulser (TLP) Test"
B-C Jeon, S-C Lee, J-K Oh, S-S Kim, M-K Han, Seoul National University; Y-I Jung, H-T So, J-S Shim, K-H Kim, Hynix Semiconductor Inc.

2003 "Comprehensive ESD Protection for RF inputs"
S. Hyvonen, S. Joshi, E. Rosenbaum, University of Illinois at Urbana-Champaign

2004 "Study of CDM Specific Effects for a Smart Power Input Protection Structure"
M. Etherton, N. Qu, J. Willemen, W. Wilkening, S. Mettler, M. Dissegna, R. Stella, L. Zullino, A. Andreini, h. Gieser, H. Wolf, W. Fichtner Swiss Federal Institute of Technology

2005 “SCR Operation Mode of Diode Strings for ESD Protection”
U. Glaser, M. Ciappa, W. Fichtner, ETH Zurich; K. Esmark, C. Russ, M. Streibl, Infineon Technologies; K. Domanski, Infineon Technologies and Nicolaus Copernicus University

2006 “Transmission Line Pulse (TLP) Testing of Radio Frequency (RF) Micro-machined Micro-Electro-Mechanical-Systems (MEMS) Switches”
A. Tazzoli, V. Peretti, E. Zanoni, G. Meneghesso, University of Padova

2007 **“**Reliability Aspects of Gate Oxide under ESD Pulse Stress”
Adrien Ille, Université de Provence and Infineon Technologies, Wolfgang Stadler, Thomas Pompl, Harald Gossner, Tilo Brodbeck, Kai Esmark , Philipp Riess, David Alvarez,Infineon Technologies; Kiran Chatty, Robert Gauthier, IBM; Alain Bravaix, Université de Provence

2008 **“**Design Methodology of FinFETDevices that Meet IC-Level HBM Target”
S. Thijs, G. Groeseneken, IMEC vzw and Katholieke Universiteit Leuven; C. Russ, H. Gossner, Infineon Technologies AG; D. Trémouilles, LAAS/CNRS; A. Griffoni, University of Padova; D. Linten, M. Scholz, N. Collaert, R. Rooyackers, M. Jurczak, IMEC vzw; M. Sawada, T. Nakaei, T. Hasebe, Hanwa Electronics Ind. Co. Ltd; C. Duvvury, Texas Instruments Inc.

2009 **“**ESD Time-Domain Characterization of High-k Gate Dielectric in a 32 nm CMOS Technology”
James Di Sarro, Elyse Rosenbaum, University of Illinois at Urbana-Champaign; Yang Yang, Dimitris Ioannou, George Mason University; Kiran Chatty, Robert Gauthier, Souvick Mitra, Junjun Li, IBM; Christian Russ, Infineon Technologies

2010 **“**Investigation of Current Flow During Wafer-Level CDM Using Real-Time Probing”
Nathan Jack and Vrashank Shukla, Advisor – Prof. Elyse Rosenbaum, University of Illinois at Urbana-Champaign

2011 “ESD Simulation with Wunsch-Bell based Behavior Modeling Methodology”
Yiqun Cao, Infineon Technologies and Technische Universität Dortmund

Advisor: Stephan Frei,Technische Universität Dortmund, Co-authors: Ulrich Glaser, Joost Willemen, Filippo Magrini, Michael Mayerhofer, Matthias Stecher, Infineon Technologies

2012 “ESD Characterization of Atomically-Thin Graphene”
Hong Li, Kaustav Banerjee, Wei Liu, University of California; Christian C. Russ, David Johnsson, Harald Gossner, Intel Mobile Communications

2013 “Predictive Modeling of Peak Discharge Current during Charged Device Model Test of Micro-Electronic Components”
Vrashank Shukla, University of Illinois at Urbana-Champaign Advisor: Elyse Rosenbaum, University of Illinois at Urbana-Champaign Co-Authors: Gianluca Boselli, Mariano Dissegna, Charvaka Duvvury, Raj Sankaralingam, Texas Instruments, Inc.

2014 “Do Devices on PCBs Really See a Higher CDM-like ESD Risk?”
Robert Mertens, University of Illinois at Urbana-Champaign Advisor: Elyse Rosenbaum University of Illinois at Urbana-Champaign Co-authors: Nicholas Thomson, Yang Xiu University of Illinois at Urbana-Champaign

2015 “CDM-Reliable T-coil Techniques for High-Speed Wireline Receivers”
Min-Sun Keel, University of Illinois at Urbana-Champaign; Advisor: Elyse Rosenbaum University of Illinois at Urbana-Champaign

2016 “An Automated Tool for Chip-Scale ESD Network Exploration and Verification”
Benjamin Viale, STMicroelectronics, CNRS-UMR Advisor: Bruno Allard CNRS-UMR

2017 “On-Chip Sensors to Measure Level of Transient Events”
A. Patnaik, M. Suchak, R. Seva, K. Pamidimukkala, D. Beetner, Missouri University of Science and Technology; G. Edgington, R. Moseley, J. Feddeler, M. Stockinger, NXP Semiconductors

2018 “Hardware and Software Combined Detection of System-Level ESD-Induced Soft Failures”
Sandeep Vora, Rui Jiang, Prajwal Mysore-Vijayaraj, Keven Feng, Yang Xiu, Shobha Vasudevan, Elyse Rosenbaum, University of Illinois Urbana-Champagne