44th ANNUAL ELECTRICAL OVERSTRESS/ELECTROSTATIC DISCHARGE SYMPOSIUM CALL FOR PAPERS

Including the EOS/ESD Manufacturing Track

Sept 18-23, 2022 **Peppermill Resort & Casino** **Reno, NV, USA**

The EOS/ESD Symposium is dedicated to the understanding of issues related to electrostatic discharge and electrical transients/overstress, and the application of this knowledge to the solution of problems in consumer, industrial, and automotive applications, including electronic components, as well as in systems, subsystems, and equipment.

Travel Uncertain – Don't Worry – Submit Anyway!

EOS/ESD Association, Inc is leading conferences with a pioneering approach to our virtual reality. Our hybrid conference includes both virtual and in person presentations and attendance to suit your needs. Authors who anticipate inability to travel to a conference because of a travel restriction are encouraged to submit papers.

Special Focus Modules

Automotive

The electronics content in the modern automotive industry has increased rapidly and this trend is further reinforced by the evolution in the electric vehicles. The most recent developments in the field of autonomous driving and infotainment services require the implementation of more and more complex systems based both on state-of-the-art digital technologies and ultra-high voltage nodes. The impact on ESD design is meaningful as severe qualification requirements, compliance testing and security requirements are defining new challenges. Therefore, suitable trade-off between ESD and competing specifications (such as EMC and EOS) must be found.

Communications

Over the past two decades, our world has been quickly moving to completely wireless communications. 5G will provide mobile traffic growth of 1000X, 100 billion connected devices, etc. High-speed interfaces are approaching 224 Gb/s. Furthermore, the types of communication have swiftly changed from voice to data. Indeed, with the proliferation of smart homes, smart cars, and even smart cities, the communication applications continue to expand. As the applications become increasingly critical, the reliability of the “Internet of Things” (IoT) devices become crucial. The complexity of the circuits required for ESD and EOS protection and mitigation continue to expand as well. Many of these electronic components are both “system on a chip” (SoC) as well as multi-component modules that contain a range of technologies from advanced to mature silicon-based technologies to GaAs and GaN chips.

Heterogeneous Integration

The integration of separately manufactured components such as dies, passive components, bridges, or systems or sub-systems into one package, allows adding more functionality into a product without device scaling. Different approaches for 2D or 3D integration are already in use. Heterogeneous integration often comes with an enormous high density of face-to-face interconnects between two chips. The dense bump pitch of these interconnects and the demand to very low power consumption restrain any ESD protection of the interconnects significantly. These interconnects do not have a package connection and, therefore, ESD robustness could be reduced compared to package pins. However, the processing of these interconnects still requires a good balance between a distinct minimum ESD robustness and very advanced ESD control measures of the corresponding manufacturing process steps.

Low Power

With the advent of handheld wireless devices, the focus on reducing power consumption of electronic products has increased. Mobile phone OEM’s have traditionally been scrutinizing leakage requirements to increase the length between battery recharging cycles. For many IoT products, small batteries are expected to power the device for years without recharging. Providing adequate ESD protection for these circuits becomes quite challenging. First, ESD protection circuits can be rather “leaky” and can consume a significant amount of the electrical leakage budget of an application. Exacerbating this is the need for system level protection in the handheld IoT device. Given these competing requirements, the design of ESD protection for low powerless applications remains an active area of research.

Advanced Technologies & Testing

The relentless drive to scale technology features and increase signaling rates continues to shrink the ESD design window as never before. New technologies require novel approaches for success. In addition to innovative protection schemes it becomes imperative that ESD be properly and accurately characterized. A key focus this year will be the ESD implications of advanced technologies and circuits – both from a design and test perspective.

Submission Options

Technical Paper	Technical Poster
Abstract: Maximum 4 pages	**Abstract:** Maximum 2 pages
Final Manuscript: 6-10 pages	**Final Manuscript:** 3-5 pages
Presentation: Maximum 20 slides	**Presentation:** Maximum 10 slides

Abstract (Paper/Poster) submission due February 7, 2022: Your original 50-word abstract and summary of work to be expanded in a full technical paper or a technical poster must clearly and concisely present specific results and explain the importance of your work in the context of prior work. Authors are required to use the applicable abstract submission template available at https://www.esda.org/events/44th-annual-eosesd-symposium-and-exhibits. Final classification of abstracts as full technical papers or technical posters is at the discretion of the technical program committee. Full manuscripts of accepted technical papers and technical posters will be due before the conference. Registration for the conference is required for the author presenting the paper.

The technical program committee accepts unpublished papers/posters for peer review with the understanding that the author will not publish the work elsewhere prior to presentation at the Symposium. Presentation of your work at the earlier International ESD Workshop (IEW) will not preclude your EOS/ESD Symposium abstract submission. The submission must follow guidelines and be expanded significantly for the EOS/ESD Symposium. Publication of accepted papers/posters in any form prior to presentation at the Symposium may result in the paper being withdrawn from the Symposium Proceedings. Authors must obtain appropriate company and government clearances prior to submitting an abstract.

Additional Submission Options

Workshop or Discussion Group

Proposals for workshops and discussion groups must be submitted no later than February 7, 2022, with an abstract describing the proposal. Send proposals to esdaadministrative@esda.org. **Workshop** topics address fundamentals, generally accepted techniques, and consider present and future challenges and solutions to problems. **Discussion Group** topics address EOS/ESD novel ideas and consider new developments or common myths dispelled. The discussion should encompass some provocative points of view.

Seminar

Proposals for seminars must be submitted no later than February 7, 2022, with an abstract defining the presentation. Send proposals to esdaadministrative@esda.org. Topics can be related to the special focus modules defined previously or can be a review of industry progress on one of the suggested areas below.

Demonstration

Proposals for live demonstrations of measurement or design techniques (hardware and software) must be submitted no later than February 7, 2022, with an abstract defining the presentation and measurement or design technique. Send proposals to esdaadministrative@esda.org. Authors complete a presentation describing the measurement or design technique followed by a live demonstration. Application, limitations, and common pitfalls should be discussed. (Note: ESDA does not provide equipment).

TEsD Talk

Proposals for a fifteen-minute talk (minimal use of slides – no words) on a controversial or futuristic topic to spark debate and discussion must be submitted no later than February 7, 2022, with an abstract defining the topic. Send proposals to esdaadministrative@esda.org.

Suggested Submission Topics

Advanced CMOS (Analog/Digital) EOS/ESD and Latch-up

- ESD Issues in Advanced Technologies (Multi-gate, FinFET, SOI, SiGe, Compound, Graphene, nanowire, etc.)
- On-Chip ESD Protection Devices & Techniques in Advanced CMOS Technologies
- IC Design and Layout Issues
- Circuit Simulation of EOS/ESD Events in Advanced CMOS Technologies
- DC/Transient Latch-up Issues and Solutions, Troubleshooting, Simulation
- ESD Issues in 2.5D & 3D Stacking and TSV

ESD Protection in Bipolar, RF, High Voltage and BCD Technologies

- ESD Issues in Bipolar, RF, High Voltage, and BCD Technologies and power Technologies (SiC, GaN, etc.)
- On-Chip ESD Protection Devices & Techniques in Bipolar, RF, High Voltage and BCD Technologies
- IC Design and Layout Issues
- Circuit Simulation of EOS/ESD Events in Bipolar, RF, High Voltage, and BCD Technologies
- DC/Transient Latch-up Issues and Solutions, Troubleshooting, Simulation
- ESD Circuit Simulation and Co-Design

Numerical Modeling and Simulation for On-Chip ESD Protection

- ESD Device TCAD Simulation
- Simulation Tool and Methodology
- Numerical Modeling and Physics of EOS/ESD Events
- TCAD/Circuit Co-simulation

EOS/ESD Failure Analysis, Troubleshooting and Case Studies

- EOS/ESD Case Studies, Reviews and Analysis
- EOS/ESD Phenomena in MEMS (Microelectromechanical Systems)
- Failure Analysis Techniques and Interpretations
- EOS/ESD Component Failure Analysis
- Testing of MR/TMR Heads and Ultra-Sensitive Devices
- EOS/ESD Protection for Aircraft, Spacecraft, and Avionics

Device Testing: Testers, Methods and Correlation Issues

- Transmission Line Pulse Testing Systems
- Novel EOS/ESD Test Methods
- Novel TLP Measurement Results
- HBM, CDM Tester Issues and Solutions
- Tester Correlation Issues
- Standards – Round-Robin Testing, Results and Analysis

System Level EOS/ESD/EMC, HMM

- System Level EOS/ESD/EMC Test Methods
- System Level EOS/ESD Modeling and Simulation
- EOS/ESD Simulators, Calibration and Correlation
- Transient ESD/EMI Induced Upset
- Case Studies, Reviews and Analysis
- Standard Test Boards as an Early Measure of Robustness

Chip/Module/Package EOS/ESD Electronic Design Automation

- Novel EOS/ESD EDA Tools
- ESD Checking and Verification Methodology
- Application of EDA tools for EOS/ESD Failure Analysis, Design and Verification

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