43rd ANNUAL ELECTRICAL OVERSTRESS/ELECTROSTATIC DISCHARGE SYMPOSIUM CALL FOR PAPERS

Co-Located with EOS/ESD Manufacturing Conference and Workshop on Robustness of IoT Devices

Sept 26-Oct 1, 2021 **Westin La Paloma Resort & Spa** **Tucson, AZ, USA**

The EOS/ESD Symposium is dedicated to the understanding of issues related to electrostatic discharge and electrical transients/overstress, and the application of this knowledge to the solution of problems in consumer, industrial, and automotive applications, including electronic components, as well as in systems, subsystems, and equipment.

Special Focus Topics

Automotive

Increasing high voltage semiconductor content, integration of sensors, and advanced CMOS is enabling advanced driver assist, safety, efficiency, entertainment, and autonomous driving. Stringent qualification requirements, compliance testing and security requirements of electronics in automotive applications is bringing new challenges and design tradeoff to ESD and latch-up with other competing EMC and EOS specifications. This is a special focus topic for the 2021 EOS/ESD Symposium, soliciting inputs on all topics ESD/EOS related to automotive ecosystem. This includes technologies, tools, design, specifications, test, and the drive to zero DPPM.

Novel Technologies

In the forthcoming 3nm CMOS node the FINFET topology will get exhausted and a shift to gate all around technologies is appearing in semiconductor manufacturing. In addition, novel 2.5D and 3D packaging technologies are ramping to achieve the needed power and performance gain. ESD is challenged by the impact of a gate all around technology on ESD devices, the design optimization of a growing number of die to die interfaces, the ESD verification of complex system in package solutions and the process assessment of these packaging techniques. This is a special focus topic for the 2021 EOS/ESD Symposium, soliciting original publications in this field.

Communications

In a world where so much activity has been forced to go virtual, communications, particularly wireless communications, have taken on an oversized importance. This includes not only mobile phones, but base stations, and all the infrastructure that these require. The ESD protection requirements are also daunting. From ESD protection for RF and analog devices to protecting antennas on hand-held devices, the challenges for designing robust products can be overwhelming. This is exacerbated by the ever-increasing requirements for signal integrity and performance. A focus for this year's EOS/ESD Symposium is finding the balance between delivering high performance wireless communication products in designs that are robust against the ESD threats that the current environment entails.

Submission Options

Technical Paper	**Technical Poster**
Abstract: Maximum 4 pages	**Abstract:** Maximum 2 pages
Final Manuscript: 6-10 pages	**Final Manuscript:** 3-5 pages
Presentation: Maximum 20 slides	**Presentation:** Maximum 10 slides

Abstract (Paper/Poster) submission due February 8, 2021: Your original 50-word abstract and summary of work to be expanded in a full technical paper or a technical poster must clearly and concisely present specific results, and explain the importance of your work in the context of prior work. Authors are required to use the applicable abstract submission template available at https://www.esda.org/events/43rd-annual-eosesd-symposium-and-exhibits. Final classification of abstracts as full technical papers or technical posters is at the discretion of the technical program committee. Full manuscripts of accepted technical papers and technical posters will be due before the conference. Registration for the conference is required for the author presenting the paper.

The technical program committee accepts unpublished papers/posters for peer review with the understanding that the author will not publish the work elsewhere prior to presentation at the Symposium. Presentation of your work at the earlier International ESD Workshop (IEW) will not preclude your EOS/ESD Symposium abstract submission. The submission must follow guidelines and be expanded significantly for the EOS/ESD Symposium. Publication of accepted papers/posters in any form prior to presentation at the Symposium may result in the paper being withdrawn from the Symposium Proceedings. Authors must obtain appropriate company and government clearances prior to submitting an abstract.

Suggested Submission Areas

Advanced CMOS (Analog/Digital) EOS/ESD and Latch-up

- ESD Issues in Advanced Technologies (Multi-gate, FinFET, SOI, SiGe, Compound, Graphene, nanowire, etc.)
- On-Chip ESD Protection Devices & Techniques in Advanced CMOS Technologies
- IC Design and Layout Issues
- Circuit Simulation of EOS/ESD Events in Advanced CMOS Technologies
- DC/Transient Latch-up Issues and Solutions, Troubleshooting, Simulation
- ESD Issues in 2.5D & 3D Stacking and TSV

ESD Protection in Bipolar, RF, High Voltage and BCD Technologies

- ESD Issues in Bipolar, RF, High Voltage, and BCD Technologies and power Technologies (SiC, GaN, etc.)
- On-Chip ESD Protection Devices & Techniques in Bipolar, RF, High Voltage and BCD Technologies
- IC Design and Layout Issues
- Circuit Simulation of EOS/ESD Events in Bipolar, RF, High Voltage, and BCD Technologies
- DC/Transient Latch-up Issues and Solutions, Troubleshooting, Simulation
- ESD Circuit Simulation and Co-Design

Numerical Modeling and Simulation for On-Chip ESD Protection

- ESD Device TCAD Simulation
- Simulation Tool and Methodology
- Numerical Modeling and Physics of EOS/ESD Events
- TCAD/Circuit Co-simulation

EOS/ESD Failure Analysis, Troubleshooting and Case Studies

- EOS/ESD Case Studies, Reviews and Analysis
- EOS/ESD Phenomena in MEMS (Microelectromechanical Systems)
- Failure Analysis Techniques and Interpretations
- EOS/ESD Component Failure Analysis
- Testing of MR/TMR Heads and Ultra-Sensitive Devices
- EOS/ESD Protection for Aircraft, Spacecraft, and Avionics

Device Testing: Testers, Methods and Correlation Issues

- Transmission Line Pulse Testing Systems
- Novel EOS/ESD Test Methods
- Novel TLP Measurement Results
- HBM, CDM Tester Issues and Solutions
- Tester Correlation Issues
- Standards – Round-Robin Testing, Results and Analysis

System Level EOS/ESD/EMC, HMM

- System Level EOS/ESD/EMC Test Methods
- System Level EOS/ESD Modeling and Simulation
- EOS/ESD Simulators, Calibration and Correlation
- Transient ESD/EMI Induced Upset
- Case Studies, Reviews and Analysis
- Standard Test Boards as an Early Measure of Robustness

Chip/Module/Package EOS/ESD Electronic Design Automation

- Novel EOS/ESD EDA Tools
- ESD Checking and Verification Methodology
- Application of EDA tools for EOS/ESD Failure Analysis, Design and Verification

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