2023 US ESD Workshop (US-IEW)
March 26-30, 2023
Hyatt Regency, Monterey, CA, USA

16th Annual US Electrostatic Discharge Workshop (US-IEW)

Now in its 16th year, the IEW continues to provide a relaxed, invigorating atmosphere to present new work and engage in discussions about the latest issues confronting the ESD and EOS communities. After a two-year hiatus, US-IEW will again co-locate with the International Reliability Physics Symposium (IRPS) in 2023! In addition to everything US-IEW provides, US-IEW registrants will also be able to attend the full IRPS technical program (any technical session, invited talks, and keynote speakers), including the joint evening poster reception showcasing works from both conferences. IRPS registrants will have access to US-IEW keynote and invited talks (but not the other unique elements of US-IEW). Therefore, submissions to US-IEW will receive exposure to a much broader audience. US-IEW will retain the distinctive elements which make it a unique experience: invited speakers & seminars, discussion groups, and some downtime to network and explore the area.

Submission Instructions

Thanks to the co-location with IRPS, submissions will occur through the IRPS website (https://irps.org/irps-call-for-papers/download-call-for-papers/). Poster submission is due by **January 23, 2023**, the deadline for IRPS' Late News Papers. The poster (in presentation format) should clearly present specific results and explain the importance of the work in the context of prior work. Use the IRPS presentation template available at www.irps.org. Registration for the conference is required for the author presenting the poster.

US-IEW does not publish proceedings, even for US-IEW-registered posters presented during joint IRPS/US-IEW poster sessions. Walk-on posters are also permitted at US-IEW with no prior review, but only those works which are submitted for review and acceptance will be included in the five-minute teaser presentation sessions.

FOCUS TOPICS FOR US-IEW 2023

New Developments in Latch-Up

Emerging product trends such as technology scaling (e.g., FinFET versus planar CMOS), increasing product complexity, and more demanding operation environments (e.g., automotive; high junction temperature; radiation-induced latch-up; etc.) all lead to the stark reality that latch-up will be a major reliability threat for the foreseeable future. There are active teams in the industry working to consolidate learning and best practices for latch-up EDA tools and to test and qualify the increasingly complex products being produced. The US-IEW welcomes you to share your experience and perspective on this important topic.

System ESD

Cable Discharge Event (CDE) - test methods, applicability, design impact, potential standardization. System ESD design - co-design between the system board and the component (SEED). System ESD simulation methods and component modeling, new stress models. On-chip design methods for improving system ESD. System ESD-related failure modes and case studies. Test methods for validating ESD on the board level - is test standardization of component robustness under system ESD feasible?

Electrical Overstress (EOS)

EOS continues to be one of the semiconductor industry's largest causes of customer returns. Have you recently completed root-cause analysis on a failure with an electrical induced physical damage (EIPD) signature? There is no defined procedure to determine a product's absolute maximum ratings (AMR). Do you have a methodology for defining AMR for a product and verifying it for different timescales? Are you an FA engineer with experience in case studies identifying EOS damage mechanisms and the ensuing physical evidence? Finding sources of EOS can be a challenge. Do you have experience auditing a manufacturing site for sources of EOS? Bring your work to the US-IEW and share it with your colleagues.

Other topics and areas to consider for abstract submissions include but are not limited to:

Anomalous/Unresolved ESD Issues
Random and unrepeatable ESD failures, case histories, ESD tester correlation issues, and unique window failures.

Automotive Applications ESD/EMC
The electronic content of automobiles is increasing, leading to more complex electronic modules and system design. Integration of ICs and discrete devices are demanding, considering the module-level EMC testing and reliability requirements. The US-IEW invites contributions that address ESD and EMC challenges in automotive systems design, including complying with standards such as bulk current injection (BCI), direct power injection (DPI), IEC-61000-4-2, ISO-10605, and ISO-7637.

ESD Big Data
Summarize and view large ESD and latch-up tester datasets, view CDM waveform parameter statistics, and map design data to ESD and latch-up test programs.

System-Level ESD Issues
On- and off-chip IEC protection clamps, component/system ESD co-design case studies, cable discharge clamps, transient latch-up, design of system-level clamp circuits, system-level ESD test issues and scan techniques, and ESD-induced soft errors.

Failure Analysis Techniques
Locating failure sites, particularly for CDM, imaging techniques, correlating FA-identified damage sites with ESD stress, distinguishing EOS-like failures from ESD failures, and unusual failure modes.

Technology Integration Issues
ESD sensitivity with technology transfers, 3D IC ESD design issues, qualification challenges for different fabs, unusual problems of process interaction with ESD, process monitor methods, and technology scaling issues.

EDA Tools
EDA verification and simulation tools; techniques, design flows, best practices, experiences with foundry rule decks, commercial tools, and custom tooling.

ESD Control
As technologies continue to change, we need to consider the control methods being used and continually review the standards and methodologies being used to ensure the best practices are being followed. Case in point, to provide the industry with the best standards possible, ANSI/ESD S20.20/JESD 625B working groups are looking at harmonizing these documents. We also need to consider whether there are any weak points in today's processes that may require updates to the control standards or new standards to cover new technologies. The use of discharge detectors as a tool for analyzing problem areas within assembly has proven to be very useful. Should analysis tools like discharge detectors become standard in the Control process?

Novel On-Chip Protection Clamps and Circuit Configurations
New clamp devices and clamp configurations, methods to increase the failure threshold of protected devices, high voltage clamps for automotive and power amplifiers, new chip protection concepts, and low-capacitance clamps for RF and high-speed interfaces.

ESD Test Characterization, Methods, and Issues
TLP & VF-TLP debug and device characterization methods, correlation of TLP & VF-TLP tests with standard qualification tests, HBM and CDM tester artifacts, unresolved test results and failures, issues relating test qualification levels to real-world exposure, test chip methodology, cable discharge test methods, and test standards issues.