3rd Workshop on Robustness of IoT Devices

September 16-17, 2020

- IoT catalyzes a change in the way device robustness is implemented and tested.
- Be there when the new directions are set for technical solutions, standards, and shared responsibilities in industry.
- Meet with today's experts and industry leaders on the Robustness of IoT Devices.
    - Invited talks by IoT technology leaders
    - Open workshop style debates
    - Interactive expert panel discussion

Education Symposium

Welcome by the Management Team

Together with the technical program committee, we would like to welcome you to our third Workshop on Robustness of IoT Devices on September 16 & 17 in conjunction with the 2020 EOS/ESD Symposium in Reno, NV, USA. During this worldwide crisis, our way of living and working has been challenged in an unprecedented way, including the cancellation of many established and appreciated scientific meetings. We are looking forward to a workshop that allows us to meet in person to discuss results and open topics of our technical fields. The crisis is, to some extent, a stress test for the 'robustness' of our social and technical systems. It shows us how important it is to study and plan for situations which are far outside our usual 'range of operation'. With the continued and accelerated growth of IoT devices and applications which reach far into our private life and impact the safety of billions, the consideration of robustness of IoT devices is an absolute necessity.

You might ask the question, "what is different in the robustness of an IoT device compared to electronic devices and systems we have produced and used for decades?" The answer is somehow trivial. There is no difference if the device is designed and tested for a specific, well-defined mission profile. However, continually growing and expanding IoT applications need semiconductor devices which have been developed for very different usage. Examples include a 5G baseband IC or an AI accelerator, which can end up in very harsh ambient conditions. A dedicated design would both delay the innovations and not be economically feasible for lower volume parts. The challenge is to establish methods to make a solid judgment of the robustness of this device used for the different mission profiles. This needs the consideration of reliability aspects as well as immunity against electrical transients. As the PCB and module design has a substantial impact on the outcome of the assessment, the treatment of co-design and co-evaluation is crucial to assess the robustness of the IoT devices.

We have created a dedicated workshop to offer a holistic discussion of robustness, including lifetime aspects as well as transient stress situations. The workshop is a unique forum to bring the IC design community, the system design community, and application development together for this topic. The mission of the Workshop on Robustness of IoT Devices has been established as a stand-alone event following a period of incubation under the umbrella of the EOS/ESD Symposium. This year's workshop is focused on the development of new methodologies supporting the fast and versatile assessment of mission profiles and the aspects of heterogeneous integration, which adds different technologies and materials (other than silicon) to the robustness considerations.

We wish you an inspiring workshop with the best possible exchange, and we are looking forward to seeing you in September.

Best regards
Ann Concannon, Texas Instruments
Mirko Scholz, Infineon Technologies AG
Harald Gossner, Intel Duetschland GmbH

Virtual Schedule

WEDNESDAY, SEPTEMBER 16, 2020

Welcome	1:00 p.m. - 1:05 p.m.	IoT Workshop Welcome
	1:05 p.m. - 2:00 p.m.	Keynote: **Advanced Packaging Architectures and Associated Robustness Challenges**
	2:00 p.m. - 5:20 p.m.	IoT Technical Sessions
	2:00 p.m. - 2:50 p.m.	**2.1 (Invited) - High Reliability Assessment**
	2:50 p.m. - 3:20 p.m.	**1.1 - Low Power Technologies for IoT**
	3:40 p.m. - 4:10 p.m.	**1.2 - MEMs Robustness in IOT Applications**
	4:10 p.m. - 4:40 p.m.	**1.3 - Active Polymer Interposers as Base for Robust Heterogenous IoT Systems**
	4:40 p.m. - 5:20 p.m.	**1.5 - Robust Wireless Connectivity for IoT Applications**

THURSDAY, SEPTEMBER 17, 2020

8:00 a.m. - 9:00 a.m.	Panel Session
9:10 a.m. - 1:00 p.m.	IoT Technical Sessions
9:10 a.m. - 10:00 a.m.	**1.4 (Invited) - Transient Pulse Characterization for IC**
10:00 a.m. - 10:50 a.m.	**2.2 (Invited) - Design Methods for Robust Aging Assessment and Validation of Automotive and Hi Reliability IP**
11:10 a.m. - 12:00 p.m.	**2.3 (Invited) - EDA Tools Supporting Heterogeneous Integration in 2.5D and 3D**
12:00 p.m. - 12:30 p.m.	**2.4 - A Novel Look at Transient AMR Representation**
12:30 p.m. - 1:00 p.m.	**2.5 - Walking Wounded Loophole in System Level ESD Qualification**

Presenters will appear via a live stream link or pre recorded video.

Register Online!

http://www.cvent.com/d/6nqqp6

KEYNOTE

Wednesday, September 16

1:05 p.m. - 2:00 p.m.

Advanced Packaging Architectures and Associated Robustness Challenges

Ravi Mahajan, Intel Fellow

Advanced packaging technologies are critical enablers of Heterogeneous Integration (HI) because of their importance as compact, power efficient platforms.. This talk will trace the evolving role of packaging over the past decades and examine its value as an HI platform. Different packaging architectures will be compared primarily on the basis of their physical interconnect capabilities. Key features in leading edge 2D and 3D technologies, such as EMIB, Silicon Interposer, Foveros and Co-EMIB will be described and a roadmap for their evolution will be presented. Challenges and opportunities in developing robust advanced package architectures will be discussed. The talk will conclude with a discussion of overall opportunities and challenges in driving the package roadmap forward.

Ravi Mahajan is an Intel Fellow and the Director of Pathfinding for Assembly and Packaging technologies for future silicon nodes. Ravi also represents Intel in academia through research advisory boards, conference leadership and participation in various student initiatives.

Ravi has led Pathfinding efforts to define Package Architectures, Technologies and Assembly Processes for multiple Intel silicon nodes since 2000, spanning 90nm, 65nm, 45nm, 32nm, 22nm and 7nm silicon. Earlier in his Intel career, he spent eight years as a Technologist and manager for the Thermal-Mechanical Tools and Analysis Group. In these roles, Ravi oversaw a Thermal-Mechanical Lab chartered with delivering detailed thermal and mechanical characterization of Intel's packaging solutions for current and future processors. His group was also responsible for the collaborative development of a number of technologies for the thermal management of micro-electronics, high precision thermal and thermo-mechanical characterization and modeling techniques.

A prolific inventor and recognized expert in microelectronics packaging technologies, Ravi holds more than 50 patents, including the original patents for silicon bridges that became the foundation for Intel's EMIB technology. His early insights also led to high-performance, cost-effective cooling solutions for high-end microprocessors and the proliferation of photo-mechanics techniques used for thermo-mechanical stress model validation.

Ravi joined Intel in 1992 after earning a bachelor's degree from Bombay University, a master's degree from the University of Houston, and a Ph.D. from Lehigh University, all in Mechanical Engineering. His contributions during his Intel career have earned him numerous industry honors, including the SRC's 2015 Mahboob Khan Outstanding Industry Liaison Award, the 2016 THERMI Award from SEMITHERM, the 2016 Allan Kraus Thermal Management Medal & the 2018 InterPACK Achievement award from ASME, the 2019 "Outstanding Service and Leadership to the IEEE" Awards from IEEE Phoenix Section & Region 6 and the 2020 Richard Chu ITherm Award for Excellence.

He is an IEEE EPS Distinguished Lecturer. He is one of the founding editors for the Intel Assembly and Test Technology Journal (IATTJ) and currently VP of Publications & Managing Editor-in-Chief of the IEEE Transactions of the CPMT. Additionally he has been long associated with ASME's InterPACK conference and was Conference Co-Chair of the 2017 Conference. Ravi is a Fellow of two leading societies, ASME and IEEE. He was named an Intel Fellow in 2017.

IoT Technical Sessions
2:00 p.m. - 5:20 p.m.

I 2.1 (Invited) Reliability and IoT Devices: IoT Mission Profiles, Design Challenges, and Methods
Scott Martin, Subhadeep Ghosh, Texas Instrument

As IoT proliferates throughout the public domain into automobiles, factories, and buildings, reliability of these IoT devices must also scale. A fundamental aspect of reliability is that the device must support the mission profile. The talk provides the key aspects how IoT device mission profiles is integrated into a design strategy.

I 1.1 Low Power Technologies for IoT
Michael Wu, Jam Wem Lee, TSMC

The IoT devices require the low cost and low power to be perfectly matched to mature technology on low power options as a quite sustainable nodes in a long run. Specific challenges for silicon foundry technology are to provide extreme low leakage power clamps to save the battery life and to deliver solutions for HMM (IEC61000-4-2) requirements.

I 1.2 MEMs Robustness in IOT Applications
Barry O'Connell, TDK-InvenSense

MEMs sensors are becoming ubiquitous in IOT devices. This paper focusses on the sensor sensitivity and robustness requirements involved in different applications and the design tradeoffs associated with these competing forces. It addresses some of the common application requirements, for example drop and tumble requirements, and methods not currently covered by industry standard testing.

I 1.3 Active Polymer Interposers as Base for Robust Heterogenous IoT Systems
Karen Shrier, Electronic Polymers; Harald Gossner, Intel

Downscaled IoT systems can efficiently be integrated as 2.5D or 3D package systems with various functionality dies in smallest volume. Active polymer interposers offer an attractive alternative to costly Silicon based interposers offering integrated ESD protection at lowest parasitic capacitance.

I 1.5 Robust Wireless Connectivity for IoT Applications
Stefan Dannenberger, Texas Instruments

The backbone of the Internet of Things (IoT) is connectivity. Sensor and actuator nodes are connected to the cloud through central hubs. This talk will discuss low-power wireless connectivity solutions for the IoT, focusing on wireless MCU radio architecture, important radio parameters and communication standards, and the environmental influences to be considered for robust and reliable communication.

Panel Session

8:00 a.m. - 9:00 a.m.

IoT Technical Sessions

9:10 a.m. - 1:00 p.m.

I 1.4 (Invited) Transient Pulse Characterization for IC and Modules

Heinrich Wolf, Fraunhofer EMFT

Considering the versatility of IoT device applications the robustness testing of IoT ICs and modules must be revisited. The presentation discusses real world examples and proposes an efficient method for transient stress testing at module and board level. Together with the characterization of the stand-alone ICs this enables the co-design of IC and PCB for robustness goals of the specific IoT mission profile.

I 2.2 (Invited) Design Methods for Robust Aging Assessment and Validation of Automotive and Hi Reliability IP

David Burnell, Cadence Design Systems

Today's ecosystem is mostly geared for consumer-grade designs where aging analysis tools are evolving but most solutions today are just running circuit simulators with aging enabled. Automotive and industrial quality requires a different mindset build on a robust IP design environment supports aging assessments at all levels. In this presentation we will cover the methods, tools and flows to enable intelligent evaluations throughout the circuit hierarchy and design process.

I 2.3 (Invited) User Friendly Full Chip ESD Design Verification Platform

Frank Feng, Synopsys

A library based ESD design rule writing python utility is presented which can greatly help users to develop their different requirements on IO, power/ground ESD protection circuits, and automatically clustering power clamping devices physically for a flexible and easy-to-use (IoT) device design. A VUE GUI assists the user to understand results of ESD layout parasitic check breakdown by layer.

I 2.4 A Novel Look at Transient AMR Representation

Harald Gossner, Intel

A concise and meaningful description of transient absolute maximum ratings (tAMR) is one of today's pain points for specifying ICs. A novel AMR diagram is proposed which contains maximum absolute ratings over all time domains. This includes the lifetime degradation regime as well as worst case power to fail characteristics.

I 2.5 Walking Wounded Loophole in System Level ESD Qualification

James Karp, Xilinx

"Walking wounded" are parts that have been damaged but are not detected as failures. Component-level ESD qualification results detect failures of functional FPGAs. Contrarily System-level ESD Qualification with JTAG detect no failures of the same FPGA. A proposal is made to match component and system-level pass/fail criteria.

Virtual Registration

Register Online!
http://www.cvent.com/d/6nqqp6

IoT Live Stream $150

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*On-Demand is available two weeks after the event. Access is for 30 days.