49th ANNUAL ELECTRICAL OVERSTRESS/ELECTROSTATIC DISCHARGE SYMPOSIUM CALL FOR PAPERS

September 20 – 23, 2027 **Riverside Convention Center** **Riverside, CA, USA**

The EOS/ESD Symposium is dedicated to the understanding and resolution of issues related to electrostatic discharge and electrical overstress in consumer, industrial, and automotive applications.

Manuscript Length: 6-8 pages
Presentation Length: Maximum 20 slides (20 minutes plus 5 minutes Q&A)

NEW for 2027: No longer a 4-page abstract submission; instead, a camera-ready 6-8 page manuscript submission is due March 12, 2027. The new submission format is introduced in 2027 to address authors' request to allow a later submission date. Your 6-8 page camera-ready manuscript needs to clearly state the purpose, methodology, results (which must include data, drawings, graphs, or photographs), and conclusions of your work. Emphasize how your work advances the state of the art. Authors must adhere to the EOS/ESD Association, Inc. submission template (Click Here). The author presenting the paper must register for the conference.

The technical program committee accepts unpublished technical papers for peer review with the understanding that the author will not publish the work elsewhere before the Symposium. Publication of accepted papers in any form before presentation at the Symposium may result in the paper being withdrawn from the Symposium Proceedings. Authors must obtain appropriate company and government clearances before submitting a manuscript.

Suggested Submission Topics

Advanced CMOS (Analog/Digital) EOS/ESD
- ESD Challenges in Advanced Technologies (Multi-gate, FinFET, SOI, SiGe, Compound, Graphene, nanowire, etc.)
- Backside Power design challenges and opportunities
- ESD Challenges in 2.5D & 3D Stacking and TSV

Advanced Bipolar, RF, BCD, and WBG Technologies
- ESD Challenges in Advanced Bipolar, RF, BCD, and WBG Technologies (SiC, GaN, etc.)

Device Testing: Testers, Methods, and Correlation Issues
- Novel EOS/ESD Test and Characterization Methods
- Transmission Line Pulse Testing Systems
- HBM and CDM Tester Issues and Solutions
- Tester Correlation Issues
- Standards – Round-Robin Testing, Results, and Analysis

Chip/Module/Package ESD EDA
- Novel ESD Verification Methodology
- Numerical Modeling and Physics of ESD Events
- ESD Device TCAD and Compact Models
- ESD IP Simulation and Co-Design Methodology
- Application of EDA tools for ESD Failure Analysis

EOS/ESD Failure Analysis and Troubleshooting
- EOS/ESD Case Studies and Analysis
- Failure Analysis Techniques and Interpretations
- Testing of MR/TMR Heads and Ultra-Sensitive Devices
- EOS/ESD Protection for Aircraft, Spacecraft, and Avionics

Latch-up in CMOS, Bipolar, RF, High Voltage, and BCD Technologies
- DC/Transient Latch-up Issues and Prevention, Troubleshooting, Simulation Methodologies

System Level EOS/ESD/EMC, HMM
- System Level EOS/ESD/EMC Test Methods, Modeling, and Simulations
- EOS/ESD Simulators, Calibration, and Correlation
- Transient ESD/EMI Induced Upset
- Case Studies, Reviews, and Analysis

Manufacturing
- ESD Packaging and Handling Procedures
- EOS/EMI/ESD Detection and Measurement Techniques
- EOS/ESD Mitigation in Test and Manufacturing
- EOS/EMC/ESD Process Assessment
- ESD Control Materials and Use of Low Charging Materials
- EOS/ESD Control Program Topics
- Electrostatics modeling, measurement, and instrumentation

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