2026 International ESD Workshop (IEW) – Asia In-Person Event

Annual International Electrostatic Discharge Workshop

Co-located with IPFA2026

13th - 16th July, 2026 Marina Bay Sands Expo and Convention Centre Singapore

CALL FOR POSTERS

In July, 2026, we will continue to embrace the IEW-Asia event co-located with the International Physical and Failure Analysis of Integrated Circuits (IPFA2026). Never change, IEW will continue to provide a relaxed, invigorating atmosphere to present new work and engage in discussions about the latest issues confronting the ESD and EOS communities in its 19th year. The workshop will retain the peculiar elements: a tutorial, invited seminar speakers, discussion groups, invited talk speakers, technical presentation sessions, and special interest groups. In addition to everything IEW-Asia provides, IEW-Asia registrants will also be able to attend the full IPFA technical program (any technical session, invited talks, and keynote speakers), including the joint evening poster reception showcasing works from both conferences. IPFA registrants will have access to IEW keynote and invited talks (but not the other unique elements of IEW-Asia). **Therefore, submissions to IEW-Asia will receive exposure to a much broader audience.**The IEW is the perfect opportunity to submit late-breaking and exciting new research to stimulate discussion and interaction around new ideas, encouraging new research topics, as shown below:

FOCUS TOPICS FOR IEW-Asia 2026

Artificial Intelligence (AI) Involved ESD/EMC Design

ESD/EMC design is an important aspect of electronic circuit and system design. With the rapid development of AI technology, ESD/EMC design that utilizes AI to optimize performance and efficiency has become an intriguing and critical area of work. The new design methodologies driven by AI are also attractive to the industry. It is promising to discuss and present AI-related work in the field of ESD/EMC design.

2.5D/3D hetero-Integrations

System-Technology Co-Optimizations (STCO) with 2.5D/3D hetero-integrations and chiplet design concepts have been considered as a major future innovation booster in semiconductor and electronics industry. The IEW invites on-going research and development work to better understand the ESD effects during the 2.5D/3D hetero-integrations? Your research and development work can provide guidance on ESD target levels, on ESD testing of die-to-die interfaces and for IP development in 2.5D and 3D ICs.

ESD Control

As technologies continue to change, we need to consider the control methods and continually review the standards and methodologies to ensure the best practices are followed. Case in point, to provide the industry with the best standards, ANSI/ESD S20.20/JESD 625B working groups are looking at harmonizing these documents. We also need to consider whether there are any weak points in today's processes that may require updating to cover new technologies. The use of discharge detectors as a tool for analyzing problem areas within assembly has proven to be very useful. Should analysis tools like discharge detectors become standard in the Control process?

Novel On-Chip Protection Clamps and Circuit Configurations

New clamp devices and clamp configurations, methods to increase the ESD robustness of the on-chip design, such as high voltage clamps for automotive application, power management ICs, new on-chip protection concepts, and low-capacitance clamps for RF and high-speed interfaces. New ESD clamp structure and circuit innovation based on advanced CMOS, BCD, RF and SiC, GaN technologies etc.

Other topics and areas to consider for abstract submissions include but are not limited to:

Automotive Applications ESD/EMC

Integration of ICs and discrete devices are demanding, considering the module-level EMC testing and reliability requirements in automotive. The IEW invites contributions that address ESD and EMC challenges in automotive systems design, including complying with standards such as bulk current injection (BCI), direct power injection (DPI), IEC-61000-4-2, ISO-10605 and ISO-7637.

ESD Big Data

Summarize and view large ESD and latch-up tester datasets, view CDM waveform parameter statistics, and map design data to ESD and latch-up test programs. Data analytics to identify ESD and latch-up trends over time. root cause identification improvement using historical and real-time big data.

Electrical Overstress (EOS)

EOS continues to be one of the semiconductor industry's largest causes of customer returns. Have you recently completed root-cause analysis on a failure with an electrical induced physical damage (EIPD) signature? Do you have a methodology for defining absolute maximum ratings (AMR) for a product and verifying it for different timescales? Bring your work to the IEW and share it with big audiences.

EDA Tools

EDA tools used for ESD design and verification keep fast developing. There could be a lot of interesting topics of EDA tools from system level down to ESD cell, such as EDA techniques, design flows, best practices, experiences with foundry rule decks, commercial tools, and custom tooling.

ESD Test Characterization, Methods, and Issues

TLP & VF-TLP debug and device characterization methods, correlation of TLP & VF-TLP tests with standard qualification tests, HBM and CDM tester artifacts, unresolved test results and failures, issues relating test qualification levels to real-world exposure, test chip methodology, cable discharge test methods, and test standards issues.

Failure Analysis Techniques

Locating failure sites, particularly for CDM, imaging techniques, correlating FA-identified damage sites with ESD stress, distinguishing EOS-like failures from ESD failures, and unusual failure modes. The IEW invites contributions that address recent FA techniques to improve the understanding of corresponding failure mechanisms.

New Developments in Latch-Up

Emerging product trends such as technology scaling increasing product complexity, and more demanding operation environments (e.g., automotive; high junction temperature; radiation-induced latch-up; etc.) all lead to the stark reality that latch-up will be a major reliability threat for the foreseeable future. The IEW welcomes you to share your perspective on this important topic.

System ESD

System ESD design: co-design between the system board and the component (SEED). System ESD simulation methods and component modeling, new stress models. On-chip design methods for improving system ESD. System ESD-related failure modes and case studies. Test methods for validating ESD on the board level: is test standardization of component robustness under system ESD feasible?

IMPORTANT DATES

March 6th, 2026
Abstract Poster Submission Deadline

April 10th, 2026
Notification of Acceptance

June 26th, 2026
Final Poster Due

Submission Guidelines

Submission instructions and an abstract template will be available at 2026 IEW-Asia event at ESDA website (https://www.esda.org/events/2026-international-esd-workshop-iew-asia/). Thanks to the co-location with IPFA, the link of 2026 IEW-Asia will aslo occur through the IPFA website (https://ipfaieee.org/2026/). The submission is in PowerPoint format and is no longer than 6 slides. Submissions are due Mar 6th, 2026. There will be no published proceedings of IEW. Walk-on posters are also permitted at IEW with no prior review, but only those works which are submitted for review and acceptance will be included in the five-minute teaser presentation sessions.