48th ANNUAL ELECTRICAL OVERSTRESS/ELECTROSTATIC DISCHARGE SYMPOSIUM CALL FOR PAPERS

September 26 - October 1, 2026 **Frisco Hotel & Convention Center** **Frisco, TX, USA**

The EOS/ESD Symposium is dedicated to the understanding and resolution of issues related to electrostatic discharge and electrical overstress in consumer, industrial, and automotive applications.

Abstract Length: 2-4 pages
Final Manuscript Length: 6-10 pages
Presentation Length: Maximum 20 slides

Abstract submission due February 6, 2026: Your abstract (2-4 pages) needs to clearly state the purpose, methodology, results (which must include data, drawings, graphs, or photographs), and conclusions of your work. Emphasis needs to be placed on how your work advances the state-of-the-art. Upon acceptance, your abstract will need to be expanded into a full technical paper (6-10 pages). Authors must adhere to the following submission template (Click Here). Registration for the conference is required for the author presenting the paper.

The technical program committee accepts unpublished technical papers for peer review with the understanding that the author will not publish the work elsewhere before the Symposium. Publication of accepted papers in any form before presentation at the Symposium may result in the paper being withdrawn from the Symposium Proceedings. Authors must obtain appropriate company and government clearances before submitting an abstract.

Suggested Submission Topics

Advanced CMOS (Analog/Digital) EOS/ESD
- ESD Challenges in Advanced Technologies (Multi-gate, FinFET, SOI, SiGe, Compound, Graphene, nanowire, etc.)
- Backside Power design challenges and opportunities
- ESD Challenges in 2.5D & 3D Stacking and TSV

Advanced Bipolar, RF, BCD, and WBG Technologies
- ESD Challenges in Advanced Bipolar, RF, BCD, and WBG Technologies (SiC, GaN, etc.)

Device Testing: Testers, Methods, and Correlation Issues
- Novel EOS/ESD Test and Characterization Methods
- Transmission Line Pulse Testing Systems
- HBM and CDM Tester Issues and Solutions
- Tester Correlation Issues
- Standards – Round-Robin Testing, Results, and Analysis

Chip/Module/Package ESD EDA
- Novel ESD Verification Methodology
- Numerical Modeling and Physics of ESD Events
- ESD Device TCAD and Compact Models
- ESD IP Simulation and Co-Design Methodology
- Application of EDA tools for ESD Failure Analysis

EOS/ESD Failure Analysis and Troubleshooting
- EOS/ESD Case Studies and Analysis
- Failure Analysis Techniques and Interpretations
- Testing of MR/TMR Heads and Ultra-Sensitive Devices
- EOS/ESD Protection for Aircraft, Spacecraft, and Avionics

Latch-up in CMOS, Bipolar, RF, High Voltage, and BCD Technologies
- DC/Transient Latch-up Issues and Prevention, Troubleshooting, Simulation Methodologies

System Level EOS/ESD/EMC, HMM
- System Level EOS/ESD/EMC Test Methods, Modeling, and Simulations
- EOS/ESD Simulators, Calibration, and Correlation
- Transient ESD/EMI Induced Upset
- Case Studies, Reviews, and Analysis

Manufacturing
- ESD Packaging and Handling Procedures
- EOS/EMI/ESD Detection and Measurement Techniques
- EOS/ESD Mitigation in Test and Manufacturing
- EOS/EMC/ESD Process Assessment
- ESD Control Materials and Use of Low Charging Materials
- EOS/ESD Control Program Topics
- Electrostatics modeling, measurement, and instrumentation

Technical Program Chair
Slavica Malobabic, Cirrus Semiconductors

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James Di Sarro, Texas Instruments

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