42nd EOS/ESD SYMPOSIUM AND EXHIBITS

September 13-17, 2020
Peppermill Resort and Casino
2707 S Virginia St, Reno, NV 89502

EXPLORE.

Technical Sessions
Tutorials
Manufacturing Track
Workshops

INNOVATE.

Featured Keynote
Hands-on Demonstrations
Invited Talks
Year-in-Review
IoT Workshop

NETWORK.

Industry Professionals
Social Receptions
Contests
Exhibition

Education Symposium

Co-sponsored by IEEE, EMC Society, The Electron Devices Society, and Reliability Society.

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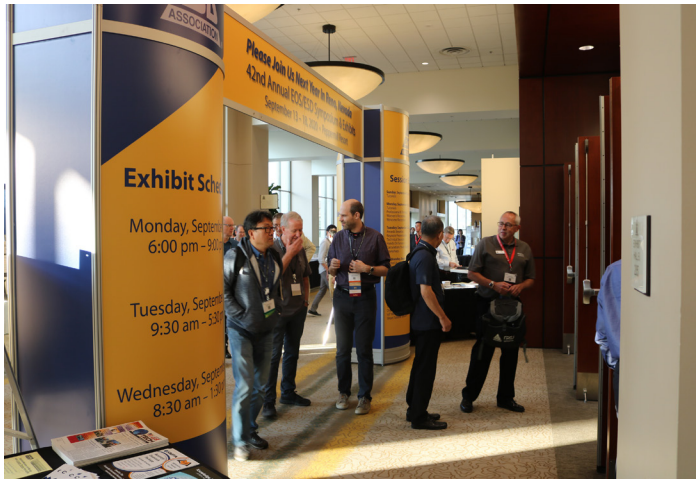

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SUNDAY, SEPTEMBER 13, 2020

Registration	7:30 a.m. - 5:00 p.m.	
Tutorials	8:30 a.m. - 4:30 p.m.	FC100: ESD Basics for the Program Manager
	8:30 a.m. - 12:00 p.m.	DD150: Introduction to RF ESD Design
	1:00 p.m. - 4:30 p.m	DD300: Circuit-Level Modeling and Simulation of On-Chip Protection (DD)

MONDAY, SEPTEMBER 14, 2020

Registration	7:30 a.m. - 5:00 p.m.	
Tutorials	8:30 a.m. - 4:30 p.m.	FC101: How To's of In-Plant ESD Auditing and Evaluation Measurements (PrM)
	8:30 a.m. - 12:00 p.m.	DD340: Integrated ESD Device and Board Level Design
	1:00 p.m. - 4:30 p.m.	DD214: Latchup Physics and Prevention NEW
Exhibits	6:00 p.m. - 9:00 p.m.	Virtual and On-Site Exhibits Open

TUESDAY, SEPTEMBER 15, 2020

Registration	7:30 a.m. - 5:00 p.m.	
Awards Breakfast	7:30 a.m. - 9:00 a.m.	Annual Meeting Breakfast
Keynote	9:00 a.m. - 9:45 a.m.	Keynote: The Role of Photons in Hardware Security
Exhibits	9:30 a.m. - 5:30 p.m.	Virtual and On-Site Exhibits Open
Technical Sessions	10:15 a.m.-10:25 a.m.	Exhibitor Showcase in Session 1A and 1B
	10:25 a.m.-12:05 p.m.	1A: Advanced CMOS EOS/ESD and Latchup
	10:25 a.m.-12:05 p.m.	1B: Device Testing: Testers, Methods and Correlation Issues I
	1:15 p.m. - 1:25 p.m.	Exhibitor Showcase in Sessions 2A and 2B
	1:25 p.m. - 2:15 p.m.	2A: Numerical Modeling and Electronic Design Automation I
	1:25 p.m. - 2:15 p.m.	2B: Device Testing: Testers, Methods and Correlation Issues II
	3:00 p.m. - 3:10 p.m.	Exhibitor Showcase in Sessions 3A and 3B
	3:10 p.m. - 4:00 p.m.	3A: Numerical Modeling and Electronic Design Automation II
	3:10 p.m. - 4:25 p.m.	3B: Device Testing: Testers, Methods and Correlation Issues III
Workshops A	5:10 p.m. - 6:25 p.m.	A.1 ESD Verification Tools: Are We There Yet? A.2 Finding the Step Where ESD failure Occurs in Manufacturing - Process Assessment Meets Event Detection

TUESDAY, MANUFACTURING

Welcome	7:30 a.m. - 9:00 a.m.	Annual Meeting Breakfast
	9:00 a.m. - 9:45 a.m.	Keynote: ESD Control Program Management for the Factory of Tomorrow
Technical Sessions	10:15 a.m. - 11:30 a.m.	Manufacturing 1
	1:00 p.m. - 1:30 p.m.	Technology Showcase 1 - StaticStop/SelecTech, Inc.
	1:30 p.m. - 2:00 p.m.	Technology Showcase 2 - Core Insight, Inc.
	2:25 p.m. - 3:25 p.m.	Panel Session

Important Notice: Due to global events some presenters will appear via live stream, or through a prerecorded presentation. Some presenters will appear virtually for a live Q&A. A technical expert will be present for Q&A.

WEDNESDAY, SEPTEMBER 16, 2020

Registration	7:30 a.m. - 5:00 p.m.	
Exhibits	8:30 a.m. - 1:30 p.m.	Virtual and On-Site Exhibits Open
Technical Sessions	8:00 a.m. - 8:40 a.m.	Year in Review: Electrical Overstress in Manufacturing and Test
	9:10 a.m. - 9:20 a.m.	Exhibitor Showcase in Session 4A
	9:20 a.m. - 10:10 a.m.	4A: EOS/ESD Failure Analysis, Troubleshooting and Case Studies II
	9:10 a.m. - 9:20 a.m.	Exhibitor Showcase in Session 4A
	9:20 a.m. - 10:10 a.m.	EMC (Invited) I
	10:35 a.m. - 11:25 a.m.	EMC (Invited) II
	10:35 a.m. - 10:45 a.m.	Exhibitor Showcase in Session 5A
	10:45 a.m. - 11:35 a.m.	5A: Numerical Modeling and Electronic Design Automation III
	1:20 p.m. - 3:20 p.m.	**EMC Short Tutorials**
	1:20 p.m. - 2:00 p.m.	**Tutorial I. ESD Testing in accordance with IEC 61000-4-2**
	1:40 p.m. - 1:50 p.m.	Exhibitor Showcase in Session 6A
	1:50 p.m. - 3:40 p.m.	6A: Published Posters
	2:00 p.m. - 2:40 p.m.	**Tutorial II. System Level ESD Design Considerations and a Means of Evaluation**
	2:40 p.m. - 3:20 p.m.	**Tutorial III. Lessons-Learned in System-Level ESD Testing**
	3:40 p.m. - 4:20 p.m.	**Tutorial IV. System-Level ESD Failure Mechanisms and Mitigation Techniques**
	4:20 p.m. - 5:00 p.m.	**Tutorial V. EMI Measurements in Manufacturing Environment**
Workshops B	5:25 p.m. - 6:40 p.m.	B.1 ESD Education in the Field
		B.2 EMC Expert Panel

WEDNESDAY, MANUFACTURING

Technical Sessions	8:00 a.m. - 8:50 a.m.	Manufacturing II
	9:15 a.m. - 9:45 a.m.	Technology Showcase 3 - ORBIS Corporation
	9:45 a.m. - 10:15 a.m.	Technology Showcase Hands-On
Workshop	10:45 a.m. - 12:00 p.m.	Manufacturing Workshop - Assessment, Selection, and Qualification of Materials and Equipment Used in the EPA

THURSDAY, SEPTEMBER 17, 2020

Registration	7:30 a.m. - 5:00 p.m.	
	8:00 a.m. - 8:40 a.m.	Year in Review: ESD On-chip Design
Tutorials	8:30 a.m. - 12:00 p.m.	FC391: Basics of ESD Process Assessment
	8:30 a.m. - 12:00 p.m.	DD/FC240: System Level ESD/EMI: Principles, Design Troubleshooting, & Demonstrations
Technical Sessions	9:05 a.m. - 10:20 a.m.	8A: System Level EOS/ESD/EMC
Virtual Exhibits Only	10:00 a.m. - 2:00 p.m.	Virtual Exhibits Only
	10:45 a.m. - 12:25 p.m.	8A: System Level EOS/ESD/EMC (continued)
	9:05 a.m. - 10:20 a.m.	8B: Invited IRPS
	10:45 a.m. - 12:00 p.m.	8B: Invited IRPS (continued)
Tutorials	1:00 p.m. - 4:30 p.m.	FC121: Grounding – Variations, Concepts, Nuisances, Equipment & Troubleshooting
	1:00 p.m. - 4:30 p.m.	DD/FC130: System Level ESD/EMI: Testing to IEC and Other Standards (DD)

Important Notice: Due to global events some presenters will appear via live stream, or through a prerecorded presentation. Some presenters will appear virtually for a live Q&A. A technical expert will be present for Q&A.

KEYNOTE

Tuesday, September 15
9:00 a.m. - 9:45 a.m.

The Role of Photons in Hardware Security

Dr. Shahin Tajik, Florida Institute for Cybersecurity (FICS) Research at the University of Florida

Live-Stream

A wide variety of deployed embedded devices in consumer, industrial, and military applications is the target of reverse-engineering and Intellectual Property (IP) piracy. The main motivation behind reverse-engineering is to get access to the stored secrets and employed IPs on the integrated circuits (ICs) to counterfeit and overbuild the target products. Cloning of a design can be carried out by mounting physical attacks, such as side-channel analysis. Although modern ICs have integrated several countermeasures to mitigate such attacks, a proper protection scheme against optical attacks conducted from the IC backside is still missing. The primary reason that the IC backside protection is ignored by the vendors is the misconception that optical attacks cannot be scaled to the very latest nanoscale technologies without further effort and cost. In this talk, we assess the attack effort against commercial devices in real scenarios, where the adversary has no knowledge of underlying hardware implementation. We demonstrate that the adversary is able to extract the sensitive design information and intellectual property (IP) from the target device in a short amount of time, with a limited budget. Finally, we propose and discuss potential countermeasures, which could protect the chips against optical attacks mounted from the IC backside.

Dr. Shahin Tajik is an Assistant Research Professor at Worcester Polytechnic Institute (WPI). Before joining WPI, Dr. Tajik was an Assistant Research Professor at the Florida Institute for Cybersecurity (FICS) Research at the University of Florida. He received his Ph.D. degree in Electrical Engineering in 2017 from the working group SECT, a collaboration of the Technical University of Berlin and Deutsche Telekom Innovation Laboratories in Germany. His field of research includes non-invasive and semi-invasive attacks, Physically Unclonable Functions (PUFs), security evaluation of FPGAs, and providing tamper protection mechanisms against attacks conducted from the IC backside. His ACM CCS'17 paper with the title "On the Power of Optical Contactless Probing: Attacking Bitstream Encryption of FPGAs" was awarded the 1st place in Applied Research Competition of European Cyber Security Awareness Week (CSAW) in 2017.

EOS/ESD Association, Inc. Professional Certification

EOS/ESD Association, Inc. offers professional certification for ESD control program managers and device design technical specialists.

ESD Certified Professional-Program Manager

The impact of the ANSI/ESD S20.20 ESD control program standard on the global industry has been extraordinary. As a result, EOS/ESD Association, Inc. recognizes the need to offer a certification program for individuals that are involved in designing, implementing, managing, and auditing ESD control programs in their facilities. The program manager certification program serves that purpose. In addition, the needs of the technical community for certification of various technical specialists are apparent.

Requirements for certification include attending required prerequisite tutorials and passing a final exam. All of the prerequisite courses cannot be completed by attending only the 2020 Symposium. Details of the certification program are also available at the registration desk.

The preferred tutorial sequence for the program manager curriculum is:

	COURSE TITLE	FACE TO FACE TUTORIAL	ONLINE
1	FC100: ESD Basics for the Program Manager	Symposium, Sunday, Sept. 13	
2	FC101: How To's of In-Plant ESD Auditing and Evaluation Measurements	Symposium, Monday, Sept. 14	
3	FC110: Cleanroom Considerations for the Program Manager		Online Academy
4	FC120: Air Ionization Issues and Answers for the Program Manager		Online Academy
5	FC200: Packaging Principles for the Program Manager		Online Academy
6	FC210: ESD Standards Overview for the Program Manager		Online Academy
7	FC140 - System Level for the Program Manager		Online Academy
8	FC220: Device Technology and Failure Analysis for the Program Manager		Online Academy
9	FC380: Electrostatic Calculations for the Program Manager and the ESD Engineer		Online Academy
10	FC340: ESD Program Development & Assessment (ANSI/ESD S20.20 Seminar)		

ESD Certified Professional-Device Design

ESD device design certification was developed for individuals that are involved in designing, testing, characterizing, and implementing improved ESD protection designs. Device design certification demonstrates knowledge, experience, and competency in the area of ESD design and test for device protection.

Requirements for certification include attending required prerequisite tutorials and passing a final exam. All of the prerequisite courses are not available in the 2020 Symposium tutorial program. Details of the certification program are also available at the registration desk.

The preferred tutorial sequence for the device design curriculum is:

	COURSE TITLE	FACE TO FACE TUTORIAL	ONLINE
1	DD110: ESD Basics for Advanced Protection Design		Online Academy
2	DD301: SPICE-Based ESD Protection Design Utilizing Diodes and Active MOSFET Rail Clamp Circuits		
3	DD211: EOS/ESD Failure Models and Mechanisms		
4	DD102: On-Chip ESD Protection in RF Technologies		Online Academy
5	DD200: Charged Device Model Phenomena, Design, and Modeling		Online Academy
6	DD112: Latch-up Fundamentals		Online Academy
7	DD300: Circuit-Level Modeling and Simulation of On-Chip Protection	Symposium, Sunday, Sept. 13	
8	DD302: Troubleshooting On-Chip ESD Failures		
9	DD120: Device Testing--IC Component Level: HBM, CDM, MM, and TLP		
10	DD311: Impact of Technology Scaling on ESD High Current Phenomena and Implications for Robust ESD Design		Online Academy
11	DD220: Transmission Line Pulse (TLP) Basics and Applications		Online Academy
12	DD/FC130: System Level ESD/EMI: Testing to IEC and other Standards	Symposium, Thursday, Sept. 17	Online Academy

ESDA Certification Exams

The certified professional program manager and device design exams will be held on Friday, September 18. To take the exam, applicants must have a registration form on file with EOS/ESD Association, Inc. headquarters complete with a $50 filing fee prior to the Symposium.

FC100: ESD Basics for the Program Manager

8:30 a.m. - 4:30 p.m.

Pre-recorded class. Instructor live-stream for Q&A

Ted Dangelmayer, Terry Welsher, Dangelmayer Associates, LLC.

Certification: PrM

Abstract

This tutorial provides the foundation material for understanding electrostatics and ESD and their role in the manufacturing and handling of ESD sensitive devices. The fundamental properties of charge, electric fields, voltage, capacitance, and current are discussed with a view towards understanding key electrostatic phenomena and electrical processes. These include charge gener ation and decay, material properties, and induction. An overview of device failure mechanisms is presented, including how these models impact ESD control programs. Finally, the course provides an overview of ESD control procedures during handling and manufacturing and an overview of ANSI/ESD S20.20 program requirements. This full day course is required for those in-plant auditors and program managers who are working toward professional ESD certification. The presentation includes many in-class demonstrations, videos, and animated slides.

Some sample topics covered in this course are:

1. Definitions and relationships among important electrical and mechanical properties
2. Causes of charge generation and decay
3. Field effects and voltages
4. Role of capacitance in ESD (Q=CV)
5. Overview of key measurements including common pitfalls of some measurements
6. Review of ESD failure models
7. Understanding and demonstrating electrostatic induction
8. Utility and limitations of air ionization
9. Basic goals of ESD controls
10. Properties of effective ESD control products and materials
11. Overview of ANSI/ESD S20.20 ESD program development requirements

Learning Outcomes

- An understanding of several concepts that are included in the ESD Program Manager Certification Exam
- A deep understanding of ESD fundamentals that are vitally important for developing and managing sound ESD programs
- Students will learn effective techniques for demonstrating a wide range of ESD fundamentals
- Students will learn how to evaluate materials for CDM mitigation properties and much more

DD150: Introduction to RF ESD Design

8:30 a.m. - 12:00 p.m.

Instructor Life-Stream

Kathleen Muhonen, Qorvo

Abstract

This tutorial is an introduction to RF concepts and RF ESD clamp design. It is intended for ESD engineers who do not have an RF background to come up to speed on the concepts needed to design effective protection circuits. The RF concepts include impedance matching and smith chart basics. RF amplifier operation and load line basics are presented to give a foundation for the RF ESD protection circuit design. The tutorial will also touch briefly on RF switches and filters. The second half of the tutorial will focus on how to design an ESD clamp for an RF application. Concepts will be presented such as calculating the turn-on voltage of the clamp such that it will protect the part but not turn on during normal, RF operation. To design successful RF ESD clamps, concepts such as peak-to-average power ratio will be explained for common cellular and WiFi standards. A clamp's parasitics also needs to be considered in an RF application so that the parasitics do not degrade the product's performance. Finally, some testing tools will be reviewed with respect to evaluating RF products. The challenges will be highlighted and different testing practices that are used in HBM, TLP and IEC testing of RF products will be reviewed.

Learning Outcomes

Learning outcomes are understanding of the following:

- Key RF and microwave concepts such as maximum power transfer, impedance matching and smith chart basics
- How components such as amplifiers, switches and LNA's have different metrics of performance for RF applications
- What RF parameters are needed to design a functional RF ESD clamp without RF performance degradation
- What to consider when determining the ESD robustness of an RF product

DD300: Circuit-Level Modeling and Simulation of On-Chip Protection

1:00 p.m. - 4:30 p.m.

Instructor Live-Stream

Elyse Rosenbaum, University of Illinois at Urbana-Champaign

Certification: DD

Abstract

This tutorial addresses modeling of on-chip ESD protection devices and simulation of ESD protection networks. The primary focus is SPICE-type simulation with compact (physics-based) models but a brief survey of other modeling approaches and simulation techniques will be provided.

The physical operating principles of commonly-used ESD protection devices will be examined. The high-current characteristics and transient responses of those devices will be explored to ascertain what behaviors should be captured by a model intended for circuit-level simulation of ESD.

Specific examples of model implementations will be provided. Techniques for circuit-level modeling of self-heating will be presented. Parameter extraction and model scalability will be addressed. This tutorial assumes some familiarity with device physics. It is directed toward persons with interests in semiconductor device physics, electronic design automation, and on-chip ESD protection circuit design.

Learning Outcomes

After completion of this tutorial, a student should know how to set up a netlist for simulation of an on-chip ESD protection networks. Students will have the necessary background to start developing their own compact models and will be familiar with resources for Verilog-A model development.

FC101: How To's of In-Plant ESD Auditing and Evaluation Measurements

8:30 a.m. - 4:30 p.m.

Pre-recorded class. Instructor Live-Stream for Q&A

Ted Dangelmayer, Ginger Hansel, Dangelmayer Associates LLC.

Certification: PrM

Abstract

Compliance verification is one of the most important elements of ESD program management and there are many technical and administrative pitfalls that can be avoided. The attendee will learn not only how to make valid auditing measurements in accordance with ESD TR53 – Compliance Verification of ESD Protective Equipment and Materials, but also how to rec ognize and avoid common pitfalls. Common instruments will be explained as well as the invalid test results that can result when they are used incorrectly. Advanced auditing techniques will also be covered that enable Class 0 devices to be handled successfully. There are many ways to administer effective compliance verification programs. Two successful examples will be presented that were developed independently by differ ent companies. Hidden administrative pitfalls that often result in poor compliance will also be discussed. This tutorial will be highly interactive with live demonstrations, in-plant photo graphs, and compelling video clips. Students will be encour aged to ask questions and to participate in the discussions.

Learning Outcomes

-Understand auditing information included in ESD Program Manager Certification Exam
-Learn to make and correctly interpret auditing measurements based on ESD TR 53
-A deep understanding of five auditing options for sustaining program execution excellence
-Understand the critical requirements to successfully handle extremely sensitive Class 0 devices
-Develop real world solutions from the review of successful case studies and class discussions

DD340: Integrated ESD Device and Board Level Design

8:30 a.m. - 12:00 p.m.

Instructor Live-Stream

Harald Gossner, Intel Deutschland GmbH.

Abstract

The tutorial is a hands-on training course for performing a simulation based optimization of PCB ESD protection design and provides deep understanding of the relevant performance criteria both of TVS diodes and IO circuits. The presented method follows the system efficient ESD design (SEED) approach as recommended by the Industry Council on Target Levels and JEDEC. The method allows the achievement of correct first time PCB builds and reduces the respin effort for boards and ICs. Based on a TLP characterization of SoC interface circuits and TVS diodes, simulation models for impedance and clamping behavior, as well as failure threshold, are extracted. These are used to assess design solutions by transient simulations. This is showcased by real world examples.

Learning outcomes

The attendee will understand the concept of SEED simulation and will be able to apply it to an own PCB /IC codesign simulation. This will allow the system design attendee to run a pre-hardware optimization of the board protection and it will enable the IC protection engineer to evaluate his protection concept regarding the available design window for system ESD.

NEW DD214: Latchup Physics and Prevention

1:00 p.m. - 4:30 p.m.

Instructor Live-Stream

Nathan Jack, Intel Corporation

Abstract

Latchup has occurred in CMOS technologies since their inception and continues as a threat in modern finFET technologies. This course will begin with a basic overview of the latchup phenomenon and then dig deeper into the theory and physics associated with it. Latchup mitigation techniques will be reviewed along with the physics behind them. These will include both design and process techniques. The basics and pitfalls of latchup testing will be taught, along with an introduction into transient latchup. Proper wafer-level test structure design and characterization will be taught.

The primary audience for this course is design and reliability engineers tasked with designing for latchup success. Latchup test engineers will also benefit from a deeper understanding of latchup physics and design practices. The course assumes some familiarity with basic circuit design practices and semiconductor physics. Participants will leave with a deeper understanding of the physics behind latchup, its mitigation, and the impact of future technology trends on latchup susceptibility.

Learning Outcomes

--Understand the physics behind latchup

--Understand how technology scaling impacts latchup

--Learn latchup mitigation strategies in design and process development and the physics behind them.

--Will learn best practices for test structure creation and measurement and how to translate the results into latchup design rules.

--Will understand the latchup test standard in the context of creating design rules to successfully pass the test as well as other real-world risks not covered by the standard.

FC391: Basics of ESD Process Assessment

8:30 a.m. - 12:00 p.m.

Instructor Live-Stream

Wolfgang Stadler, Intel Deutschland GmbH.; Reinhold Gaertner, Infineon Technologies

Abstract

This tutorial gives an introduction to the approach and measurement methodologies for ESD process assessment and ESD risk analysis in typical production processes in semiconductor, printed-circuit board (PCB), and electronic system manufacturing industries. To large extents, the tutorial follows the ESD process assessment approaches described in ANSI/ESD Standard Practice SP17.1.

The tutorial summarizes the relevant physical parameters, for example, resistance, charge, electric fields, capacitances, resistances, discharge currents, and ESD event detection by EMI. The influence of these parameters on the ESD risks caused by charged personnel, charged devices and boards, and ungrounded conductors is discussed. Also, measurement techniques are explained in detail together with their limitations for the different process steps and strategies for an efficient ESD risk assessment. The application of those measurement techniques to assess possible ESD risks and to solve ESD problems are explained using theoretical and real-world case studies from many of the processes mentioned above. Examples of possible mitigation strategies are discussed with the attendees. The tutorial includes practical demonstrations and a hands-on session for the attendees to get experience and learn pitfalls of the most important measurement techniques used in ESD process assessment.

Learning Outcomes

The attendees will be enabled to analyze ESD critical process steps, select the appropriate measurement technique, and perform the measurement. They will learn how to evaluate the measurement results and assess the ESD risk in various typical process steps.

DD/FC240: System Level ESD/EMI: Principles, Design Troubleshooting, & Demonstrations

8:30 a.m. - 12:00 p.m.

Instructor On-Site

Jay Skolnik, Skolnik Technical Training

Abstract

System level ESD tutorial about how to reduce ESD effects on systems (boards, chassis, etc.). Real circuits will be demonstrated in class showing techniques to correct the detrimental effects. Theory and real-life examples from recent past will be used to substantiate the methods.

Learning Outcomes

•Understand how an ESD soft failure can upset a system and how to design to eliminate soft ESD failures

•Realize how ESD and electrical noise can enter a system and acquire methods to locate / remove the issues from ESD and electrical noise based on electric & magnetic field edification

•Encounter new methods to make a circuit board design more robust against direct ESD hits to a connector pin

•Assess the Faraday Shield principle and learn to apply it directly to applications in order to reduce detrimental ESD/EMI effects

FC121: Grounding – Variations, Concepts, Nuisances, Equipment & Troubleshooting

1:00 p.m. - 4:30 p.m.

Instructor On-Site

Jay Skolnik, Skolnik Technical Training

Abstract

Grounding for ESD control seems so simple, yet many times issues arise after a grounding strategy is implemented. This class will cover variations in grounding approaches, concepts to consider when employing a ground system, nuisances and how to troubleshoot them with the correct equipment.

Learning Outcomes

- Understand the term “ground” and all of its associated meanings from the industry in order to test, measure and/or design effective ground systems.
- Understand the various ESDA standards and test methods in regards to measuring ground connections.
- Realize the reason for a Common Point Ground and how to achieve it.
- Determine the right amount of resistance, (not too little and not too much) for many ESD control situations.
- Determine how to troubleshoot typical ground issues in order to maximize productivity.

DD/FC130: System Level ESD/EMI: Testing to IEC and Other Standards

1:00 p.m. - 4:30 p.m.

Instructor Live-Stream

Jeff Dunnihoo, Pragma Design, Inc.

Certification: DD

Abstract

This tutorial is intended to help those tasked with testing products to system level ESD standards by providing first an overview of how real-world system ESD events are simulated in different standards and testers in general, and then provide detailed information on IEC 61000-4-2, the most widely used standard. This introduction will highlight the similarities and differences between IEC, ANSI, Telcordia, and some automotive ESD standards. We will answer common questions regarding test setups, test points, and procedures, and address key issues, including: 1) differences between “verification” and “calibration” and when is each required; 2) test equipment requirements, the test environment, ground connections, return paths, and ground plane effects. 3) Testing procedures with demonstration on actual products, how the tester and procedure affects test results, and problems with test result variations due to simulator influences; 4) definitions of testing failure criteria for the product; 4) what points need to be tested and why, guidance on determining “operator accessible” points and ports, exempted points and ports, and what to do around connectors and connector pins. 5) ANSI and other ESD standards, the drive toward harmonization with IEC, the scope of different standards, and why they are unlikely to converge. This system level ESD tutorial will cover different perspectives on ESD as applied to electronic systems from the user’s, the designer’s, and even the designer’s competitor’s points of view.

DD200: Charged Device Model Phenomena, Design, and Modeling

On-Demand Tutorial

Michael Chaine, Micron Technology, Inc.; Melanie Etherton, NXP Semiconductors

Certification: DD

Abstract

This course teaches basic ESD circuit design concepts and ideas required to design ESD protection for Charge Device Model ESD tests. The course covers a brief history of CDM ESD development, charge and discharge physics, characterization methods, CDM failures mechanisms, and CDM design-in strategies.

CDM ESD circuit design approaches and simulation setups for CDM failure debugging are presented in this tutorial on the basis of case studies. Insight into CDM circuit simulation requirements and physical aspects of the CDM ESD phenomenon that are important for reproducing the event with circuit simulation will be taught and modeling approaches for CDM specific device physical effects necessary for accurate circuit simulation will be introduced. This course also teaches methods for simplified CDM circuit simulations where detailed information is either not available or too complex to simulate.

The course focuses on what type of circuits fail during a CDM discharge event and teaches the different types of ESD design circuit strategies that can be applied to protect those circuits. This class covers basic to advanced topics for CDM ESD design, but the student is assumed to already have a basic understanding of the CDM test method.

Learning Outcomes

The attendees of this class are expected to have an improved understanding of the basics of charging of an IC component, CDM discharge event physical effects, internal circuit damages caused by the voltage and current during fast transient discharges and basic high current properties of ESD protection circuits in the CDM time domain. They should have an improved appreciation of circuit simulation methods for designing CDM ESD protection and for debugging failures caused by CDM ESD with circuit simulations. They should be able to apply ESD design strategies as discussed in the tutorial that have proven to protect ultra thin gate oxides of input circuitry and of devices connecting to signals that cross power domains techniques and strategies to protect cross domain circuits.

DD100: ESD Circuits

On-Demand Tutorial

Eugene Worley, Silicon Crossing, LLC.

Abstract

This tutorial will focus on a number of clamp approaches including BigFETs or RC clamps, snap-back NFETs, diodes, SCRs including HV SCRs, low capacitance clamps methods including those for MOSFET based LNAs and RF transceiver switches, and cross domain clamping. Spice simulations and simple models where applicable will be used to design and analyze circuit performance. Models include HBM, CDM, and IEC sources, gate pull requirements for dynamically lowering snap-back thresholds, and diodes. Gate pull for snap-back NFETs will include cascade and stacked NFETs. The need for NQS MOSFET models will be discussed with respect to CDM simulations. Operational characteristics of diodes will be examined including simple models and turn on delay. Diode types to be examined include STI, gated, and gated with LDD block. Protecting RF transceiver switches will be studied and will include spice simulations and design of low capacitance snap-back NFETs. Cross domain analysis will feature SPICE-based gate oxide rupture models and design requirement for secondary clamps including secondary clamps for LNAs.

Learning Outcomes

The attendee will learn how to design BigFETs clamps, gate pull snap-back clamps, types of SCRs, and circuit protection networks. There will be an emphasis on circuit simulation for design and circuit models including failure mechanisms, tester models, pin interconnect parasitics, and diodes.

DD240: ESD Device Qualification Testing

On-Demand Tutorial

Brett Carn, Intel Corporation; Wolfgang Stadler, Intel Deutschland GmbH.

Abstract

This tutorial addresses the details of both Human Body Model (HBM) and Charged Device Model (CDM) qualification testing. This course will help in interpretation of the HBM joint standard JEDEC/ANSI/ESD JS-001-2014 including the following details: Waveform verification, understanding of Table 2A (minimum required set of pin combinations) and Table 2B (legacy pin combinations), pin categorization and pin grouping, I/O pin sampling, stress plans details including efficient testing (reduction in pin count) and some debugging options. In addition, this course will discuss CDM testing details regarding waveform verification, stress plans, peak current (Ipeak) variability and how does it affect the testing results, and debugging options as well as an overview on the new CDM joint standard JEDEC/ANSI/ESD JS-002-2014.

Learning Outcomes

The attendee should come away with a stronger understanding of both human body model (ANSI/ESDA/JEDEC JS-001 - HBM) and charged device model (ANSI/ESDA/JEDEC JS-002 – CDM) testing specifications and the requirements called out in each of these specifications. For HBM this includes a better understanding of Table 2A and Table 2B and the use of association in Table 2A as well as opportunities to minimize test time and an understanding of cloned IO requirements. For CDM this includes a better understanding of the waveform verification requirements and the impacts of an air discharge on product qualification.

DD311: Impact of Technology Scaling on Components High Current Phenomena and Implications for Robust ESD Design

On-Demand Tutorial

Gianluca Boselli, Texas Instruments

Abstract

This advanced tutorial will focus on high-current behavior of stand-alone components, with the aim of optimizing effectiveness of ESD clamp devices (irrespectively of their schematic implementation) and maximizing the ESD SOA (Safe Operating Area). Components in both Analog and Digital technologies will be discussed, with emphasis on technology trends. This class is intended for individuals who have taken the basic on-chip protection class and are familiar with the basic device physics for both ESD and latch-up.

Learning Outcomes

1. Understand the physics of basic components under high current conditions with particular emphasis on scaling aspects (geometrical (i.e. W & L), power (following Wunsch-Bell power curve) and electrical (rise time)
2. Understand how to experimentally extract high current characteristics
3. To optimize ESD protection circuits based on fundamental components behavior

DD231: ESD System Level: Physics, Testing, Debugging of Soft and Hard Failures

On-Demand Tutorial

David Pommerenke, Graz University of Technology

Abstract

The tutorial is an expanded version of the previous DD231 tutorial on system level ESD. The main difference is the addition of many experimental demonstrations, update of information, and in-depth discussion on problems of the IEC 61000-4-2 testing, with examples on how to perform this testing and obtain the best possible results and documentation. About half of the time will be spent on experimental demonstrations. Topics will include:

- ESD physics: charging and discharging.
- System level ESD testing
- System level soft failure mechanisms and debugging
- Design for avoiding ESD problems

Learning Outcomes

The seminar will enable the audience to better understand system level ESD testing such that meaningful, repeatable tests can be performed and data is gathered, that allows to identify the root cause of observed failures.

FC166: ESD QMS Best Practices Strategy Including Class 0 and Costly Controversial ESD Myths

On-Demand Tutorial

Ted Dangelmayer, Dangelmayer Associates, LLC.

Abstract

Part I: ESD QMS Best Practices Strategy Including Class 0

While most companies are acutely aware of the hazards of ESD (electrostatic discharge), few are aware that the ESD QMS Strategy is equally important as the technical requirements. This is especially true for the extreme ESD sensitivities of Class 0 since the trend toward Class 0 devices is escalating rapidly. Furthermore, most companies do not know what their device sensitivities are because 90% of IC datasheets do not include CDM Sensitivity data. The absence of this data and the lack of understanding of ESD QMS best practices has reached a critical stage.

S20.20 (ANSI/ESD S20.20) is the best industry standard available and is an excellent foundation for ESD QMS best practices programs. However, companies with advanced technologies have found they must customize the technical requirements of S20.20 and introduce sound ESD QMS practices to avoid unacceptable failure rates in the factory and field. Join us for this interactive presentation and learn if you are at risk and how to establish a robust ESD QMS strategy. You will also learn how to obtain ESD CDM & HBM device sensitivity data as well as how to prepare for Class 0.

Part II: Costly Controversial ESD Myths

There are several common misunderstandings and controversies that can have significant impact on costs, quality and reliability of ESD programs. These misunderstandings or "myths" often result in costly unnecessary expenditures and/or a compromise of the program integrity. These same myths are cited by skeptics who do not fully understand the physics involved. Consequently, it is important to identify and dispel these myths.

Latency is a significant reliability consideration that is surrounded with controversy. Some experts will argue that latency is virtually non-existent while others claim that it is the dominant failure mode. Join us for this highly interactive discussion and learn about Latency as well as common myths such as:

Myth: Circuit Boards are Less Sensitive to ESD than Devices
Myth: HBM Data Are Sufficient for Determining Device Sensitivity Levels
Myth: MM Is A Valid Simulation Related To Machines
Myth: Air Flow Causes Charging
Myth: Metalized or Highly Conductive Shielding Layers Are Essential
Myth: Humidity Control is Essential for ESD
Myth: Latency Failures Comprise 90% of ESD Failures

Learning Outcomes

- A Deep Appreciation for The Importance of A Solid ESD QMS Strategy
- How To Include Class 0 In The QMS Strategy
- The Importance of Fully Understanding ESD Fundamentals and Advanced Technology
- How Many ESD Myths Can Disrupt the Best of ESD Programs And How To Prevent This From Happening
- A Review of Important Technical Concepts Such as CDM And CBE

NEW DD208: ESD Parameters for the Foundry, IC Designer and IP/EDA Vendor

On-Demand Tutorial

Efraim Aharoni, Tower Semiconductor

Abstract

ESD devices and protection circuits should demonstrate an effective shunting and clamping of ESD stress in ICs and electronic systems. It should also not influence the proper functionality of the protected system. The trade-off between ESD capability and signal integrity is reflected in key ESD parameters extracted from dedicated measurements. The ESD protection, planned at IC design level, requires information and data exchange between foundry supplier, IP vendor, and IC designers, and EDA tools vendors. This tutorial aims in guiding the ESD engineer in the foundry in the process of creation and supplying the ESD portion of the PDK. In particular providing a variety of special parameters required for design of an optimized ESD protection. This includes an overview of benchmark key ESD parameters, test structures, measurements, extraction methods, and useful presentation of the information. The designer and the EDA tool vendor are equipped with the know-how of using the parameters in optimizing the ESD window as well as developing effective methods of proper ESD protection, ESD checkers and simulations. As part of this tutorial, two technical reports ESD TR22.0-01-14 (Relevant ESD foundry parameters for seamless ESD design and verification flow) and ESD TR22.0-02-18 (ESD parameters from Intellectual Property (IP) providers), written by ESDA 'ESD parameters' WG-22, are reviewed.

Learning Outcomes

1. Learn about the required ESD-related deliverables that the foundry should provide to its design customers and IP/EDA tools vendors. In formal words, the ESD ingredients of the Process Design Kit (PDK).
2. Understand the benchmark methods for creation and extraction of ESD-related data, including test-structures, measurement procedures and tools, as well as presentation of key parameters, curves, etc. This know-how covers a variety of technologies ranging from CMOS, RF, embedded NVM, to high voltage BCD.
3. Learn about possible monitoring of ESD parameters, protection performance, interference to normal operation, and robustness to process variation.
4. Exposure to the inter-relations between the foundry, the IC designer, IP vendors, and EDA tools vendors, from the ESD perspective. In particular, the data exchange between foundry supplier, IP vendor, EDA tool vendor, and IC design integration.

TUTORIALS: On-Demand

DD220: Transmission Line Pulse (TLP) Basics and Applications

On-Demand Tutorial

Evan Grund, Grund Technical Solutions, Inc.

Certification: DD

Abstract

This tutorial will cover the basics of TLP including underlying theory, the types of TLP systems available, and how I-V curves are extracted from TLP pulses. The tutorial uses examples to show how fundamental device parameters can be measured with TLP. These parameters allow the ESD engineer to understand a technology's properties which can be used to design successful ESD protection circuits. The student will gain an understanding of the purpose of TLP measurements, how TLP relates to HBM and CDM, fundamentals of how TLP systems work, including impedance and refl ections, types of TLP systems, importance of load lines, adaptive ranging, TLP calibration, time dependence from TLP, and biased TLP measurements. The tutorial will present examples of TLP use for nMOS transistors, diodes, oxides/capacitors, and power supply clamps, as well as time dependent TDR-O and VF-TLP examples.

Exhibitor Showcase 10:15 AM-10:25 AM

Magwel NV

Session 1A: 10:25 AM-12:05 PM

1A: Advanced CMOS EOS/ESD and Latch-up

Co-Moderators: Scott Ruth, AMD; Markus Mergens, QPX

1A.1 Latchup Test Structure Optimization in Advanced CMOS Technologies

Collin Reiman, Nathan Jack, Intel Corporation

Latchup sensitivity is often measured with a single collinear PNPN test victim. This method is insufficient for measuring the latchup performance of advanced CMOS technology because it does not represent real-world designs. As a result, the predicted latchup performance is too optimistic. In this work, more realistic latchup test structures are discussed. By adopting these new structures, a more accurate prediction of latchup sensitivity can be measured, leading to better latchup prevention.

1A.2 ESD Protection Diodes in Sub-5nm Gate-All-Around Nanosheet Technologies

Shih-Hung Chen, Anabela Veloso, Hans Mertens, Geert Hellings, Marko Simicic, Wen-Chieh Chen, Wei-Min Wu, Kateryna Serbulova, Dimitri Linten, Naoto Horiguchi, imec

A Gate-All-Around (GAA) nanosheet (NS) transistor is a candidate for sub-5nm bulk Si CMOS. The impact of the new architecture and relevant process options on intrinsic ESD performance needs to be studied. The first measured results show GAA NS ESD diode performance is strongly influenced by dual epitaxy process options.

1A.3 Analytical Model and Verification Algorithm to Prevent Injection Induced Latchup Failures

David Marreiro, Slavica Malobabic, Vladislav Vashchenko, Maxim Integrated Corp.

Unexpected latchup qualification test failures of HV analog integrated circuit were observed and explained by a new mechanism - injection current upset of internal HV blocks resulting in overload and burnout of LV circuits. A novel verification algorithm is implemented based on analytical model calibrated with latchup test structures data.

1A.4 Increased Latch-up Susceptibility of ICs using Reverse Body Bias

Sandeep Vora, Elyse Rosenbaum, University of Illinois at Urbana Champaign; Michael Stockinger, NXP Semiconductors

This work presents a previously undocumented cause of latch-up in circuits with reverse body bias capability. This latch-up phenomenon was first noticed during power-on ESD testing. The latch-up risk is determined by the biasing scheme and power delivery network. SPICE simulations are used to confirm the cause and evaluate counter-measures.

Exhibitor Showcase: 10:15 AM-10:25 AM

iT2 Technologies,LLC

Session 1B: 10:25 AM-12:05 PM

1B - Device Testing: Testers, Methods and Correlation Issues I

Moderator: Brett Carn, Intel Corporation

1B.1 Impact of Alternative CDM Methods on HV ESD Protections Behavior

Leonardo Di Biccari, Andrea Boroni, Alessandro Castelnovo, Lucia Zullino, Lorenzo Cerati, Antonio Andreini, STMicroelectronics; Heinrich Wolf, Johannes Weber, Fraunhofer EMFT

Alternative CDM methods show a good correlation with Field Induced CDM on failing peak current for products not affected by recovery effects. Methods correlation using HV technologies impacted by Forward Recovery Effects, considering multiple DUT impedance variations and rise time impact, is investigated by means of characterizations and TCAD simulations.

1B.2 Optimization of Wafer-Level Low-Impedance Contact CDM Testers

Marko Simicic, Shih-Hung Chen, imec; Wei-Min Wu, imec, KU Leuven, National Chiao Tung University; Nathan Jack, Intel Corp.; Shinichi Tamura, Yohei Shimada, Masanori Sawada, Hanwa Electronic Ind.

The low-impedance contact CDM (LICCDM) ESD tester can be used for wafer-level CDM testing. However, compared to the industry standard field-induced CDM (FI-CDM), it shows some differences. We investigate solutions to mitigate these differences which are mainly the wafer chuck influence and the probe reflections due to matching.

1B.3 Charged Device Model (CDM) and Capacitive Coupled Transmission Line Pulsing (CC-TLP) Stress Severity Study on RF IC's

Dolphin Abessolo-Bidzo, Victoria Kiriliouk, Sheela Verwoerd, NXP Semiconductors; Johannes Weber, Heinrich Wolf, Ellen Jirutková, Fraunhofer EMFT

This paper studies the CDM stress severity on RF IC's. The IC's are housed in various IC packages sizes and tested with both CDM and CC-TLP test methods. Empirical correlation factors are established based on peak current and energy content driven failure mechanisms of RF pins.

1B.4 A Relay Discharged FI-CDM Method for Improved Repeatability

Matthew Drallmeier, Wei Huang, ESDEMC Technology LLC; David Pommerenke, Graz University of Technology

A new design for CDM testing is proposed that retains the field charging DUT method while providing a consistent discharge inside of a reed switch. The method is shown to adhere to the current JS-002 industry standard and to perform with high repeatability and at low charging voltages.

Exhibitor Showcase: 1:15 PM-1:25 PM

Estatec, LLC

Session 2A: 1:25 PM-2:15 PM

2A: Numerical Modeling and Electronic Design Automation I

Moderator: Gernot Langguth, Infineon Technologies

2A.1 Addressing Latch-up Verification Challenges of 2.5D/3D Technologies

Dina Medhat, Ain Shames University, Mentor, a Siemens Business; Mohamed Dessouky, DiaaEldin Khalil, Ain Shames University

This paper illustrates advanced latch-up verification challenges associated with 2.5D/3D ICs, especially for external and mixed voltage rules. It presents the proposed automated verification flows and demonstrates experimental results. Flows are based on identification of external IOs from the assembly level, without using any layout markers on the die level.

2A.2 Empirical ESD Modeling of Multi-Gate ESD Transistors

Efraim Aharoni, Avi Parvin, TOWERJAZZ

ESD transistors with multiple parallel gate terminals were measured by TLP using worst-case scenario set-up. Empirical ESD Models for ESD transistors with multiple gates, were created. They employ behavioral code and contain the dependency of Vt1 and post-snapback characteristics on the sizes of the multiple gates of the ESD transistor.

Exhibitor Showcase: 1:15 PM-1:25 PM

HPPI GmbH

Session 2B: 1:25 PM-2:15 PM

2B: Device Testing: Testers, Methods and Correlation Issues II

Moderator: Robert Gauthier, GLOBALFOUNDRIES

2B.1 Pitfalls for Transient Analysis with VF-TLP

Theo Smedes, Sander Sluiter, Paul Cappon, NXP Semiconductors; Mart Coenen, EMCMCC

Analyzing transient ESD device behavior with TLP equipment requires more attention for implementation and measurement details than the classical quasi-static TLP approach. Minimizing hardware parasitics reduces the de-embedding effort and optimizes the quality of the voltage and current measurements. We explore different methods and hardware options and highlight potential pitfalls.

2B.2 Transmission Line Pulse (TLP) Statistical Characterization Approach

L. Merlo, L. Di Biccari, A. Castelnovo, L. Cerati, A. Boroni, A. Martino, A. Andreini, STMicroelectronics

In this work a methodology to properly define design guidelines by means of TLP statistical data analysis is presented, avoiding overdesign and failures for products. Using fully automated TLP set-up, a large amount of characterization data is collected. This information can be used to drive an advanced optimization of ESD protections.

Exhibitor Showcase 3:00 PM-3:10 PM

ESDA Standards (Live-Stream)

Session 3A: 3:10 PM-4:00 PM

3A: Numerical Modeling and Electronic Design Automation II

Moderator: Gernot Langguth, Infineon Technologies

3A.1 Novel ESD Compact Modeling Methodology Using Machine Learning Techniques

Wei Liang, Xuejiao Yang, Alain Loiseau, Souvick Mitra, Robert Gauthier Jr., GLOBALFOUNDRIES

Novel ESD compact modeling methodology using machine learning techniques is proposed in this paper. Comparisons between conventional, novel fitting methodology and among different machine learning models are discussed. The advantages of this novel methodology are introduced and methods to further improve the model accuracy are also discussed.

3A.2 Efficient ESD Generator Modeling Using Reinforcement Learning

Akhilesh Kumar, En-Cih Yang, Ming-Chih Shih, Ying-Shiun Li, Wen-Tze Chuang, Norman Chang, ANSYS, Inc.

This paper describes Reinforcement Learning (RL) based technique for estimating the parameters of ESD generators modeled using circuit templates, given the current discharge waveform. The proposed algorithms can be applied to any circuit template to tune the circuit parameters for the desired application or optimization efficiently with minimum prior knowledge.

Exhbitor Showcase 3:00 PM-3:10 PM

Barth Electronics, Inc.

Session 3B: 3:10 PM-4:25 PM

3B: Device Testing: Testers, Methods and Correlation Issues III

Moderator: Robert Gauthier, GLOBALFOUNDRIES

3B.1 An Experimentally Verified Methodology for Calculating Coaxial Cable Loss Effects on CDM Waveforms

Peyman Ensaf, Intel Corp.; Timothy J. Maloney, Center for Analytical Insights

Experimental verification of a turnkey methodology for assessing the precise impact of cable loss on specified CDM pulses in the time domain is presented. Experiments verify the impact of cable losses, mainly skin depth, by convolving CDM waveforms with impulse responses for cables of various lengths.

3B.2 Ultrafast RVS as an Efficient Method to Measure Oxide Breakdown in the EOS and ESD Time Domain

Simon Van Beek, Marko Simicic, Jacopo Franco, Shih-Hung Chen, Dimitri Linten, imec,

Conventional methods to measure breakdown in the ESD time domain, make use of time consuming TLP measurements with a fixed pulse amplitude. With ultrafast RVS, similar equivalent lifetime of oxide breakdown is obtained, using only a pulse generator and oscilloscope and without the need of predefined stress conditions like in CVS.

3B.3 Cable Discharge Event Simulation and Measurement Methods

Pasi Tamminen, EDR&Medeso

Cable discharge events can damage sensitive electronics and these risks can be estimated with measurement and simulation methods. Here measured cable discharges are compared to 3D simulation and vector network analyzer S-parameter based discharge current calculations. This study shows that real-world cable discharge events can be estimated based on calculation methods.

MANUFACTURING KEYNOTE

Tuesday, September 15

9:00 a.m. - 9:45 a.m.

ESD Control Program Management for the Factory of Tomorrow

Kevin Duncan, Seagate Technology

Live-Stream

As IC technologies evolve in favor of faster IO speeds and increased package sizes, challenging constraints will be placed on development of on chip ESD protection. Current industry approach uses Human Body Model (HBM) and Charged Device Model (CDM) testing to determine the relative sensitivity of a device to aid the ESD Program Manager in developing and ESD control program plan.

With this information ESD protection strategies and handling risk assessments are conducted and control programs developed. These control programs typically follow general industry guidance and best practices. Few make a conscious and concerted effort to develop a program tailored for their individual needs. Developing this tailored program approach is the next evolutionary step in ESD control program management.

This talk will review current ESD control program management approaches and look at different ways to evaluate ESD threats in your process. Armed with this knowledge we will talk about how ESD control methodologies will change, which controls will require additional focus, and new threats that will need to be considered.

Kevin Duncan currently serves as the Corporate ESD Program Manager for Seagate Technology. In this position he is responsible for controlling factory level ESD in the ultra-sensitive Hard Disc Drive manufacturing process.

Kevin has been a member of the ESD Association since 2000 and is currently the Chairman of the Technical and Administrative Support (TAS) Committee and Vice Chairman of the Standards Committee. He has served as Chairman of Working Group 3 – Ionization and currently as Chairman of WG53, Compliance Verification and serves as a member of many additional Working Groups. He enjoys teaching and has spent many years providing training regarding ESD Control Program Management.

Kevin is a Technical Expert of the United States National Committee, where he represents the United States participating in International Electrotechnical Commission (IEC) Technical Committee 101 – Electrostatics, where he currently serves as Convener of Maintenance Team 9 – Footwear and Flooring and participates in various other Maintenance Teams and Working Groups. He is an ESD Certified Professional Program Manager and an iNARTE Certified ESD Engineer.

Manufacturing I

10:15 a.m. - 11:30 a.m.

(Moderator: Andy Nold, Teradyne)

M.1 Shielding Effectiveness of ESD Protective Packaging

John Werner, Piyush Kashyap, John Kinnear, IBM

There has always been the claim that ESD protective packaging will shield electric fields. While there exist tests to measure the shielding effectiveness of materials, there does not exist any measurement on protective packaging. One approach to measuring field shielding is described in this paper where a noise source is placed inside multiple types of ESD protective packages. The ESD protective packaging with the noise source was then placed in a reverberation chamber where radiated emissions measurements were studied.

M.2 Can Electrostatic Discharge Sensitive Electronic Devices be Damaged by Electrostatic Fields?

Jeremy Smallwood, Electrostatic Solutions Ltd

This paper demonstrates that very high impedance voltage sensitive device such as MOSFETs or MOS capacitors can be damaged due external field changes without making contact with other conductors. A simple electronic model is proposed. A neon bulb is used as proxy for the voltage sensitive device in practical experiments.

M.3 A Thin Film Storage Device to Characterize the CDM Event Distribution of a Process

Matt Lauderdale, Emmanuel Onyegam, Brad Smith, Jane Yater, NXP Semiconductors; Scott Ruth, AMD

TFS Flash technology is incorporated into chips as a mean to detect, measure, and record CDM events that the chip experiences during processing and handling. TLP and CDM results show a VT shift proportional to the discharge. the VT shift can be tuned and is measured by standard test equipment.

Technology Showcase I

1:00 p.m. - 1:30 p.m.

(Moderator: Michelle Lam, IBM)

Flooring Systems from A-Z

Tom Ricciardelli, StaticStop/SelecTech, Inc.

The presentation will cover:
What constitutes a complete ESD flooring system to ensure it provides a reliable grounding mechanism for personnel.
The various types of ESD flooring systems available.
Unique Interlocking ESD flooring systems that overcome many of the pitfalls associated with conventional ESD flooring systems.

Technology Showcase II

1:30 p.m. - 2:00 p.m.

(Moderator: Michelle Lam, IBM)

New Steady-state DC Bar Ionizer Technology Introduction

Joshua Yoo, Core Insight, Inc.

Most bar ionizers are constructed by conventional AC, pulsed AC, or high frequency AC ionizers and they have swing voltage of more than 500 V p-p. Recently, a developed and patented innovative design bipolar nozzle could use steady-state DC bar ionizer which eliminates swing voltage. Conventional DC bar has 300 - 400 V offset voltage at each end of the bar and cannot be used for ESD control in the EPA. Swing voltage from an AC bar ionizer could lead to ESD damage on a device such as ultrasensitive IO pins or class 0 device handling automated process for ESD control applications.

Panel Session

2:25 p.m. - 3:25 p.m.

Then, Now and Future of ESD control

Moderator: Marcus Koh, Everfeed Technology Pte Ltd

Panelists: Christopher Almeras, Raytheon; Bernard Chin, Qorvo; Rita Fung, Cisco; Matt Jane, Tesla; Dale Parkin Seagate Technology

A panel of ESD control experts in electronics, automobile, space and aviation system will come together to discuss their perspectives in current and future state of ESD control in manufacturing, sharing best practices and lessons learned in implementing ESD control program, training plan, compliance verification and qualification,etc. Bring your questions and pain point, join us in this lively interactive forum.

Year-In-Review: Electrical Overstress in Manufacturing and Test

Vladimir Kraz, OnFILTER, Inc.

Wednesday 8:00 AM - 8:40 AM

Instructor Live-Stream

Electrical overstress (EOS), sometimes referred to as EIPD (electrically-induced physical damage), is a number one cause of damage to devices. This presentation will discuss the recent publication of the technical report (TR) ESD TR23-01-20 - "Identifying, Measuring, and Mitigation of Electrical Overstress Sources". The TR's purpose is to present to a wide constituency of EOS/ESD Association members and adjacent industries a body of knowledge encompassing practical aspects of dealing with EOS in manufacturing environment. The TR describes the basic difference between ESD and EOS and outlines EOS effect on equipment. It further provides explanation on the types and causes of EOS in manufacturing. An important portion of the TR is dedicated to EOS measurements and mitigation.

Exhbitor Showcase 9:10 AM-9:20AM

Simco-Ion

Session 4A: 9:20 AM-10:10 AM

4A: EOS/ESD Failure Analysis, Troubleshooting, and Case Studies II

Moderator: Alain Loiseau, GLOBALFOUNDRIES

4A.1 Balancing the Tradeoff Between Performance and Mis-Trigger Immunity in Active Feedback-Based High-Voltage Tolerant Power Clamps

Alex Ayling, Elyse Rosenbaum, University of Illinois at Urbana-Champaign; Javier Salcedo, Srivatsan Parthasarathy, Jean-Jacques Hajjar, Analog Devices, Inc.

An active feedback based high-voltage tolerant power clamp with optimally biased positive and negative feedback was designed to bypass the trade-off between ESD performance and mis-trigger immunity. The design was fabricated in 28-nm CMOS, and characterization results show a 70% improvement in failure current while maintaining mis-trigger immunity.

4A.2 Open-Relay Tester Capacitance Parasitic Induced Product Level HBM Failure with ESD Proven IP in FinFET Technology

Tao-Yi Hung, Li-Wei Chu, Paul Lee, Wei-Chao Chang, Ming-Fu Tsai, Wun-Jie Lin, Jam-Wem Lee, Chris Wang, Kuo-Ji Chen, Taiwan Semiconductor Manufacturing Company

A packaged-level HBM failure case of an isolated-VSS I/O is presented. Propose the unbalanced p-well substrate potential gap induce unexpected HBM failures in high pin-count relay-based machine. The suspect failure models, simulations and silicon verifications are performed and discussed in this paper.

EMC Special Session Welcome 9:10 AM-9:20AM

9:20 AM-11:25 AM

EMC (Invited) I

Moderator: Alan Righter, Analog Devices

E1.1 (Invited) ESD Generator Tip Current Reconstruction Using a Current Probe Measurement at the Ground Strap

Shubhankar Marathe, Javad Meiguni, Keyu Zhou, David Pommerenke, Missouri University of Science and Technology; Mike Hertz, Teledyne LeCroy

Monitoring ESD generator discharge current during IEC 61000-4-2 testing helps to better understand product failures. By acquiring the discharge waveform using an oscilloscope, this enables the operator to both document the current waveform which resulted in product failure, and to identify the presence of secondary ESD event within the product. Placing a current probe such as an F-65 current clamp at the tip of the ESD generator may change the discharge current waveform shape due to probe loading. In addition, the inclusion of an extra cable and current clamp increases physical weight at the tip of the ESD generator and reduces operator convenience during testing. In order to overcome the probe loading effect, a non-intrusive measurement method of positioning the F-65 current clamp at the ground strap of the ESD generator is proposed. The disadvantage of this configuration is that the captured waveform does not include the initial high-frequency peak current directly. Since the waveform measured at the ground strap does not contain high frequency components, mathematical processing is needed to reconstruct the initial nanosecond high-frequency current waveform which may lead to product failure. The goal of this work is to reconstruct the high-frequency discharge tip current waveform by measuring the current on the ground strap and applying deconvolution. The deconvolution method is first validated using circuit simulation. In addition, measurements are performed with different ESD generators to determine the effectiveness of the reconstruction algorithm.

E1.2 (Invited) ESD Analysis and Evaluation of Typical Spacecraft Survival Suit Umbilical Tubing

Robert C. Scully, Jet Propulsion Laboratory

This document presents an assessment of the potential for occurrence of triboelectrification effects resulting from gas and fluid flow through umbilical tubing attached to a typical spacecraft survival suit. The assessment demonstrates that gas and fluid flow through the umbilicals poses no threat to crew safety over expected operational time periods up to 150 hours.

Exhibitor Showcase 10:35 AM-10:45 AM

ESDA Advanced Topics(Live-Stream)

Session 5A: 10:45 AM-11:35 AM

5A: Numerical Modeling and Electronic Design Automation III

Moderator: Michael Khazhinsky, Silicon Labs

5A.1 A Physical Finite Difference Model of a Forward Biased Diode Using SPICE

Steffen Holland, Nexperia Germany GmbH

A physical model for a forward biased diode with a lowly doped region is presented. The diffusion and transport equation is solved by the finite difference method in a spice simulator. A good agreement of the transient voltage for different VF-TLP rise times is achieved.

5A.2 3D TCAD Studies of Snapback Driven Failure in Punchthrough TVS Diodes Under System Level ESD Stress Conditions

Jhnanesh Somayaji B, Monishmurali M, Ajay Singh, N Kranthi K, Mayank Shrivastava, Indian Institute of Science

This paper explains the ESD failure dynamics of TVS diode reported for the first time. The failure is universal to TVS diode structure designed as ESD protecting element. This work gives the detailed physical insights into failure mechanisms using 2D & 3D TCAD simulations. Failure at very low currents due to non-uniform bipolar turn on, for longer pulse duration is explained. 2D simulation shows the non -uniformity due to current crowding while 3D simulation supports the failure dependency with thermally driven filamentation failure).

EMC (Invited) II

Moderator: Alan Righter, Analog Devices

E1.3 (Invited) Investigation of Electrostatic Discharge-Induced Soft-Failure Using 3D Robotic Scanning

Omid Hoseini Izadi, David Pommerenke, Missouri University of Science and Technology; Hideki Shumiya, Kenji Araki, Sony GM&O Corp

A robotic ESD scanning system is presented for scanning complex 3D objects. It provides pseudo-2D plots that illustrate the sensitive locations of the device under test on a relative scale. Using this system, we could determine the susceptible regions of the device. It was observed that disturbing different sensitive regions lead to different soft-failure types. Determining the sensitive locations of a complex-shaped DUT helps to identify the disturbed circuitry and verify the effect of countermeasures in a repeatable way.

E1.4 (Invited) Experimental Validation of an Integrated Circuit Transient Electromagnetic Event Sensor

Shubhankar Marathe, Abhishek Patnaik, Kaustav Ghosh, David Pommerenke, Daryl G. Beetner, Missouri University of Science and Technology; Jingook Kim, Ulsan National Institute of Science and Technology

Determining the components or coupling path responsible for soft failures during transient testing is challenging, In part because components are hidden deep within the product and because measuring internal voltages or currents during a transient test may not be practical. Adding cables to the system to make voltage or current measurements may be difficult and may alter the test results. To overcome this problem, a compact sensor has been designed to measure the peak over- or under-voltage on a trace or pin during a transient electromagnetic event. The sensor was designed to wirelessly transmit the peak level of the event to a receiver outside the device under test using frequency-modulated electric and magnetic fields, so that no cabling or other changes to the system are needed. A proof-of-concept of the sensor has been implemented in an integrated circuit (IC) using 180 nm technology which can measure the peak level of a negative transient event. The sensor operation was validated by direct injection to the sensor from a transmission line pulser. The sensor was also used to detect the peak voltage on a USB cable during a transient event on the cable-connected system. Tests showed that the sensor can successfully detect and transmit the peak level of the event, and that the oscillation frequency (and thus the level) could be easily detected by a near-field probe placed outside the enclosure of the device under test.

Exhibitor Showcase 1:40 PM-1:50 PM

DayStrong Rubber Products, LLC

Session 6A: 1:50 PM-3:40 PM

6A: Published Posters

Moderator: Gianluca Boselli, Texas Instruments

6A.1 Physics of Dynamic Current Filament Spreading in Silicon Controlled Rectifiers Under ESD Stress

Om kesharwani, Kranthi N.K, Mayank Shrivastava, Indian Institute of Science

By using 3D TCAD simulations, the physics of filament formation and subsequent spreading along device width in Silicon controlled rectifiers (SCR) is studied. A detail transient study of different physical parameters probed with respect to time and device width, and their impact into current filament spreading in SCR is presented.

6A.2 Study of Inter-Power Domain Failures During a CDM Event

Chloé Troussier, STMicroelectronics, University Grenople Alpes; Johan Bourgeat, Jean Jimenez, Blaise Jacquier, STMicroelectronics; Emmanuel Simeu, Jean-Daniel Arnould, University Grenoble Alpes

This work introduces a study of inter power domain failures during a CDM event. A comprehensive simulation is developed using substrate and package modeling as well as VF-TLP characterization of CDM protections and oxide breakdown study in the CDM timescale. Simulation results are confronted with silicon testing.

6A.3 Race Conditions Among Protection Devices for a High Speed I/O Interface

Jianchi Zhou, Javad Meiguni, Yang Xu, Giorgi Maghlakelidze, Daryl Beetner, Missouri University of Science and Technology; Sergej Bub, Steffen Holland, Guido Notermans, Nexperia Germany; David Pommerenke, Graz University of Technology

Test conditions strongly affect the ESD rise time seen on-PCB. Possible race conditions between external and on-die ESD protection were studied using measurement-based models of the transient response and on-board passives. Results show the interplay of rise time and protection turn-on can prevent the external TVS from responding in time.

6A.4 Understanding ESD Characteristics of GGNMOS in Bulk FinFET Technology

Wen-Chieh Chen, Katholieke Univeriteit Leuven, imec; Shih-Hung Chen, Geert Hellings, Thomas Chiarella, Jie Chen, Sujith Subramanian, Yong Kong Siew, Dimitri Linten, imec; Guido Groeseneken, Katholieke Univeriteit Leuven

Bulk FinFET is a main technology option for sub-20nm nodes. Device geometry and process options in advanced FinFET show effects on ESD performance. In addition, the impact of layout parameters of gate length and drain ballast distance on the grounded-gate NMOSFET (GGNMOS) are investigated and demonstrated by 3D TCAD simulation.

6A.5 Slow Turn Off Optimization of CMOS ESD NAND Clamp Design to Eliminate Fly-Back Damage During Unlatch

Divya Acharya, Nathaniel Peachey, Stephen Franck, Emilio Ruiz-Linares, Jian Liu, Qorvo

The unlatching mechanism of the ESD NAND clamp can cause it to turn off sharply, resulting in fly-back and damaging oscillations. This paper presents simulations and hardware measurements that verify a simple feedback circuit addition to the clamp that can be effectively used to control the turn off and prevent failures.

6A.6 ESD Characterization and Modeling of Cascoded, Silicided FETs in a 22nm FDSOI Technology

Alain Loiseau, Xuejiao Yang, Anindya Nath, Souvick Mitra, John Forguites, Mike Fortney, GLOBALFOUNDRIES

Cascoded FETs in FDSOI under ESD stress is characterized and modeled for the first time. A novel characterization structure is developed to regulate channel modulation precisely. ESD failure voltage (Vt2) modulation of such system is explained and excellent model to hardware correlation is demonstrated.

6A.7 (Invited) Design Optimization of MV-NMOS for ESD Self-protection in 28nm CMOS technology

Kyongjun Hwang, Sagarpremnath Karalkar, Vishal Ganesan, Sevashanmugam Marimuthu, Alban Zaka, Tom Herrmann, Bhoopendra Singh, Robert Gauthier, Jr., GLOBALFOUNDRIES

An effective design for self-protection MV-nMOS with modification of drain junction in 28nm high voltage CMOS technology is presented. Modification of N+ drain with LDD spacer shows improved ESD performance with identical Idsat, HCI level, by reducing the electric field at poly/drain overlap region and, spreading ESD current path between drain and source. TLP, DC-IV and HCI characterization techniques were used to verify the structure and TCAD was utilized to examine the failure root cause.

6A.8 (Invited) Triggering Optimization on NAND ESD Clamp and Its ESD Protection IO Scheme for CMOS Designs

Jian Liu, Divya Acharya, Nathaniel Peachey, Qorvo, Inc.

This paper presents the improvements on the NAND ESD clamp and the associated IO scheme to address the challenges in specific circuit applications, such as mis-triggering
and parallel clamp triggering. Simulation and measurement results were compared and analyzed.

Poster Session (Author's Corner for Published Posters)

EMC Short Tutorials: 1:20 PM-5:00 PM

Coordinator: Ross Carlton, ETS-Lindgren

ESD Testing in Accordance with IEC 61000-4-2

1:20 p.m. - 2:00 p.m. (Instructor On-Site)
Ross Carlton, ETS-Lindgren

IEC 61000-4-2 is the most used System-Level ESD test method standard since it is used for most consumer, commercial, and industrial products. This presentation will discuss the specified ESD waveform, test setup, test methodology, and reporting requirements. The application of this method for testing PCBs, IC package pins, and other unusual applications will be discussed.

System Level ESD Design Considerations and a Means of Evaluation

2:00 p.m. - 2:40 p.m. (Instructor On-Site)
Colin Brench

This workshop will discuss the impact of ESD events on the behavior of high data rate interfaces and how such events impact not only hardware design but also the firmware and software. Simple pass/fail tests give little indication of true performance, but when done under slightly different operating conditions, a deeper understanding is possible. Details of the test methodology are described, and will include an example of the process and results from a particular case.

Lessons-Learned in System-Level ESD Testing

2:40 p.m. - 3:20 p.m. (Instructor Live-Stream)
Derek Walton, SSC Labs, Harry Reid Engineering Laboratory

The methodology specified for EMC testing is complex and contains many uncertainties that can impact the test results. This presentation will address these complexities and the lessons learned from years of testing a wide variety of products. Strategies for managing these complexities will be discussed.

System-Level ESD Failure Mechanisms and Mitigation Techniques

3:40 p.m. - 4:20 p.m. (Instructor Live-Stream)
David Pommerenke, Graz University of Technology

System-level ESD can lead to soft-errors (e.g., bit-errors, wrong resets etc.) and even damage. This presentation offers guidance on finding the root cause of upsets frequently observed in immunity testing (e.g., ESD, EFT) and describes various measurement techniques. Further, it is shown how measurements, revealing local sensitivities, can be used for the characterization and optimization of circuits and software.

EMI Measurements in Manufacturing Environment

4:20 p.m. - 5:00 p.m. (Instructor Live-Stream)
Vladimir Kraz, OnFILTER, Inc.

This short tutorial provides practical guidance on measuring and quantifying relevant EOS-causing EMI signals in a semiconductor or electronic manufacturing environment. An attendee will be able to understand the basic methodology, required tools, and the difference between correct and incorrect approaches. Measurements of EMI voltage and current will be covered.

Manufacturing II

8:00 a.m. - 8:50 a.m.

(Moderator: Robert Hank Mead, BAE Systems)

M.4 Understanding Electrostatic Field Meter Field and Voltage Measurements from Conductors and Insulators

Jeremy Smallwood, Electrostatic Solutions Ltd; Nicolas G. Green, University of Southampton; Kelly Robinson, Electrostatic Answers LLC

Evaluation of electrostatic risks in ESD control relies on electrostatic field and voltage measurements on conductors and insulators. A simple capacitor model helps clarify measurements made using electrostatic field meters on conductors at constant voltage, isolated conductors with constant charge and uniformly charged insulating surfaces using electrostatic field meter instruments.

M.5 Statistical Characterization of ESD Through Solder Paste

Junsoo (Steve) Paek, California Polytechnic University; Rita Fung, Richard Wong, Geronimo Filippini, Jeff Kendo, Allen Zhao, Cisco System Inc.

Few models exist to characterize the electrical properties of un-reflowed solder paste. As such, determining whether ESD could occur through un-reflowed solder paste is difficult. To evaluate the risk of a discharge through un-reflowed solder paste, an automated fixture is used to create and measure field induced discharge.

Technology Showcase III

9:15 a.m. - 9:45 a.m

(Moderator: Michelle Lam, IBM)

Creating Permanent Static-Dissipative and Conductive Protection in Reusable Containers and Dunnage

Samantha Goetz, ORBIS Corporation

For decades, reusable packaging has been considered an economical and sustainable way to store and move parts and components, in various states of assembly, in the supply chain. As tech companies continue to require high-value electronics, the protection of these items in the supply chain is critical. The ability to mold reusable totes and fabricate custom dunnage/ divider sets with permanent static-dissipative properties helps part makers manage their part shipments more confidently. In this session, attendees will learn the benefits of reusable packaging in the supply chain, manufacturing considerations, material factors, the importance of testing and how companies can get started with reusables.

Hands-on demonstrations from the three featured technology showcases:

StaticStop/SelecTech, Inc.

9:45 a.m. - 10:15 a.m. (On-Site)

Workshop: Assessment, Selection, and Qualification of Materials and Equipment Used in the EPA

10:45 a.m. - 12:00 p.m. (On-Site)

Moderator: John Kinnear, IBM

Material qualification is a requirement for ESD control items to meet ANSI/ESD S20.20 requirements. While the standards sets the measurement techniques there are many different ways to implement the process of qualification. Selection of the proper equipment, decisions made, are all up to the process owner. This workshop is to discuss issues, processes and ways to implement qualification processes depending on materials, equipment and environments. This a discussion of any issues or creative ways to conduct qualification and still meet the requirements of ANSI/ESD S20.20.

Year-In-Review: ESD On-chip Design

Christian Russ, Mirko Scholz, Gernot Langguth, Infineon Technologies AG

Thursday 8:00 AM - 8:40 AM

Instructor Live-Stream

Today, on-chip ESD protection design is well established and integrated in the product-level design of integrated circuits (ICs). The designers can rely on established ESD characterization methods like TLP. Electronic Design Automation (EDA) tools support the designer with simulations and during the verification process. But there are several trends that provide challenges to the on-chip protection design. Automotive products are implemented in advanced technologies that have not been developed for these applications. The use of foundry technologies and external IP limits the access to device physics-based simulations and analysis. Also, system-level requirements like Electrical Overstress and IEC61000-4-2 often need to be taken into account already during on-chip design. In this review we will use recently published work in conferences and peer-reviewed journals to have a look on how some of these challenges are solved. We will also present an overview on the latest advances in the relevant ESDA working groups.

Session 8A: 9:05 AM-12:25 PM

8A: System Level EOS/ESD/EMC

Moderator: Pasi Tamminen, EDR&Medeso

INV RCJ- Clarification and Countermeasures of Electrostatic Discharge (ESD) in High-Pressure Spray Cleaning During Flat Panel Display Manufacturing

Yoshiyuki Seike, Yasuaki Fukuoka, Tatsuo Mori, Aichi Institute of Technology; Taishi Segawa, Yoshinori Kobayashi, Keiji Miyachi, Asahi Sunac Corporation

High-pressure spray cleaning during the manufacture of flat panel displays has the problem of electrostatic discharge (ESD). In this study, the factors of static electricity generated from high-pressure spray were clarified. Further, a counter voltage was applied to the nozzle, and the water was heated to reduce the charges.

INV German Forum- Measuring the Body Voltage while performing the Walking Test

Magdalena Hilkersberger, Reinhold Gärtner, Infineon Technologies AG; Wolfgang Stadler, Josef Niemesheim, Intel Deutschland GmbH; Jürgen Speicher, Wolfgang Warmbier GmbH & Co. KG

In this paper the suitability of different measuring devices for the walking test according to ANSI/ESD STM 97.2 will be investigated and evaluated. The influence of the signal frequency and the cable between hand-held electrode and recording device will also be assessed. Finally, the need for a more specific definition of the test setup in international standards will be discussed.

8A.1 Insights into the System Level IEC ESD Failure in High Voltage DeNMOS-SCR for Automotive Applications

Nagothu Karmel Kranthi, Mayank Shrivastava, Indian Institute of Science; James Di Sarro, Rajkumar Sankaralingam, Gianluca Boselli, Texas Instruments, Inc.

Unique failure mechanism for IEC stress through a common-mode choke is investigated. Minor variations in the current waveform shape for specific IEC stress levels are found to cause device failure. 3D TCAD simulations are used to understand the device behavior and failure under the peculiar two-pulse shaped IEC current waveform.

8A.2 Electromagnetic Shielding Effectiveness of Conductive Compounds

Toni Viheriäkoski, Cascade Metrology; Jan Järveläinen, Premix Oy; Pasi Tamminen, EDR&Medeso Oy; Jeremy Smallwood, Electrostatic Solutions Ltd.

Electromagnetic and electrostatic discharge shielding effectiveness of conductive compounds were studied with a coaxial electrode. Attenuation of continuous low power signals and high-power transients were measured. Results of the samples with different conductivities were compared, showing that adequate shielding for different applications can be achieved by conductive compounds.

8A.3 Spectral Analysis of IEC Generators for System Level Testing of RF Components

Kathleen Muhonen, Luis Perez, Nathaniel Peachey, Qorvo

Studies over the last decade have brought to the forefront several hurdles to testing components to the IEC 61000-4-2 standard. One hurdle is that the generators produce different results despite being qualified generators. This work analyzes the frequency domain spectra to demonstrate why the IEC generators are not repeatable across equipment for use with frequency sensitive components.

8A.4 Hot Plug-in: Test Method and HV Active Clamps

Vladislav Vashchenko, David Marreiro, Slavica Malobabic, Maxim Integrated Corp.

Hot-plug-in (HPI) compatibility of HV rail-based ESD protection networks is addressed by establishing express wafer level test method followed by upgrading HV active clamps. The clamp level solution is validated experimentally by cross-comparing the novel HPI I-V characteristics and TLP I-V characteristics of the original and improved HPI tolerant clamps

8A.5 A New Current Probe for Measuring Transient Events under Data Traffic

Omid Hoseini Izadi, DongHyun Kim, Missouri University of Science and Technology; David Pommerenke, Graz University of Technology

Using inductive current measurement technique, a new current probe is proposed. The proposed probe allows transient current measurement on Gbps data traces without disturbing the normal operation or transfer rate of the trace under test. The proposed probe layout, circuit model, and frequency response is discussed in detail.

Session 8B: 9:05 AM-12:00 PM

8B: Invited IRPS

Moderator: Gianluca Boselli, Texas Instruments

8B.1 (Invited) How to Achieve Moving Current Filament in High Voltage LDMOS Devices: Physical Insights & Design Guidelines for Self-Protected Concepts

Kranthi Nagothu, Sampath Kumar Boeila, Chirag Garg, Mayank Shrivastava, Indian Institute of Science; Akram Salman, Gianluca Boselli, Texas Instruments

New design approach for improving ESD robustness of High voltage LDMOS devices is presented using 3D TCAD simulations by developing physical insights,engineering approaches for moving filaments. (i) NPN turn-on engineering by using an optimum P-well profile & substrate biasing and (ii) filament width engineering by using optimum drain diffusion length (DL), shows how static filament can be modified to achieve dynamic (moving) nature. This approach resulted in 10× improvement in ESD robustness for self-protecting concepts.

8B.2 (Invited) Over-Voltage Protection on the CC Pin of USB Type-C Interface against Electrical Overstress Events

Chao-Yang Ke, Ming-Dou Ker, National Chiao-Tung University

An over voltage protection (OVP) design on the CC pin of USB type-C IC was proposed. An EOS detection circuit is proposed to turn off the gate of the HVNMOS when EOS stressing on the CC pin, which can mitigate the hot carrier degradation (HCD) of HVNMOS. Silicon chip fabricated in a 0.15-μm BCD technology has been measured to successfully verify the proposed OVP design in device level and circuit level.

8B.3 (Invited) Design Insights to Address Low Current ESD Failure and Power Scalability Issues in High Voltage LDMOS-SCR Devices

Kranthi Nagothu, Sampath Kumar Boeila, Mayank Shrivastava, Indian Institute of Science; Akram Salman, Gianluca Boselli, Texas Instruments

Power-scalability issues for longer pulse duration discharges (PW>100ns) in high voltage LDMOS-SCR devices is evaluated. The severity of the problem with increasing LDMOS voltage classes is highlighted with a need for newer design strategies. A systematic design approach is presented to evaluate the effect of different design parameters on LDMOS filament and SCR turn-on near the snapback region. Finally design guidelines are presented to improve the power scalability without compromising on its ON-state DC characteristics.

8B.4 (Invited) Threshold Voltage Shift in a-Si:H Thin film Transistors under ESD stress Conditions

Rajat Sinha, Prasenjit Bhattacharya, Sanjiv Sambandan, Mayank Shrivastava, Indian Institute of Science

We present physical insights into the instability behavior of hydrogenated amorphous TFTS under ESD stress using real-time current-voltage and capacitance-voltage characterization. A threshold voltage increase under moderate stress and a recovery under high stress is investigated. Impact of gate-bias and device dimension is explored. Physics of bias annealing and an associated device recovery is explored. Finally, we investigate the instability behavior in a-Si:H gated diodes and explore the role of self-heating on their reliability.

8B.5 (Invited) Sub-Nanosecond Reverse Recovery Measurement for ESD Devices

Alex Ayling, Shudong Huang, Elyse Rosenbaum,University of Illinois - Urbana Champaign

A transient, reverse recovery current will flow in a diode that is switched from the on-state to the off-state; the same occurs in bipolar and SCR devices. Proper modeling of reverse recovery is important when simulating ESD events in which the current is bipolar, and a measurement technique is outlined that can be used for sub-nanosecond reverse recovery events. Existing compact model predictions were compared with these measurements and found to be inaccurate.

8B.6 (Invited) Improved Turn-on Uniformity & Failure Current Density by n- & p-Tap Engineering in Fin Based SCRs

Monishmurali M, Milova Paul, Mayank Shrivastava, Indian Institute of Science

Failure threshold in Fin based SCR (FinSCR) is limited by non-uniform current distribution across the anode/cathode fins, attributed to non-uniform turn-on of individual fins. Unique physical insights related to FinSCR turn-on uniformity and position of hot-spot are developed as a function of the placement of n- & p- taps. Unique tap schemes are explored, which offered relaxed self-heating and improved turn-on uniformity. A novel Distributed Tap FinSCR device is proposed, which offers failure threshold scalability.

Session A: 5:10 PM - 6:25 PM

On-Site

A.1 ESD Verification Tools: Are We There Yet?

Stephen Fairbanks, SRF Technologies

In the past 10 years, we have seen a lot of development in the EDA space, bringing to market viable tools to help validate, model and anticipate ESD performance in our IC designs. The main focus is on final run verification flows similar in style to traditional DRC/LVS tools, but specialized for ESD, seeking to be final signoff tools capable of finding, anticipating and catching errors prior to tapeout. Given the phenomenal strides tool developers have made, have we reached a point where end-users trust and use these tools with confidence? Do we find them working, and meeting expectations? Or do we find ourselves often times using them but with false errors, false passes, debugging failures not caught by the tools while waiving failures we understand to not be real? Are these tools now as standard and as comfortable as LVS and DRC? Or are we finding ourselves fighting them and struggling or dreading their use and effort in our projects? This all begs the question, “Are we there yet?”

A.2 Finding the Step Where ESD Failure Occurs in Manufacturing - Process Assessment Meets Event Detection

Christopher Almeras, Raytheon

When ESD concerns or issues arise in the factory, what steps should be taken to drive down to the root cause? This workshop will involve a discussion of the investigation techniques that can help efficiently find the smoking gun. Topics covered will include common threats, assessments, questions to ask, measurements and re-creation. Scenarios will also be used to aid the understanding of applying the techniques.

Session B: 5:25 PM - 6:40 PM

On-Site

B.1 ESD Education in the Field

Jay Skolnik, Skolnik Technical Training; Dana Beatty, XFabion, LLC

Varied company types & sizes face diverse training predicaments, from the startup & small sizes to the large corporations covering many worldwide locations. This comprises the various target-audiences, such as design engineering laboratories, contract manufacturing environments, and others. This workshop will include dialogue from a panel of experts to deliberate the most effective approaches and will address the fundamentals of training employees at their company site. We will discuss the generally accepted techniques for training such as live instruction, training videos, interactive computer-based programs, symposium, etc. One of the challenges of training is the **cost.** We will address these challenges as well as the **value** of training with return-on-investment realization and methods to measure it.

B.2 EMC Expert Panel

Colin Brench; Ross Carlton, ETS-Lindgren; Vladimir Kraz, OnFILTER; David Pommerenke, Graz University of Technology; Robert Scully; Derek Walton, SSC Labs, Harry Reid Engineering Laboratory

The ESD Ask the Experts panel provides an excellent opportunity to have your hard-to-answer questions answered by true, knowledgeable experts in the field. This year's panel includes experts from industry, academia, consultants and EMC labs offering their unique perspectives on the latest ESD topics.

Virtual Exhibit Hall

Virtual Exhibit Hours

Monday, September 14
6:00 p.m. - 9:00 p.m.

Tuesday, September 15
9:30 a.m. - 5:30 p.m.

Wednesday, September 16
8:30 a.m. - 1:30 p.m.

Thursday, September 17
10:00 a.m. - 2:00 p.m.

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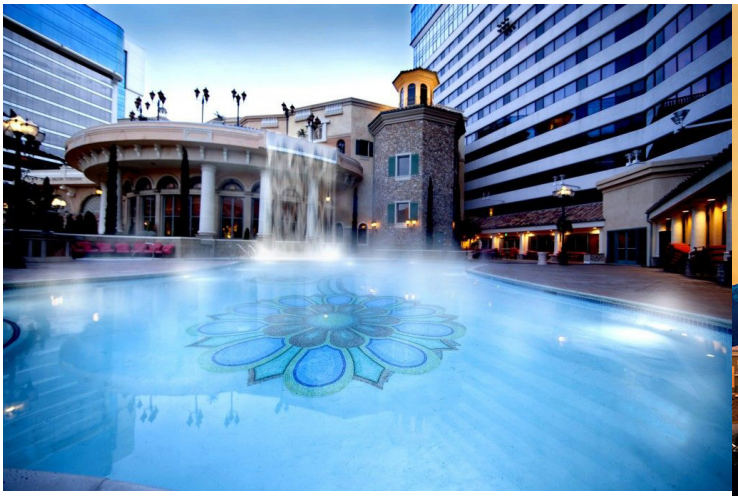

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- **Call in information – 1-800-282-2444 (reference group code: AESDA20)**
- **Book reservations by 8/26/2020 (Please book early as a limited number of hotel rooms are available at the group rate)**
- **Rate – •**
  Sunday-Thursday will now be $65+tax per night (resort fee waived)
  Friday-Saturday will remain at the group rate of $129+tax (resort fee waived)
  Tuscany Tower Rates adjusted to…
  Sunday-Thursday will now be $85+tax per night (resort fee waived)
  Friday and Saturday will remain at the group rate of $149+tax (resort fee waived)

Note: The Resort Fee is included in the rate and includes the following:
• **Resort fee includes high-speed internet access throughout the hotel (including hotel rooms, public space, meeting space, etc.), in-room coffee makers, use of the health club, pool, valet, access to the parking garage and surface parking, concierge, local and #800 phone calls, and shuttle service to and from the airport.**

Note: Complimentary internet access in meeting rooms (only for guests staying at The Peppermill Resort Hotel).

UNAUTHORIZED HOUSING

Housing block “pirates” now routinely “poach” event attendees and exhibitors!
Pirating companies gather group’s contact information from published or online directories. They call attendees leaving the impression that they are an “official” housing representative. They will also frequently cite an imminent sell-out of the block while urging you to secure housing immediately. Another tactic is to offer a room rate that is significantly less than the official rate. Offered rooms may be substandard or at other properties. Please do not respond to these solicitations or book your rooms with any housing organizations that “claim” to represent EOS/ESD Association, Inc. Booking via the hotel link or calling the number we provided are the only safe and reliable methods for booking your hotel reservations.

Reservations When reserving your room, in all instances, identify yourself as a participant of the EOS/ESD Symposium.

Cancellation of reservation must be made at least seven days prior to arrival date or you will be charged one nights room/tax.

Registration - page 1

Register Online!
http://www.cvent.com/d/6nqqp6

On-Site Tutorials

Check each session attending, one session per time slot.

SUNDAY, SEPTEMBER 13

- ☐ FC100: 8:30 a.m. - 4:30 p.m. ESD Basics for the Program Manager (PrM)
- ☐ DD150: 8:30 a.m. - 12:00 p.m. Introduction to RF ESD Design
- ☐ DD300: 1:00 p.m. - 4:30 p.m. Circuit-Level Modeling and Simulation of On-Chip Protection (DD)

MONDAY, SEPTEMBER 14

- ☐ FC101: 8:30 a.m. - 4:30 p.m. How To's of In-Plant ESD Auditing and Evaluation Measurements (PrM)
- ☐ DD340: 8:30 a.m. - 12:00 p.m. Integrated ESD Device and Board Level Design
- ☐ DD214: 1:00 p.m. - 4:30 p.m. Latchup Physics and Prevention **NEW**

THURSDAY, SEPTEMBER 17

- ☐ FC391: 8:30 a.m. - 12:00 p.m. Basics of ESD Process Assessment
- ☐ DD/FC240: 8:30 a.m. - 12:00 p.m. System Level ESD/EMI: Principles, Design Troubleshooting, & Demonstrations
- ☐ FC121: 1:00 p.m. - 4:30 p.m. Grounding – Variations, Concepts, Nuisances, Equipment & Troubleshooting
- ☐ DD/FC130: 1:00 p.m. - 4:30 p.m. System Level ESD/EMI: Testing to IEC and Other Standards (DD)

On-Demand Tutorials

ONE ON-DEMAND TUTORIAL = ONE HALF-DAY

- ☐ DD200: Charged Device Model Phenomena, Design, and Modeling (DD)
- ☐ DD311: Impact of Technology Scaling on Components High Current Phenomena and Implications for Robust ESD Design
- ☐ DD231: ESD System Level: Physics, Testing, Debugging of Soft and Hard Failures
- ☐ DD100: ESD Circuits
- ☐ DD240: ESD Device Qualification Testing
- ☐ DD208. ESD Parameters for the Foundry, IC Designer and IP/EDA Vendor **NEW**
- ☐ FC166 ESD QMS Best Practices Strategy Including Class 0 and Costly Controversial ESD Myths
- ☐ DD220: Transmission Line Pulse (TLP) Basics and Applications (DD)

Student Fees

The EOS/ESD Association, Inc. offers a fifty percent discount for full-time students. Proof of enrollment required. Student fees apply only to on-site symposium or tutorial registration and do not apply to bundled fees, Live Stream, or On-Demand.

Fees

☐ **Symposium $600 *Limited to the first 50 attendees**
(Includes Symposium, Manufacturing, and IoT technical sessions, workshops, and exhibits)
Bonus: Includes 30-day access to Symposium On-Demand access (excludes tutorials)

☐ **Tutorials $510**
(Sunday, Monday, OR Thursday (Full Day))
Mix & match on-site, live stream, and on-demand tutorials.
NOTE: Attend select tutorials on-site or via live stream. Instructors of select tutorials are delivering tutorials on-site or via live broadcast. On-demand tutorials are prerecorded and viewed at your convenience.

☐ **Bundled Fees $1,765**
On-site Symposium plus Sunday, Monday, and Thursday full tutorial days; . Mix & match on-site, live stream, and on-demand tutorials.
NOTE: Attend select tutorials on-site or via live stream. Instructors of select tutorials are delivering tutorials on-site or via live broadcast. On-demand tutorials are prerecorded and viewed at your convenience.
Bonus: Includes 30-day access to Symposium On-Demand (excludes tutorials)

Virtual Registration

☐ **Symposium Live Stream $300**
(Includes three parallel track Zoom links for Symposium, Manufacturing, IoT technical sessions, and complimentary access to virtual exhibits)
Bonus: Includes 30-day access to Symposium On-Demand (excludes tutorials and IoT on-demand)

☐ **IoT Live Stream $150**
(Includes Zoom link for IoT technical program, and complimentary access to virtual exhibits)
Bonus: Includes 30-day access to IoT On-Demand

☐ **Symposium On-Demand only $250**
30-day access to full recording of Symposium and Manufacturing technical program, and complimentary access to virtual exhibits (excludes tutorials and IoT on-demand)

☐ **IoT On-Demand only $90**
30-day access to full recording of IoT technical program, and complimentary access to virtual exhibits

Live Stream is in PDT (GMT-7) timezone.

How did you learn about this event? _____

☐ Under the Americans With Disabilities Act, I require auxiliary aids or services.
☐ First Time Attending

*On-Demand is available two weeks after the event. Access is for 30 days.

Cancellation & refund requests will be honored if received in writing no later than July 13, 2020, and are subject to a $50 fee. Any other approved dispositions will also be assessed a $50 fee.