

News bits

Tee it up for charity

The ESD Association will sponsor a charity golf tournament on Saturday afternoon, September 8 at Langdon Farms Golf Club, Aurora, OR. The tournament is held in honor of David F. Barber, Sr., an avid golfer and one of the founders of the Symposium. Proceeds from the scramble event will be donated to two Portland charities: the Portland Ronald McDonald Houses and Doernbecher Children's Hospital. Advance reservations are required. Contact ESD Association headquarters or visit the ESDA web site, www.esda.org, for additional information.

FDA recognizes S20.20

The US Food and Drug Administration has given full recognition to ANSI/ESD S20.20 for use in conjunction with the manufacture, processing, assembly, installation, packaging, labeling, service, testing, inspection and handling of electrical and electronic parts, assemblies and equipment incorporated into medical devices.

In this issue

Symposium	1
From the Threshold chair	2
Calendar of events	3
Standards site license	3
Kay Adams honored	3
Symposium highlights	4-11
Standards update	12
CDM survey	13
Office remodeling	13
Letters to the editor	14



2001 EOS/ESD Symposium

Comprehensive...concentrated... customizable...cost-effective

The 23rd annual EOS/ESD Symposium packages research, technology, education, and peer networking into the premier international ESD event scheduled September 9-13 at the Oregon Convention Center, Portland, Oregon.

Comprehensive

Tutorials, workshops, and technical papers cover the latest information, research, and technology in electrostatic discharge and electrical overstress. With topics ranging from the basics of ESD and on-chip protection to the newest developments in the emerging fields of RF ESD design and transmission line pulsing, the Symposium offers something for everyone. And, this year's keynote presentation by Tak H. Ning of IBM's Thomas J. Watson Research Center takes attendees from current technologies to looking at new trends in the new millennium.

Concentrated

Sixty-three technical papers presenting the world's leading research, 22 tutorials

from basic to advanced, 8 workshops for peer interchange of ideas and information, and more than 100 exhibits are packed into five full days of activity. And, it's all in one location.

Customizable

Organized and programmed in four technical tracks, attendees will be able to customize their Symposium experience along specific areas of interest: *Design and Device Technology, Factory Issues and Materials, System Level ESD, and Magnetic Recording.*

Cost-effective

With so much ESD education and technology concentrated in one location in a single time period, the Symposium is a cost-effective way to focus on new developments or to gain basic background on ESD. This year's fee structure has been revised to provide additional savings for attendees who participate in the entire five-day program.

In addition, individuals interested in the ESDC certification program will be able to take the certification exams on Friday, September 14. Special tutorials during the week will help applicants prepare for the examinations.

Symposium highlights can be found elsewhere in this issue of *Threshold*. The detailed program is available on the Association's web site, www.esda.org.

The Symposium is sponsored by the ESD Association in cooperation with the IEEE. It is technically co-sponsored by the Electron Devices Society. The general chair is Mark A. Kelly, Delphi Delco Electronics Systems. The vice general chair is Steven H. Voldman, IBM Microelectronics. The technical program chair is Joseph Bernier, Intersil Corporation.

More Symposium

Schedule	4
Registration	4
Technical tracks	5
Technical sessions ...	6
Exhibits	6
Workshops	7
Portland	8
Tutorials	9
Keynote	11

Visit the ESDA web site at
www.esda.org

Device testing needs your response to a technical survey

For the last two years, the device testing standards working group has discussed going beyond the confines of the working group members for input on a number of issues related to device level testing. The two working groups needing the information are the socketed device model (SDM) and the machine model (MM) groups.



Leo G. Henry

There is no existing standard document for SDM because of major waveform correlation issues between those from the SDM simulators and those from the charged device model (CDM) simulators. There are other issues that can be found in several documents prepared by the SDM working group: one

presented at the 1999 EOS/ESD Symposium and later issued as an ESDA Technical report; and one scheduled for publication in an upcoming issue of *Compliance Engineering*.

The SDM 5.3.2 working group now wants to obtain direct input from users of these CDM simulators. Several questions have been developed that cover a sufficiently wide area that will allow the working group to "move on" to address the needs of the user. The working group has looked at several methods for distributing the questionnaire including the ESDA web site, direct mail to ESDA members and the industry, and the EOS/ESD Symposium.

The working group hopes that most of

you will read and respond to the survey so that we have enough data by the September 2001 standards meeting series. This input is critically important to the working group's preparation of a standard practice document by 2002.

Please check your ESDA web site or look for the survey in your mailbox.

I did not cover the issues associated with the machine model working group, but I will do so in the next issue. The group also plans to do a survey, but it will not be ready until later in the year.

We look forward to hearing from you when the survey is sent out. Our expectation is a very high return from the members. See page 13 for more information on the SDM survey.

Thanks in advance. Until next issue, be happy.

Leo G

Threshold

THRESHOLD™ is published six times a year for the members of the ESD Association. The association is a not-for-profit corporation. It strives for the advancement of theory and practice of electrical overstress avoidance and of allied arts and sciences and the maintenance of a high professional standing among its members and others.

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Threshold™ Publication Schedule

Issue	Deadlines
September/October	Aug. 1
November/December	Oct. 1
January/February	Dec. 1
March/April	Feb. 1
May/June	April 1
July/August	June 1



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Calendar of events

July 2001

ESD Northwest Chapter Meeting and Bar-B-Que: July 11; Best Known Methods for Static Control in Assembly/Test Environments; Julian Montoya, Intel; IBM, Beaverton, OR; www.esdnw.org

September 2001

Midwest ESD Chapter Meeting: September 5; ESD and Corrosion Control; Keith Donaldson, Engineered Materials, Inc.; Bimbo's Restaurant, Palatine, IL; www.midwestesd.org

ESDA Standards and Committee Meetings: September 6-9; Doubletree Hotel, Portland, OR; www.esda.org

David F. Barber Sr. Memorial Golf Tournament: September 8; Langdon Farms Golf Course, Aurora, OR; www.esda.org

EOS/ESD Symposium: September 9-13; Oregon Convention Center, Portland, OR; www.esda.org

ESDC Certification Exams: September 14; Portland, OR; www.esda.org

Silicon Valley EOS/ESD Society Membership Meeting: September 18; Ramada Inn, Sunnyvale, CA; www.esdsiva.org

October 2001

Midwest ESD Chapter Meeting: October 10; Selecting Static Control Flooring; Donna Robinson-Hahn, Agere Systems; Bimbo's Restaurant, Palatine, IL; www.midwestesd.org

November 2001

ESD Northwest Chapter Meeting: November 14; Doug Smith, Doug Smith Consulting; Sweetbrier Inn, Tualatin (Tentative); www.esdnw.org

Midwest ESD Chapter Meeting: November 14; Drive-By ESD; Ken Kern, Siemens Medical Systems; Bimbo's Restaurant, Palatine, IL; www.midwestesd.org

Association news

Standards site license program

In a large, multi-facility company, how do you economically provide ESD Association standards on a corporate wide basis to the dozens of people who need to work with them? Just as important, how do you ensure that the standards are complete and the most currently issued documents?

The answer, according to ESDA standards chair Ron Gibson, is the standards site license program. "The program is basically the standards subscription program for larger companies. For a single annual fee (\$5,000 US), the company receives a CD containing all standards documents and a company wide license to place the documents on their internal intranet or provide other company wide access for their internal company use."

The CD includes all standards, standard test methods, standard practices, glossary,

and the *ESD Handbook*. Any new or revised standards issued during the 12-month period are provided as automatic updates. The site license program can be renewed at the end of the license year.

"There are several benefits of this program," says Ron. "First, it's an economical and easy method of acquiring and using standards in a company that needs multiple copies in several different facilities or divisions. Second, it allows a company to provide wider and more consistent availability of the documents. Third, if you are an ISO 9000 certified company and reference ESDA standards in your internal ESD program, the site license is one method of ensuring that you always have the most current standards available."

For additional details about the site license program, contact ESD Association headquarters.

Pacific Northwest thanks Kay Adams



The Pacific Northwest local chapter recognized local chapters chair Kay Adams for her efforts in assisting the local chapter in starting up and developing their newly established chapter. The award was presented to Kay by Pacific Northwest president Jerry Dull during a recent local chapters committee meeting in Portland, OR,

EOS/ESD Symposium



Summary Program and Schedule

September 9-13, 2001
Oregon Convention Center
Portland, Oregon, USA

Saturday, September 8

Registration Opens
Charity Golf Tournament

Sunday, September 9

Tutorials

Monday, September 10

Tutorials
Spouse/Companion Portland
City Orientation Tours
Professional and Technical
Women's Reception
Welcome Reception (In Exhibit
Hall)
Exhibits

Tuesday, September 11

Awards Breakfast
Exhibits
Technical Sessions
Novel CMOS Devices
Materials I
Simulation and Modeling
Factory Issues
Magnetic Recording Heads I

Wednesday, September 12

Technical Sessions
Design – Process & Device
Technology
Materials II
Magnetic Recording Heads II

Exhibits

ESD Association Luncheon/
Keynote Speaker

Workshops

Spouse/Companion Tour

Thursday, September 13

Technical Sessions
RF ESD Design & Technology
Systems Issues
Transmission Line Pulsing &
Standardization
Tutorials

Friday, September 14

ESDC Technician Exam
ESDC Engineer Exam

Register early and save

You can save money and you can save time by registering in advance. Advance registration fees are valid if received no later than August 3, 2001. Registrations received after this date will be processed at the on-site fees.

You can save several hundred dollars by registering early. Plus, attendees who participate in the "total Symposium experience" and full-time students will save even more over last year's fees with this year's new fee structure.

To register, use the registration form you received in the mail, download the form from the ESDA web site, www.esda.org, or contact Association headquarters.

Registration and Fees

	Advance Fees On or Before <u>August 3, 2001</u>	On-Site Fees After <u>August 3, 2001</u>
Symposium		
ESD Association Members	\$495	\$695
Non-Members	\$595	\$695
Tutorials		
Sunday (Full Day)	\$475	\$550
Monday (Full Day)	\$475	\$550
Thursday (Full Day)	\$475	\$550
Thursday (Half Day, AM or PM)	\$275	\$275
Save on the Total Symposium Experience: Bundled Fees (Symposium plus 3 full days of tutorials)		
ESD Association Members	\$1,725	\$2,110
Non-Members	\$1,815	\$2,110
Student Fees: 50% discount for full-time students. Proof of enrollment required.		
Exhibits Only	No Charge	No Charge

Customize your Symposium experience

Whatever your interest or experience in ESD, you will find it at this year's Symposium. To help you better plan your participation, the Symposium is programmed in four technical tracks: *Design and Device Technology*, *Factory Issues and Materials*, *System Level ESD*, and *Magnetic Recording*. Use these tracks to customize and concentrate your experience along specific areas of interest. Remember, the tracks serve as guidelines and you can attend any event you wish.

Technical Tracks

Track 1

Design and Device Technology

Tutorials

ESD On-Chip Protection in Advanced Technologies (Sunday)
 Application and Process Dependent ESD Design Strategy (Monday)
 EOS/ESD Failure Models and Mechanisms (Monday)
 Electrostatic Fundamentals (Monday)
 ESD Protection and RF Design (Monday)
 Troubleshooting On-Chip ESD Failures (Monday)
 CDM Protection Design and Test (Thursday)
 EOS and ESD Laboratory Simulations for Failure Signature Analysis (Thursday)
 Electrostatic Calculations for the ESD Engineer (Thursday)
 Device Testing (Thursday)
 Transmission Line Pulse Testing of ICs (Thursday)

Technical Sessions

Novel CMOS Devices (Tuesday)
 Simulation and Modeling (Tuesday)
 Design – Process & Device Technology (Wednesday)
 RF ESD Design & Technology (Thursday)
 Transmission Line Pulsing & Standardization (Thursday)

Workshops

On-Chip Protection (Wednesday)
 How and Why TLP Is Used (Wednesday)
 How TLP Aids ESD Protection Designers (Wednesday)

Track 2

Factory Issues and Materials

Tutorials

ESD Basics (Sunday)
 Practical Application of ANSI ESD S20.20 (Monday)
 Electrostatic Fundamentals (Monday)
 In-Plant ESD Survey and Evaluation Measurements (Monday)
 ESD Control and Practices for Extremely Sensitive Devices (Monday)
 ESD Standards and Procedures (Thursday)
 Electrostatic Measurements (Thursday)
 Air Ionization: Issues and Answers (Thursday)
 Common Issues Complying with S20.20 and Training Demonstrations (Thursday)
 Cleanroom Electrostatic Charge Considerations (Thursday)

Technical Sessions

Materials I (Tuesday)
 Factory Issues (Tuesday)
 Materials II (Wednesday)

Workshops

ESD Control Program - Audit Problems (Wednesday)
 ESD in Cleanrooms (Wednesday)
 Grounding of People, Worksurfaces, and Walking Surfaces (Wednesday)

Track 3

System Level ESD

Tutorials

System Level ESD/EMI Design and Troubleshooting (Sunday)

EOS/ESD Failure Models and Mechanisms (Monday)
 Electrostatic Fundamentals (Monday)
 Electrostatic Measurements (Thursday)
 Electrostatic Calculations for the ESD Engineer (Thursday)

Technical Sessions

Systems Issues (Thursday)

Workshops

System Level ESD Considerations (Wednesday)

Track 4

Magnetic Recording

Tutorials

Understanding ESD in Magnetic Recording (Sunday)
 EOS/ESD Failure Models and Mechanisms (Monday)
 Electrostatic Fundamentals (Monday)
 ESD Control and Practices for Extremely Sensitive Devices (Monday)
 ESD Standards and Procedures (Thursday)
 EOS and ESD Laboratory Simulations for Failure Signature Analysis (Thursday)
 Electrostatic Measurements (Thursday)
 Air Ionization: Issues and Answers (Thursday)
 Electrostatic Calculations for the ESD Engineer (Thursday)
 Cleanroom Electrostatic Charge Considerations (Thursday)

Technical Sessions

Magnetic Recording Heads I (Tuesday)
 Magnetic Recording Heads II (Wednesday)

Workshops

ESD in Magnetic Recording (Wednesday)
 ESD in Cleanrooms (Wednesday)

Technical sessions feature new topic areas, invited papers

Another record...63 technical papers presented in 11 sessions will feature current international technological issues and research on ESD and EOS. The papers will be offered in parallel sessions to allow attendees to concentrate on those sessions of greatest interest to them. Reflecting the interest in new technologies, two new sessions are being presented this year: *RF ESD Design & Technology* and *Transmission Line Pulsing & Standardization*, both on Thursday, September 13.

Invited Papers

The technical sessions also feature invited papers including the award winning paper from the 2000 RCJ EOS/ESD Symposium-Japan. Summaries of the invited papers appear below.

Interconnect Reliability under ESD Conditions: Physics, Models, and Design Guidelines, K. Banerjee, Stanford University, Wednesday, September 12

Interconnect failure due to ESD stress conditions has become a reliability concern in high-performance designs. This paper will present an overview of the problem, discuss characterization techniques and open-circuit failure mechanisms in advanced multilayered AICu lines, contacts, and vias. Latent ESD damage of interconnects that significantly degrades

electromigration lifetimes will be discussed. Design guidelines for preventing open-circuit interconnect failures in ESD and I/O circuits will be examined.

The Future of RF Technology for Established Wireless Markets and Emerging Wireless Applications, D. R. Pehlke, Ericsson, Thursday, September 13

As the wireless market expands from voice to data networks, advances in radio architecture, circuit implementation, and semiconductor device technology all contribute to significant increases in integration, functionality, and reductions in cost for wireless consumer products. This paper presents a description of these advances, basic RFIC building block functionality, and the criteria used to evaluate semiconductor process technologies for optimal fit to those requirements.

ESD Evaluation by TLP Method on Advanced VLSI Devices, K. Katsuhiko, Y. Fukuda, OKI Electric Industry Co., Ltd. (Best Paper RCJ 2000 EOS/ESD Symposium, Japan), Thursday, September 13

TLP (transmission line pulsing) is an effective method to evaluate the ESD properties of advanced protection units. This paper covers SOI (silicon-on-insulator) ESD protection design by TLP analysis for

responses to ESD on diodes, resistors, and transistors. As a result of this study, it is proved that TLP is essential to designing ESD protection by response analysis.

Technical session schedule

Tuesday, September 11

Novel CMOS Devices
Materials I
Simulation and Modeling
Factory Issues
Magnetic Recording Heads I

Wednesday, September 12

Design – Process & Device Technology
Materials II
Magnetic Recording Heads II

Thursday, September 13

RF ESD Design & Technology
Systems Issues
Transmission Line Pulsing & Standardization

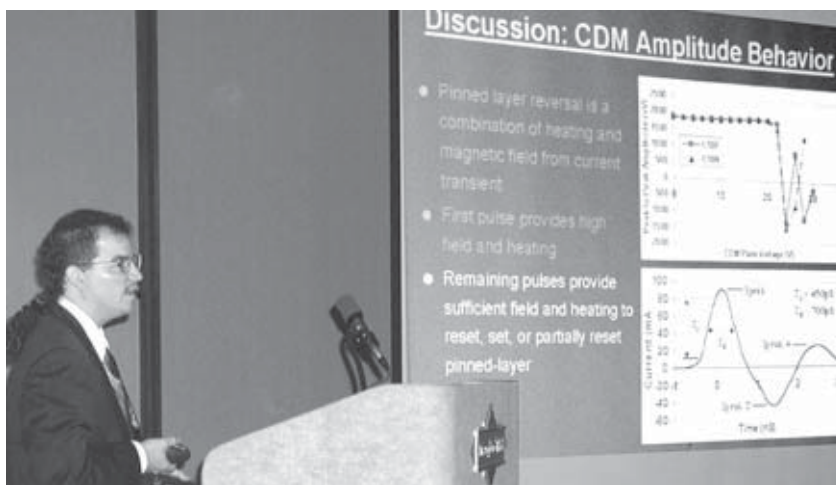
Exhibits

More than 120 exhibit spaces will display products and services from leading companies covering the broad spectrum of static protection, control, testing, and analysis, as well as prominent trade publications. Information on exhibiting may be obtained by contacting Scien-Tech Associates, Inc., P.O. Box 2097, Banner Elk, NC 28604-2097, Phone: 828-898-6375, Fax: 828-898-6379.

Exhibit Hours

Monday, September 10, 7:00 PM–10:00 PM
Tuesday, September 11, 9:00 AM–5:00 PM
Wednesday, September 12, 9:00 AM–Noon and 2:00 PM–4:00 PM

Exhibits are open to all persons interested in ESD and EOS products and services. You do not need to register for the Symposium or the tutorials in order to attend the exhibits.



Workshops provide interaction and discussion

Eight interactive workshops on Wednesday provide attendees with the opportunity to explore specific topics in depth. The workshops encourage discussion, questions, and audience interaction and participation.

Workshop Summary

Wednesday, September 12

A.1 ESD in Magnetic Recording

Moderator: Eric Granstrom, Seagate Technology

This workshop will be an open and highly interactive discussion of the latest ESD issues in magnetic recording. Extremely ESD sensitive components and the lack of convenient, integrated ESD protection devices make ESD a key concern in the magnetic recording industry. Panel members have direct experience with ESD testing, EMI and ESD control, as well as all aspects of GMR wafer, head, and disk drive assembly and manufacturing.

A.2 ESD Control Program - Audit Problems

Moderator: Bill Metz, Hewlett Packard

This interactive ESD control workshop will explore controversial areas that an

ESD auditor might encounter. The session will examine audit concerns, measurement techniques, strategies, and training tools when auditing to S20.20 and typical corporate ESD specifications.

A.3 On-Chip Protection

Moderator: Eugene Worley, Conexant Systems

Panelists will briefly discuss their approach to on-chip ESD protection and what steps they take to ensure successful implementation. In addition, open discussions will be held on these topics and a number of other ESD protection issues raised by the audience.

A.4 How and Why TLP Is Used and B.4 How TLP Aids ESD Protection Designers

Moderator: Jon Barth, Barth Electronics, Inc.

Two workshop sessions on TLP are scheduled this year. The first session will be directed at the basics of TLP analysis of ESD protection circuits, measurement data presentation, analysis, operating characteristics, differences between systems, and how TLP is used to test both packaged devices and circuits on wafer. The second session will delve into greater

detail and will also discuss the work of the new ESDA TLP standards working group, WG5.5. (Note--The TLP workshops will be audio recorded this year.)

B.1 System Level ESD Considerations

Moderator: Douglas Smith, D. C. Smith Consultants

Discussion topics will follow the system level ESD interests of the attendees and likely will include both theoretical and practical issues with an emphasis on the practical side. There also will be demonstrations of ESD principles as applied to the system level. Time and equipment permitting, audience members will be able to operate some of the experiments themselves.

B.2 ESD in Cleanrooms

Moderator: Tom Albano, Eastman Kodak Company

This workshop will cover issues of electrostatic control compatibility in cleanrooms and clean manufacturing areas. Panelists and attendees will discuss ESD, EMI, and contamination considerations. The focus will be on methods of identifying and avoiding problems.

B.3 Grounding of People, Worksurfaces, and Walking Surfaces

Moderator: Steve Koehn, 3M Company

Grounding of people, worksurfaces, and walking surfaces — how to tie everything together to make a top-notch electrostatic protective area. An overview of personal, worksurface, and walking surface grounding techniques and ESD Association standards will be presented.



In Portland, there's more than the Symposium

Portland, Oregon – City of Roses – City of Fountains – City of Bridges – River City – Rip City. It is a hub of international trade, the gateway to a natural wonderland.

Nestled in the heart of the Willamette Valley, Portland sits squarely between the Pacific Ocean and the 10,000 plus foot tops of the Cascade Mountain Range and Mt. Hood. You can literally go clamming at the beach during the day, have dinner in Portland that night, and go hiking in the mountains the next day.

Spouse, companion tours

Two special tours have been arranged for spouses and companions of attendees. A 2-hour Portland city tour is being offered on Monday, September 10, visiting many local attractions and districts. On Wednesday, September 12, spouses and companions may take a guided bus tour of Columbia River Gorge and Mt. Hood, visiting Multnomah Falls, Cascade Locks, Bonneville Dam, and Timberline Lodge. Sign-up for either tour is at the Oregon Convention Center. See the Symposium program for additional details.

On your own

When you're not in a technical session, workshop, tutorial, the exhibits, take time to enjoy this "foot-friendly" city. Cafes, restaurants, bookstores, galleries and specialty stores are waiting around every corner. Words of wisdom from famous thinkers are carved in the brickwork under one's feet. Bronze sea lions and bear cubs frolic among award-winning architecture. Green-suited concierges known as "Portland Guides" walk through downtown streets day and night answering questions and helping with directions.



Portland, OR, city of roses, features Mt. Hood in the background.

Photo courtesy of Portland Oregon Visitors Association

Pioneer Courthouse Square, a public plaza designed after the ancient Greek and Roman public squares, sits in the hub of downtown. Affectionately known as the "city's living room," Pioneer Courthouse Square brings together representatives from every possible social and cultural niche – a metro melting pot. On sunny summer days, the square hosts high-powered executives and purple-haired poets alike for "brown bag" concerts. If you finally tire of walking, "MAX," Tri-Met's light rail system, connects the Oregon Convention Center to downtown, the Rose Quarter, the Lloyd business and retail district, and outlying residential neighborhoods.

Dozens of parks in all shapes and sizes dot the entire city. One hundred acre **Washington Park** in the west hills above Portland encompasses the **International Rose Test Gardens** with more than 400 varieties of roses, the peaceful contemplation of the **Japanese Gardens** and the

Oregon Zoo with its world-class elephant exhibit. Washington Park also provides a breathtaking panorama of Portland with Mt. Hood in the background.

Tom McCall Waterfront Park traces the west side of the **Willamette River** for two and one-half miles, and reverberates throughout the summer months with cultural, musical and gastronomic festivals. The river itself winds through the center of Portland like a bright blue ribbon, where tugboats, sailboats, historic sternwheelers, water skiers, rowers and salmon fisherman recreate.

For more information on Portland, visit the web at www.pova.org

Some facts about Portland

- Saturday Market is the largest continuously operating open-air crafts market in the US.
- Powell's City of Books, occupying an entire city block, is the country's largest new-and-used book store.
- Portlandia is the second largest hammered copper statue in the world (the Statue of Liberty is the first).
- Portland's International Rose Test Garden is the oldest in the nation.
- More Asian elephants (27 to date) have been born in Portland than in any other North American city.
- Portland has more movie theaters and restaurants per capita than any other city in the United States.
- Portland has more microbreweries and brew pubs than any other city in the nation.
- Portland is the only U.S. city with an extinct volcano (Mount Tabor) within its city limits.
- The Port of Portland is home to one of the world's largest floating dry docks, able to handle ships nearly three football fields in length. The port's combined terminals handle \$9 billion worth of cargo per year.

Tutorials offer in-depth education

Three days of in-depth tutorials provide opportunities for detailed study of specific topic areas. Internationally recognized instructors will present a total of 22 courses appealing to both beginners and advanced practitioners.

Organized in four educational tracks, *Factory, Protection Design, Magnetic Recording and Failure Analysis*, and *Systems and Technology*, the program opens Sunday, September 9 with four full day tutorials. Eighteen additional sessions will be presented on Monday, September 10, and Thursday, September 13.

Several new tutorials are being offered this year, and several tutorials from past years have been expanded or revised. Even if you may have attended the tutorials in the past, you will find new or expanded offerings. New sessions this year include *Practical Application of ANSI/ESD S20.20*; *Application and Process Dependent Design Strategy*; *ESD Control and Practices for Extremely Sensitive Devices*; *CDM Protection Design and Test*; and *Common Issues Complying with S20.20 and Training Demonstrations*. In addition, several tutorials will help you prepare to take the ESDC certification examinations for engineers and technicians.

To help you make your selections, several tutorials are highlighted below. The complete list of tutorials and abstracts is in the Symposium program.

Tutorial Highlights

Tutorial A: ESD Basics

8:30 AM–4:30 PM, Sunday, September 10
Burt Unger, Burt Unger Associates

One of the most popular offerings year after year, the ESD Basics tutorial covers the fundamentals of ESD. Whether you are a newly appointed ESD coordinator or need a review to prepare for the ESDC certification, exam, this tutorial will provide answers, answers, and more answers. The course will include the fundamentals of charging and discharging, how and why different materials charge, and how to measure the charge. Instructor Burt Unger will discuss the three generalized models that describe how ESD events occur, the use and pitfalls of field meter, various ESD control techniques, and properties and characteristics of ESD control products.

Tutorial E: Practical Application of ANSI ESD S20.20

8:30 AM–Noon, Monday, September 10
Dave Leeson, Motorola

The ANSI/ESD S20.20 ESD control program standard details the requirements for the design, implementation and maintenance of a factory level ESD control program. This session will provide operation managers, quality assurance managers, ESD coordinators, and technical and engineering staff with guidance to help them design an ESD control program that is specific to the needs of the implementing organization. The tutorial will cover tailoring the requirements, personnel training plan, and compliance verification plan focusing on the seven primary technical elements necessary for a compliant and relevant ESD control program.

Tutorial S: Common Issues Complying with S20.20 and Training Demonstrations

1:00 PM–2:40 PM, Thursday, September 13
Ted Dangelmeyer, Lucent Technologies

In this highly interactive companion to tutorial E, you will learn about the ex-

continued on page 10

ESD Tutorial Tracks			
Track 1 Factory	Track 2 Protection Design	Track 3 Magnetic Recording and Failure Analysis	Track 4 Systems and Technology
ESD Basics Practical Application of ANSI ESD S20.20 In-Plant ESD Survey and Evaluation Measurements ESD Standards and Procedures Common Issues Complying with S20.20 and Training Demonstrations Cleanroom Electrostatic Charge Considerations	ESD On-Chip Protection in Advanced Technologies Application and Process Dependent ESD Design Strategy ESD Protection and RF Design CDM Protection Design and Test Device Testing Transmission Line Pulse Testing of ICs	Understanding ESD in Magnetic Recording EOS/ESD Failure Models and Mechanisms ESD Control and Practices for Extremely Sensitive Devices EOS and ESD Laboratory Simulations for Failure Signature Analysis	System Level ESD/EMI Design and Troubleshooting Electrostatic Fundamentals Troubleshooting On-Chip ESD Failures Electrostatic Measurements Air Ionization: Issues and Answers Electrostatic Calculations for the ESD Engineer

continued from page 9

Symposium tutorials

periences of the instructor's company becoming certified to S20.20. A review of the two-day in-depth audit will give you insight on what to expect and how to prepare for certification. In addition, you will be presented with new training techniques that will help you more clearly demonstrate ESD events in training programs.

Tutorial F: Application and Process Dependent ESD Design Strategy

8:30 AM–Noon, Monday, September 10
James Miller, Motorola

The engineer developing an efficient and robust ESD protection network for an advanced deep submicron CMOS integrated circuit must first choose an appropriate overall ESD design strategy. This tutorial will review examples of various design strategies, comparing their advantages and disadvantages and discussing the factors should affect your choice of design strategy, such as process technology, IC application, in-house ESD device development resources, and IC manufacturing business model.

Tutorial K: ESD Control and Practices for Extremely Sensitive Devices

1:00 PM–4:30 PM, Monday, September 10
Dr. Albert Wallash, Maxtor Corporation

An offshoot of last year's Magnetic Recording tutorial, this will focus exclusively on *extremely* ESD sensitive devices like laser diodes, RF devices, semiconductor devices without protection diodes and GMR/TMR magnetic recording devices. The main emphasis of the tutorial will be on understanding the process steps that

damage these devices and how to modify them in simple ways to prevent the damage.

Tutorial J: ESD Protection and RF Design

1:00 PM–4:30 PM, Monday, September 10
Dr. Steven Voldman, IBM Micro-electronics

Presented last year for the first time, this tutorial will deal with on-chip ESD protection in RF technologies and products, which is being spurred by the growth of GHz applications in wired, wireless, storage and test applications. This session will include a brief review of RF parameters with examples of typical RF circuits and comparative study of ESD devices for RF ESD applications. The tutorial will discuss RF design practices and input pin protection and ESD power clamp circuits and ESD failure mechanisms and failure criteria. Gallium arsenide (GaAs), silicon-on-sapphire (SOS) and silicon-on-insulator (SOI) for RF ESD applications used in industry will be briefly covered as well.

Tutorial N: CDM Protection Design and Test

8:30 AM–Noon, Thursday, September 13
Koen Verhaege, Sarnoff Europe

This totally new tutorial is an advanced ESD design class that focuses solely on the protection and testing for charged device model (CDM) ESD. The CDM stress event will be reviewed as an IC phenomenon, rather than a standard test method. ESD clamping behavior of elementary (HBM/MM) protection devices will be assessed. Published literature and cases related to CDM on-chip protection will be studied. A set of 'golden rules' for successful CDM ESD protection design will be defined. Also, a general CDM protection strategy for IO libraries and full chip will be discussed. Attendees can expect to acquire some advanced/CDM protection design skills and know-how.

continued on page 11



*Keynote address***Silicon technology in the new millennium**

Where lies the future in electronics technology? The answers not only affect our lives as consumers, but also our careers and our efforts in ESD control and protection.

Tak H. Ning, IBM Fellow at the IBM Thomas J. Watson Research Center in Yorktown Heights, New York, will gaze into his crystal ball at Wednesday's keynote address during the Association's annual luncheon, Wednesday, September 12.

Silicon technology development is at a crossroad, after progressing at an exponential rate for more than thirty years. Ning suggests that it is now clear that CMOS devices, which have been the key enabler of rapid progress in the computer and consumer electronics industries for the past fifteen years or so, are fast approaching their limits. He proposes that new materials and novel device structures need to be explored in an effort to extend CMOS device performance as far as pos-



Tak H. Ning

sible. In addition, circuit designers are learning to live with significant amounts of leakage currents.

He further proposes that future silicon technology development will detour around the CMOS limits, becoming more diverse and driven in application-specific directions. System-on-chip and system-on-package are the high-level themes. BiCMOS, particularly SOI BiCMOS, will emerge as an important technology platform for the growing market of mixed-signal systems.

Ning received his Ph. D. degree in physics from the University of Illinois at Urbana-Champaign in 1971. He joined IBM Thomas J. Watson Research Center at Yorktown Heights, New York in 1973. He has made significant contributions to silicon device physics, and to bipolar, CMOS, and DRAM technologies. As manager of the silicon device technology department between 1982 and 1991, he directed the development of submicron bipolar and CMOS technologies in IBM Research as

well as led his team in exploring SOI and EEPROM devices.

Since 1991, he has been an IBM Fellow, focusing on VLSI industry directions, technology trends, and opportunities beyond CMOS scaling.

He is a member of the U.S. National Academy of Engineering, and a fellow of the IEEE and the American Physical Society. He has authored or co-authored more than 100 technical papers, 21 U.S. patents, and a book.

He is a fellow of the American Physical Society. Tak was named IEEE Fellow for his contributions to the understanding of hot electrons in MOSFET devices.

He is a member of the National Academy of Engineering. He received the IEEE Electron Device Society 1989 J.J. Ebers Award, the IEEE 1991 Jack A. Morton Award, the 1998 Pan Wen-Yuan Foundation (Taiwan) Outstanding Research Award, and the IEEE 2000 CICC Best Paper Award.

With technology development in electronics a key to the future work in ESD, this is one look into the future that you won't want to miss.

continued from page 10

Symposium tutorials**Preparing for the certification exams**

If you're considering taking either the ESDC Engineer or ESDC Technician certification exam on Friday, September 14, there are a number of tutorials that will help you prepare. The following tutorials have been identified as being especially useful in preparing for the exams.

Certification preparation tutorials**Preparing for the Technician Exam**

ESD Basics (Sunday)
Practical Application of ANSI ESD S20.20 (Monday)

Electrostatic Fundamentals (Monday)
In-Plant ESD Survey and Evaluation Measurements (Monday)
ESD Standards and Procedures (Thursday)
Electrostatic Measurements (Thursday)
Air Ionization: Issues and Answers (Thursday)

Preparing for the Engineer Exam

ESD Basics (Sunday)
EOS/ESD Failure Models and Mechanisms (Monday)
Electrostatic Fundamentals (Monday)

In-Plant ESD Survey and Evaluation Measurements (Monday)
ESD Standards and Procedures (Thursday)
Electrostatic Measurements (Thursday)
Air Ionization: Issues and Answers (Thursday)
Electrostatic Calculations for the ESD Engineer (Thursday)
Device Testing (Thursday)

Additional information is available in the registration area, at the ESD Association booth, or by contacting ESD Association headquarters.

May 2001 standards meetings

by

Michael T. Brandt, Editor

The June 2001 ESD Association standards committee and working group meetings concentrated primarily on reviewing existing documents and the continued development of technical reports, although there was other activity in the device testing working groups as well as the recently formed working groups on gloves and TLP testing.

Five-year review

Three existing standards completed their five-year review process required by ANSI and ESD Association procedures. No technical changes were made and the following documents were reaffirmed as standards test methods:

STM 5.1: Electrostatic Discharge Sensitivity Testing — Human Body Model

STM 7.1: Floor Materials — Resistive Characterization of Materials

STM11.11: Surface Resistance Measurement of Static Dissipative Planar Materials

Working group activities

Ionization WG-3 reviewed its draft technical report covering alternate test methods to the charged plate monitor for determining discharge time and offset voltage in ionizers. The group discussed test results using smaller sized plates, determined that stray capacitance was an important issue and developed a list of improvements to the test fixture to address the issue. Future work will include an investigation of plate perimeter versus plate area effects on discharge time testing.

Worksurfaces WG-4 reviewed comments on its draft technical report *A Survey of Static Control Worksurfaces and Grounding Mechanisms*. A revised draft of the document is targeted for completion by the September meeting series.

Machine Model Device Testing WG-5.2 continued its review of a proposed technical report discussing the reasons

for not reducing the number of pulses per stress level from three to one and reducing the time between pulses from 1 second to 0.5 seconds. The group is planning an industry survey on machine model ESD.

CDM Device Testing WG-5.3.1 is coordinating inputs and issues to define direction and action items for future work.

Socket Discharge Model (SDM) Device Testing WG-5.3.2 completed work on an article "What is the Future of the SDM Test Method" for publication in *Compliance Engineering* magazine. The group also has developed a survey of CDM test equipment. (See article on page 13 of this issue of *Threshold*). Work is continuing on a draft standard practice document based on the 1994 draft document and the technical report prepared in 1999. The goal is to have a draft document ready for comment and review at the September meeting series.

Transient Latch-Up Device Testing WG-5.4 completed wordsmithing and technical review of an initial draft standard practice covering transient latch-up and submitted it to TAS for further review and comment.

Transmission Line Pulsing WG-5.5 held its first formal meeting with the objective of developing a standard practice covering TLP testing. Planning and work on an initial draft will be covered in a series of conference calls prior to the September meeting series.

Footwear WG-9 is working on editorial revisions to an initial draft standard for measuring the electrical resistance of foot grounders.

Handlers WG-10 reviewed comments on its draft technical report on automated handlers. The group is clarifying references to CDM and HBM models as well as issues concerning soft grounds versus hard grounds. The group anticipates having a revised draft by the September meeting series.

Packaging WG-11 expects to finalize a draft revision EIA-541 by the fall meet-

ing series. Initial work with a proposed probe for Two Point Resistance (Packaging) WG-11.13 has shown good repeatability in initial testing and the proposed procedure is ready for round-robin testing.

Simulators 14 is looking at the effects or radiated fields on equipment and measurement procedures and will be polling industry for input and interest in this area.

Gloves WG-15 is evaluating fixtures for making resistance measurements of

continued on page 13

Tentative Schedule September Standards Meeting Series

DoubleTree Hotel Portland—Lloyd Center, Portland, OR
September 6-9, 2001

Thursday, September 6, 2001

2:00 PM Ionization WG-3
Device Testing Working Groups WG-5

Friday, September 7, 2001

8:00 AM: Worksurfaces WG-4
Device Testing Working Groups WG-5
Handlers WG-10
1:00 PM Footwear WG-9
Work Stations WG-53
Cleanroom Considerations WG-55
5:30 PM: Daily Activity Review

Saturday, September 8, 2001

8:00 AM: Device Testing Working Groups WG-5
Flooring WG-7
Packaging WG-11

Sunday, September 9, 2001

8:00 AM: Handtools WG-13
Simulators WG-14
Gloves WG-15
1:00 PM: Standards Committee

What is your opinion on CDM test simulators?

The ESD Association standards working group 5.3.2 on socketed discharge model (SDM) would like your help with a questionnaire on CDM/SDM test equipment.

To assist the working group in developing an appropriate standard test method, they would like to know what the ESD test equipment user community thinks about the commercially available CDM test simulators.

The working group has developed a questionnaire on CDM test simulators that is available on the ESD Association web site.

Today, the user can do device level CDM tests by using the field induced test method (CDM) (Figure 1) or the socketed device model (SDM) test method (Figure 2), previously called the socketed CDM test method. Both types of CDM test methods are intended to simulate discharge events that occur when a charged IC device dis-

charges directly through one of its pins into a very low impedance ground. Real world CDM events can occur during automatic handling or placement of IC devices during the manufacturing operations. The discharge current waveforms from the two types of CDM test equipment show very fast rise times ($< 1\text{ns}$) and very short pulse duration ($< 20\text{ns}$). Both test methods can produce failure mechanisms such as gate oxide ruptures in IC devices.

If you are a user of either type of CDM test equipment, the working group invites you to answer a few questions regarding your opinion on how effective the current test equipment is in performing CDM simulation tests. Please visit the ESD Association web site, www.esda.org, click on the CDM survey text on the home page, and spend a few minutes to answer the attached questions. The working group thanks you for your input.

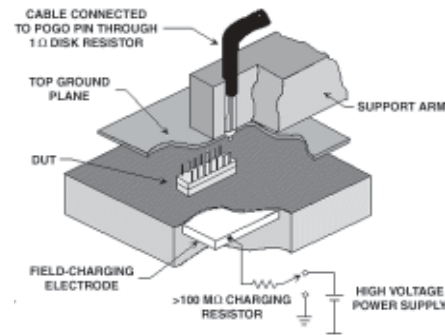


Figure 1: Field induced CDM simulator

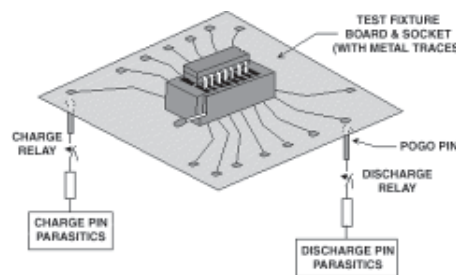


Figure 2: Socketed device model simulator

continued from page 12

Standards update

gloves. Variables affecting the measurements are being identified. Possible measurement methods under discussion include measuring between the thumb and forefinger, between a gloved finger and an ungloved finger, and between a gloved finger and the body.

Workstations WG-53 is continuing a 5-year review of the existing advisory and is working on a section on troubleshooting guidance to assist users in meeting the compliance verification requirements of *ANSI/ESD S20.20*. The existing advisory is being updated with a goal of converting it to a standard practice or standard test method.

Cleanrooms WG-55 has nearly completed its technical report, which should be ready for publication in late spring. The group is also working on future additions covering garments and packaging that may be added later.



Facility expansion and remodeling complete

The expansion and remodeling of Association offices in Rome, NY is now complete. The expansion includes a training and meeting center with breakout rooms, expanded file and document space, a member service area for improved mailings and communication, production areas for supporting Symposium, standards, certification and education activities, and a new shipping and receiving area. In addition, the project provides a more efficient and pleasant office space (above) for Association staff. The expansion from 1,700 ft² to approximately 5,000 ft² was made possible when the tenants in the adjoining office vacated the space, allowing the Association to lease additional space and remodel very economically.

Voltage of insulators?

Editors Note: The following letter from John Chubb comments on the "Voltage of Insulators?" article by Niels Jonassen (Mr. Static) that appeared in the May/June issue of Threshold.

Voltage on insulators IS meaningful

I disagree with the notes presented by Niels Jonassen in the latest issue of *Threshold*. It is not "meaningless" to talk of the voltage on an insulator. The voltage is there – but needs to be considered and measured with care.

If I approach a surface with a fieldmeter and adjust the voltage to get zero electric field (voltage follower probe) then, if one is sufficiently close that there are no significant influences from anything else nearby, one will have a measure of the local potential of the surface. This is true whether the surface is a conductor or an insulator. This is an entirely "meaningful" concept.

If I approach a surface with an earthed fieldmeter, then, as the fieldmeter gets closer, the added capacitance will affect the actual potential of the surface (as Jonassen rightly points out). The variation of the surface potential however depends on the relative capacitance experienced by the surface charge from the nearby fieldmeter and from all other sources. To keep the influence of the fieldmeter low, it is obviously sensible to keep the separation distance fairly large – but the larger the separation, the more readings are influenced by the size of the area charged and by any other sources of charge around.

It is perfectly sound to set up a fieldmeter to read surface voltage at a defined separation distance so long as one remembers that the presence of the fieldmeter may influence the observations.

Many of the problems from "static" arise not from the charge on surfaces per se, but from the influence such charge has on things nearby via the electric fields that the charge creates. These effects include induction charging of items, the initiation of electrostatic spark breakdown, and the attraction of dust, dirt and thin films. The effects are the same as if the dielectric surface had a potential – so why the distinction?

It is worth noting that there are problems in using a fieldmeter to measure surface charge density – even if the fieldmeter is properly guarded to ensure field uniformity. On many materials surface charge may experience a high capacitance from within the material itself (1,2). In this situation the simple relation between charge density and local electric field is not directly applicable.

John Chubb
John Chubb Instrumentation
5/13/01

¹J. N. Chubb, "The assessment of materials by tribo and corona charging and charge decay measurements" *Electrostatics 1999*, Univ Cambridge, March 1999, Inst Phys Confr Series 163, p. 329.

²J. N. Chubb, "Measurement of tribo and corona charging features of materials for assessment of risks from static electricity" *Trans IEEE, Ind Appl* **36** (6), Nov/Dec 2000, p.1515-1522.

Mr. Static Replies

In his reply to my paper "Voltage of Insulators?" John Chubb tries to avoid the issue by talking about something different. I was showing the meaninglessness of characterizing an insulator as a whole by a single voltage figure, i.e. the voltage of the insulator. Instead Mr. Chubb talks about the voltage **on** an insulator, i.e. *surface voltage*. As shown in my paper, of

course surface voltages do exist, and of course this concept is meaningful. Apart from the fact that it also does not make sense to talk about the surface potential of a conductor as Mr. Chubb claims, all points in and on a conductor have the same voltage (or potential)

Except in very special cases, the surface voltage will change from point to point on the insulator. So, for that reason alone you cannot characterize the insulator with a (one) voltage as you can with a conductor.

But my paper is **not** primarily dealing with surface potentials, which are useful for estimating one quantity, the surface charge density.

John Chubb asks the question: Why distinguish between dielectric surfaces and insulated conductors? If they are charged, they have the same effects.

But that is exactly the point: they don't.

For the same field strength, the plate out of airborne particulates and cling events may be (almost) the same. But induction is different, and even more so is the initiation and whole course of a discharge process. A discharge from a conductor (sometimes, but not always, a spark) will dissipate all the energy stored in the field in the discharge. And this energy can be readily calculated from the voltage and capacitance of the conductor. A discharge from an insulator (never a spark) will dissipate only part of the field energy, and there's no way this energy can be calculated.

And this indisputable difference is essentially the reason it does not make sense to talk about the voltage (nor the capacitance) of an insulator.

Niels Jonassen
Mr. Static
5/30/01

Institutional Listings

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<p>Howell Packaging, Division of F.M. Howell & Company P.O. Box 286, Elmira, NY 14902 Tel: 607-734-6291 Fax: 607-734-8667 Designers & Manufacturers of ESD Protective Packaging, Paperboard & Thermoformed Plastic, In-House Testing</p>	<p>Julie Industries, Inc. 355 Middlesex Avenue, Wilmington, MA 01887-0783 Tel: 978-988-8802 Fax: 978-988-8803 Email: questions@julieindustries.com StaticSmart™ products including carpet, rubber & polymeric flooring, personnel grounding products & materials, ESD workstations and chairs</p>
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