

## **Yeshwant Subramanian**

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### **OBJECTIVE**

A full time position in the area of ESD Design/technology development or any related area

### **EDUCATION**

PhD candidate in Electrical Engineering, University of Washington, 09/99 – 03/05, GPA:3.58/4

**MSEE**, University of Washington, 08/98, GPA: 3.71/4

**B.Tech** in Electrical and Electronics Engineering, IIT, Madras, India (July 1996)

### **SUMMARY OF SKILLS**

Very proficient in SPICE and Saber Simulation, MATLAB, C++ simulations and working on convergence issues

Substantial characterization experience using oscilloscopes, parameter analyzers, power sources, pulse generators, ESD equipment

Substantial experience with FA equipment and deprocessing issues

Substantial experience with Cadence, IC Station, Eldo, Liberty, Assura, Calibre, MAGIC, L-Edit  
ESD knowledge and 3 years industry experience in ESD

### **EMPLOYMENT**

#### **Mobility Semiconductor San Jose CA**

**10/08-present**

##### *Analog IC Design Engineer*

Design of a 40-100MHz PLL with 2GHz clock and 4GHz VCO

PTAT voltage reference design

Design of LVDS buffer

C++ and TCL programming

Use of tools like MAGIC, LEdit for layout

#### **Cypress Semiconductor, San Jose CA**

**01/07 –**

**12/08**

##### *Electrical Design Engineer Staff*

Developed and characterized ESD IP for PSoC products and existing Cypress products. Worked on the layout and characterization of ESD structures.

Participated in ESD Review Board and provided layout/circuit feedback on ESD issues

Developed ESD testchip modules (using Cadence) consisting of ESD structures in a given library

Performed physical verification (DRC, LVS) checks on ESD cells

Performed physical verification and IP Accept checks on completed modules/libraries and IP submission

Worked on ESD defects- involving conduction of HBM and latchup testing followed by characterization of parts and documentation of results

Extensively characterized ESD trigger circuits and documented results

Developed OPUS simulation testbench for ESD trigger circuits and IP Cells and ran verification test cases for comparison to expt

Mentored co-op employees in ESD group

Completed several training courses on ESD testing, PSoC, Reliability. Experience gained with IMCS 700, Oryx 11000, UTI, latchup testing, Barth Electronics 4002 TLP tester

Gained familiarity with JEDEC/ESDA ESD standards

#### **Advance Micro Devices (AMD), Austin TX**

**08/05-**

**11/06**

***Product Development Engineer***

Employed in Quality and Reliability Engineering group working on ESD related failure analysis and characterization on ICs - (K8 and GX3 products)  
Conduction of HBM, MM and CDM tests to determine the causes of failures (ESD Debug). Worked with 90nm and 65nm technologies  
Submission of failed parts for FA and review of FA results. Usage of a variety of device analysis (DA) equipment including characterization (UTI), TIVA, SEM, IREM, TDR, X-Ray etc for ESD and HTOL related debug purposes  
Participating in ESD task force and providing product/layout related feedback on ESD issues.  
Experience in usage of ESD HBM and CDM equipment and software  
Some experience in TLP testing. Also worked with yield / data software to investigate effects of device parameters on ESD fails

**Qualcomm, Inc. San Diego CA** **09/04 – 12/04**

***Interim Engineering Intern***

Interned in ESD - I/O VLSI Design group. Worked on design and optimization of RC clamp circuits using HSPICE  
Prepared detailed documentation of ESD protection schemes for 130nm and 90nm processes  
Prepared support materials for ESD design reviews. Simulated HBM, CDM and TLP pulses on RC Clamps. Compared RC clamps developed in house with RC clamps used in other companies

**University of Washington** **09/99 – 03/05**

***Research Assistant, Department of Electrical Engineering***

Dissertation project (07/00 – 03/05) : Development of compact SPICE models of ESD protection devices for ESD circuit simulation  
MEMS (09/99- 07/00): Development of compact MEMS models using Saber

**Coventor Inc., Cambridge, MA** **07/99 – 09/99**

***Intern***

Development/documentation of compact models for a MOSFET, BJT, 2D beam element and inkjet for usage in MEMCAD

**Texas Instruments, Inc., Dallas TX** **08/98 – 06/99**

***Power SPICE Modeling Engineer***

Development, extraction and support of BSIM3v3 based SPICE model cards for LDMOS and DEMOS devices  
Development of testchips for characterization of LDMOS and DEMOS devices  
Development of complementary SPICE netlist code to account for unusual behavior encountered in LDMOSFETs using the BSIM3v3 model as base

**Texas Instruments Inc, Dallas TX** **06/97 – 12/97**

***Co-op Student***

Development, validation and extraction of compact models for LDMOS devices  
Worked on implementing Saber models in internal software for parameter extraction  
Successfully developed and validated Saber models for LDMOS devices

**University of Washington** **09/96 – 07/98**

***Research Assistant, Department of Electrical Engineering***

Completed development, validation (including characterization using HP 4145B, HP 4163A

instruments and LABVIEW) and documentation of a compact model for an LDMOSFET, towards MSEE thesis  
Development of compact Saber models for Vertical and Lateral DMOS devices

### **SKILLS**

- C++, LABVIEW, HSPICE, Cadence, Analog Artist, IC Station, ASIM/ELDO, Nanosim, IPVGEN, Liberty tools, VHDL, Saber, Matlab, MEDICI Microtec, L-edit, MAGIC, DASH

### **CHARACTERIZATION EQUIPMENT AND SOFTWARE TOOLS**

- Labview, Barth 4002 TLP tester, Oryx 11000, IMCS700, HP4142, HP4145, Agilent 4156C, HP4284, HP4263A, UTI Curvetracing systems, X-Ray equipment, Camelot

### **TRAINING COURSE PROJECTS**

- IC Station- Accelerating your productivity
- PSOC Professional Associate Certification at Cypress Semi
- Time management
- Precision Question and Answering
- Design for Manufacturability

### **IC DESIGN/COMPUTER COURSE PROJECTS**

- Project oriented course- Analog IC Design (EE536) at Univ of Wash – High Speed OpAmp using MOSIS
- Project oriented course -Digital IC Design (EE476) at Univ of Wash- Traffic Signal Controller - MOSIS
- Several courses at undergrad level taken at University of Washington/IIT involving C++ programming (Data Structures), VAX/VMS, Assembly language programming (Intel x86 SDK)TCL/TK, OrCad, SmARTwork

### **CONFERENCE PAPERS**

1. Y. Subramanian and R.B. Darling, "Compact Modeling of Tunneling Breakdown in PN junctions for computer aided ESD design (CAD for ESD).", Proc. 5th Int. Conf. Modeling and Simulation of Microsystems, pp. 628-631, 03/02, San Juan, Puerto Rico
2. Y. Subramanian and R.B. Darling " Compact Modeling of Avalanche Breakdown in PN junctions for Computer-Aided ESD design (CAD for ESD)", Proc. 4th Int. Conf. Modeling and Simulation of Microsystems, pp. 48-51, 03/01, Hilton Head Island, SC
3. Y. Subramanian, M. Azadeh and R.B. Darling, "Compact Models for Pixels with Smart Illumination", Proc. Third Int. Conference on Modeling and Simulation of Microsystems, pp. 229-232, 03/00, San Diego, CA
4. Y. Subramanian, P.O. Lauritzen and K.R. Green, "A Compact Model for a Lateral Diffused MOSFET Using the Lumped-Charge Methodology", proc. Second Int. Conference on Modeling and Simulation of Microsystems, pp.284-288, 04/99, San Juan, Puerto Rico
5. Y. Subramanian, P.O. Lauritzen and K.R. Green, "Two Lumped-Charge Based Power MOSFET models", Proc. of IEEE Workshop on Computers in Power Electronics, pp. 1-10, Como, Italy, 07/98

### **AWARDS/ACHIEVEMENTS**

- All India 248<sup>th</sup> Rank in IIT JEE for entrance to IITs
- CDADIC best poster award for research in ESD- 2004
- 5<sup>th</sup> in a class of 41 students in IIT Madras Btech program- 1996

### **REFERENCES**

- Available upon request