



THRESHOLD™

The ESD Association newsletter, published for everyone with an interest in the understanding and control of electrostatic discharge.

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The International ESD Workshop (IEW)

May 16-19, 2011 Stanford Sierra Conference Center, Lake Tahoe, CA

The International ESD Workshop (IEW) management committee is pleased to announce the final technical program for the 2011 IEW, with a strong series of technical presentations, seminars, invited talks, special interest group meetings, and discussion groups addressing the hottest topics in ESD. The technical program includes advances in system-level and high-voltage ESD as well as studies of component protection techniques for advanced technologies. An expanded poster format provides an opportunity for deep technical discussions and networking. Technical sessions feature presentations covering the following subjects:

- System-Level ESD
- Device-Level ESD
- Tester Interactions
- ESDA Tools
- Class-0 ESD Protection

The invited talks at this year's workshop will focus on communication electronics, with speakers from the cell phone, mobile device, and network communication fields describing ESD problems and solutions in their industries. In addition, our keynote

speaker, Greg Leyh, who has been featured on The Discovery Channel's show *Mythbusters*, will discuss the large-scale physics of atmospheric electricity.

Ability of Evanescent Electric Fields to Deliver Potentially Devastating Amounts of Power over Laboratory-Scale Distances

Greg Leyh, Nevada Lightning Laboratory

Cell Phone Front End ESD Challenges

Eugene Worley, Qualcomm

ESD Design and Performance Challenges in High-Speed Serial Links of 20 Gb/s and Beyond

Thomas Morf (Presenter), Junjun Li, Christian Menolfi, Thomas Toifl, Peter Dill, Marcel Kossel, Peter Buchmann, Matthias Braendli, IBM; Vivek Sharma, Andrea Prati, Miromico

System Level ESD: A Networking Perspective

Richard Wong, Cisco Systems

High Speed I/O (Transceiver) Design

Charles Chu, Altera Corporation

The seminars this year cover four important topics addressing the challenges of ESD design in a changing industry. Seminar topics



Continued on page 11

From the President

Inside ESDA....



Donn G. Bellmore

While many of us continue to deal with winter weather, I hope spring thoughts fill the air.

We have already had a busy start to our year with the successful completion of our new ESD Essentials for ESD Programs seminars held in Shenzhen, China and in Anaheim, CA.

The mission of the ESDA has been and continues to be, "Become the recognized global leader serving industry in the field of electrostatic mitigation". The goals of the ESD Association to accomplish our mission are to "Provide Solutions and Become Known". There are a number of ways to accomplish our goals and mission. The Standards Business Unit serves our worldwide industry through the generation of Standards, Standard Test Methods, Standard Practices, and Technical Reports. The Standards Business Unit is continually monitoring new technology, while updating and re-

viewing our standards. The Annual EOS/ESD Symposium addresses our mission and goals through the myriad of components designed to share information, showcase equipment and services, and educate members of our industry. Education is another important Business Unit that serves our industry and helps us meet our goals.

In order for Education to address our Mission and Goals, several factors need to accompany our course line-up. First and foremost, they must be up to date, pertinent to industry, affordable, and convenient, to both the student and the instructor. Affordability and convenience are important to each component. This requires intense consideration, careful thought, and detailed planning. One goal is to offer all of the professional certification courses at the Symposium and also once outside of the Symposium during the course of a year. Scheduling these courses can be a challenge. ESDA strives to offer courses in new locations each year for those who have limited travel options, and also schedule symposium courses for those who have planned courses based on the previous year's symposium schedule. To bring new material to our customers, ESDA also offers several non-certification classes

each year at the Symposium.

The Essentials for ESD Programs course is a new two day seminar that offers a basic set of factory technologies and procedures designed for managers, technicians, and specialists who want ESD control program training and information. A similar Essentials for Device Design course is under development. It will offer a basic set of device design technologies for engineers, technicians, and specialists who want ESD control training for device manufacturing. The Essentials for Device Design Seminar is expected to be available in June of this year. Both of the Essentials seminars have been developed to assist ESDA in offering global ESD training opportunities. The seminars are also excellent review courses for anyone pursuing ESDA Professional certification.

Our education programs have had increased recognition through ESDA's cooperative relationship with iNARTE. We now offer courses in conjunction with their certification programs and jointly offer both iNARTE and ESDA certification exams at our annual symposium. Many ESDA courses, while not required by iNARTE, prove to be very beneficial to the members in completing iNARTE certification and exams offered by iNARTE around the world. The

Continued on page 3

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From the President

Continued from page 2

ESDA and iNARTE Organizations are committed to the education of our industries and are working closely together to provide related training programs.

As an added benefit to ESDA customers who cannot travel, we offer several online training courses each year; these classes are also archived for additional training opportunities that are easy to access at anytime, anywhere. Online courses are one hour in length, each on a specific ESD topic pertinent to today's industry. A listing of archived online courses and scheduled live courses are available on the education page of our website. To "provide solutions" for our customers who are in need of in house training materials, the ESDA also offers Computer Delivered Training videos on DVD. There are computer based training options for individual locations or enterprise wide applications described on the ESDA Website.

As we strive to serve the global industry, the ESDA developed the ESD On Campus Lecture Program. Its purpose is to provide students with an insight as to the importance of ESD control, its research, and study. ESD Lectures and presentations have been given at numerous campuses in Asia and in the United States. Our On Campus lecture program has helped to stimulate new research and instructional

programs at many universities we have visited.

The ESDA offers a number of courses and delivery methods to provide convenient and affordable education within our industry. Many of our courses support the ESDA professional certification programs such as the Certified Program Manager and Certified Device Designer programs. The Certified Professional Program Manager program is intended for individuals who are involved in designing, implementing, managing, and auditing ESD control programs in their facilities. The Certified Professional Device Design program was created for device design engineers, to successfully design ESD device protection. Certified professionals are recognized by their companies and customers as experts in the field of ESD control. As one Certified Program Manager offered, it increased his ability to perform factory assessments and because of the certification he obtained more authority within the company and customers. Another Certified Program Manager stated he has found that the program was very valuable and proved to be an asset in contacts with customers. Certified Professional Program Managers are the best qualified to manage the required control programs for their companies

to become ESD facility certified. Many facilities are being requested by their customers to become certified to ANSI/ESD S20.20-2007 and IEC 61340-5-1. There are now over 172 Certified Facilities with more being certified all the time.

I hope you agree that our business units and committees work hard to answer the call of becoming the recognized global leader serving industry in the field of electrostatic mitigation.

Donn & Billmore



*Donn,
As ESDA President you should be glad to hear that by the virtue of my carrying ESDA backpack during my recent trip to Antarctica I was able to establish local ESDA chapters among the natives on the distant islands.
A letter recently recieved from Vladimir Kraz, ESDA Volunteer*

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Question and Answer

HiPot Test and ESD Mats

Q We have a HiPot test station set-up on an ESD worksurface. We are experiencing breakdowns in some of our Hall effect sensors due to a high inrush voltage measured with a scope. Hooking the ground to the body of this particular black anodized motor casing and the positive lead of the HiPot to the motor A,B,C windings (which we twist together for the test) we then apply 500 volts AC. Intermittently we get a surge of voltage which we believe is damaging the hall sensors. We have placed the device under test on an insulated platform and they pass the test but breakdown when on the ESD mat.

I have contacted numerous HiPot Manufacturers and talked with their engineers and they are telling me not to test on the ESD mat, because the ESD mat is conductive. They are recommending we use an isolated platform for the test.

Here is my question, if we are to have a truly ESD safe area, would we not be defeating the purpose of the ESD safe workstation theory to have an isolated area to do this Hi-Pot test?

A Thank you for your important question. HiPot testing is one of the areas where personal safety has to take precedence over ESD control. The other people you have talked to have given you correct information. It is NOT recommended to use ESD control materials in or around these types of test areas where personnel may be exposed to open voltage sources. The other aspect of having a dissipative or conductive mat in the area is the problem you have experienced. The resistive coupling between the tester and the product under test through a ground plane (formed by the ESD control mat) is

setting up for current flow through the product under test. That is most likely why you are seeing failures.

You need to provide ESD protection for the product going into the test up to the point where you make the connections for the HiPot test. For circuit boards this may mean shunts across the edge connector, shielding bags for transport etc. Often personnel will be grounded while setting up the test but when the test is actually being conducted, they should be disconnected from ground for safety purposes.

The response given is a service to industry; the ESDA is not responsible for content.

The users of this information need to determine the suitability of the response.

Association News

SMTA Paper Exchange

The top two papers presented at the annual EOS/ESD Symposium are considered for presentation at the SMTA International conference. The SMTA has selected the 2010 Symposium Outstanding Paper, to be presented at the SMTA 2011

event that is being held October 16-20 2011 in Fort Worth, TX.

The ESDA will choose one of the top two papers from the SMTA best papers to be presented at this year's 2011 EOS /ESD Symposium

Register Online!

Registration for select Tutorials are now available online!



Look for this button at www.esda.org

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Volunteer Warren Anderson, “establishing a good rapport!”



Warren Anderson is currently a Fellow at AMD’s Boston Design Center, where he works on high-speed I/O and electrostatic discharge (ESD) protection design. Warren leads a team designing I/O and ESD circuits and developing technology for high-speed off-chip signaling on AMD’s microprocessors.

Prior to joining AMD, Warren worked for Intel in Hudson, MA where he managed a team developing the specifications for advanced link signaling technologies. Prior to Intel, he worked for Hewlett Packard and Compaq Computer as part of the Alpha Development Group. While at HP and Compaq, he designed the ESD protection for all Alpha products. He also led the I/O design team for the Alpha EV79 microprocessor, designed the Rambus I/O interface for the Alpha EV7 microprocessor, and worked on the production debug of the EV6, EV7, and EV79 I/O. From 1993 to 1998, he worked in the Advanced Semiconductor Technology Development group at Digital Equipment Corporation,

where he was responsible for ESD and latch up protection design on all of the company’s semiconductor products.

Warren’s areas of expertise include I/O circuit design, I/O jitter modeling and performance prediction, ESD protection, and signal integrity. His publications include numerous papers on ESD protection design as well as contributions to three books: the second edition of ESD in Silicon Integrated Circuits and chapters on I/O and ESD design in the books Design of High-Performance Microprocessor Circuits and High Performance Energy Efficient Microprocessor Design. His conference publications include three ISSCC presentations describing Alpha microprocessors and several papers on ESD design at the ESD Symposium. He has delivered

lectures on ESD and I/O circuit design through the University of California Berkeley Extension and the ESD Symposium tutorials. Warren holds 11 patents on ESD protection devices, circuits, and I/O design techniques.

Warren told us of another ESD related accomplishment that he is very proud of, the creation of the troubleshooting ESD failures tutorial. Participants have to apply the knowledge that they gained in other tutorials to find the root cause of actual ESD qualification failures, most of which, unfortunately, come from first-hand experience. “I wanted the format for the tutorial to be interactive, with participants exchanging ideas for what the source of the real problem could be with each other. The actual failures took several weeks to debug, but we would only have about 15



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ESDA Spotlight *continued*

Warren Anderson continued

min. to work through each one in the classroom, so it was a challenge to get the mix of background information correct so that there was enough to allow participants to figure out the solution while not giving it away." This tutorial, run by Hans Kunz, is now one of the core device design tutorials at the workshop.

From 2000 to 2006, Warren was a co-instructor for the University of California, Berkeley extension course on ESD in integrated circuits.

As an ESDA volunteer, Warren has been involved in the Symposium technical program committee, a tutorial instructor, on the IEW management committee, and is the 2011 IEW management committee chair.

"Serving on a technical program committee is a great way for me to keep abreast of the latest findings and research on component level ESD protection design. Interactions through TPC and workshop committee meetings have connected me with other ESD engineers, establishing a good rapport and leading to informative discussions on a variety of topics." Warren said.

Warren received his Ph.D. in 1993 in applied physics from Yale University for research on low-temperature measurements of MOS transistor properties. He received a B.A. in physics from Carleton College, Northfield, MN and a M.S. in applied physics from Yale University.

Warren lives in Boxborough, MA, with his wife Janet, and their children, Elizabeth and Ben.

The Anderson family shares a common interest in music. Both kids play the violin. Although they take formal lessons in classical music, they really enjoy Scottish fiddling. They have won awards at the New England Regional Scottish Fiddle competition. Warren plays the trumpet and runs a 10 piece amateur jazz group, doing some composing and arranging as time allows. The family also enjoys the outdoors. Janet leads a Girl Scout troop and Warren is involved in the leadership of a Boy Scout troop.

Association News

RCJ Paper Exchange

Each year the ESD Association and the Reliability Center for Electronic Components of Japan (RCJ) exchange best papers from each of their conferences

The Best Paper from the EOS/ESD Symposium is presented at the RCJ ESD Symposium in Japan, while ESDA invites the RCJ Best paper to present at the EOS/ESD Symposium.

The 2009 Best Paper Award

"Characterization and Simulation of Real-World Cable Discharge Events" *By Wolfgang Stadler, Tilo Brodbeck, Josef Niemesheim, Reinhold Gaertner, Infineon Technologies; Kathleen Muhonen, Penn State Erie, The Behrend College*, was presented at the RCJ conference in Japan in October 2010 by Tilo Brodbeck of Infineon Technologies.



Tilo Brodbeck left, Professor Kimura Right

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Education

Texas Regional Tutorial

March 1-2, 2011

3M Innovation Center
Austin, Texas 78726

ESD Basics for the Program Manager

March 1, 8:30 a.m. - 4:30 p.m.

Ted Dangelmayer & Terry Welsher, Dangelmayer Associates LLC

This tutorial provides the foundation material for understanding electrostatics and ESD and their role in the manufacture and handling of ESD sensitive devices. The fundamental properties of charge, electric fields, voltage, capacitance and current are discussed with a view towards understanding key electrostatic phenomena and electrical processes.

How To's of In-Plant ESD Survey and Evaluation Measurements

March 2, 8:30 a.m. - 4:30 p.m.

Ted Dangelmayer, Dangelmayer Associates LLC; Carl Newberg, MicroStat Laboratories, Dangelmayer Associates LLC

The attendee will learn not only how to make valid auditing measurements in accordance with ESD TR53 – Compliance Verification of ESD Protective Equipment and Materials, but also how to recognize and avoid common pitfalls.

ESD On-Chip Protection in Advanced Technologies

March 2, 8:30 a.m. - 4:30 p.m.

Charvaka Duvvury, Texas Instruments, Inc.

This tutorial addresses the important issues for the design of IC protection circuits built with advanced deep sub-micron CMOS technologies, including high voltage MOSFETs for analog applications. This tutorial will present fundamental aspects of ESD protection design such as basic NMOS and SCR concepts, gate-biased and substrate-driven NMOS protection techniques, as well as some new advanced low capacitance and high speed protection devices.

Register Online At <http://esda.org/onlineregistrations.html>

SiVa Regional Tutorial

March 23-24, 2011

AMD Commons Building,
Sunnyvale, CA

Electrostatic Calculations for the Program Manager and the ESD Engineer

8:30 a.m. - 12:00 p.m.

Leo G. Henry PhD, ESD/TLP Consultants, LLC

This tutorial focuses on the basic calculations and techniques of use to the Program Manager and the ESD engineer. The content is at the introductory college pre-calculus and introductory college physics level set in the context of electrostatic discharge and its effects. It is suggested that the student gain some familiarity with these subjects prior to the tutorial.

ESD Standards Overview for the Program Manager

1:00 p.m. - 4:30 p.m.

David E. Swenson, Affinity Static Control Consulting, LLC

This Standards Tutorial provides an overview of all the ESD Association and other relevant industry and military Standards, grouped into common test types based on measurement probe and test instruments. A common methodology is used in this tutorial to cover the requirements, applications and specifications for each Standard and Standard Test Method.

System Level ESD/EMI: Testing to IEC and Other Standards

8:30 a.m. - 12:00 p.m.

Leo G. Henry PhD, ESD/TLP Consultants, LLC

This tutorial is intended to help those tasked with testing products to IEC and other System Level ESD standards by providing detailed information on IEC 61000-4-2, the most widely used standard, and highlighting the harmonization and differences among IEC, ANSI, Telcordia and some automotive ESD standards.

Ionization Issues and Answers for the Program Manager

1:00 p.m. - 4:30 p.m.

Arnold J. Steinman, MSEE, Electronics Workshop

Air ionization can neutralize the charge on insulated and isolated objects. This seminar will present the information needed to use ionizers to solve problems caused by static charge. It will first examine the problems caused by static charges in a variety of workplaces, and then review the common methods by which static charges are generated and controlled.

Register Online At <http://esda.org/onlineregistrations.html>

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Education

**Northeast Regional Tutorial
May 4-5, 2011**

Teradyne Conference Center, North Reading, MA

MAY 4, 2011

Part I ESD Damage - A Surprisingly Dominant Failure Mechanism!

8:30 a.m. - 10:00 a.m.

Ted Dangelmayer, *Dangelmayer Associates, LLC*

While most companies are acutely aware of the hazards of ESD (electrostatic discharge), few are aware of just how pervasive ESD failures actually are. Recent studies into the misdiagnosis of these failures suggest that ESD damage may, in fact, be the dominant failure mechanism on the factory floor and in the field. This includes all sources of device failure such as EOS, ESD, Contamination, Charged Board Event, Cable Discharge Event, device fabrication etc. You will also learn which are the dominate ESD failure mechanisms among CDM, HBM and MM. Attend this highly interactive tutorial and learn the latest facts about ESD damage and about current best practices for ESD damage prevention.

Part II Electrical Overstress (EOS) in Manufacturing

10:30 a.m. - 4:30 p.m.

Terry Welsher, *Dangelmayer Associates, LLC*

Electrical overstress (EOS) is a major cause of device failure in manufacturing and in the field. Despite this there is relatively little information on the sources of EOS and on prevention practices, particularly for the factory. In this tutorial, the fundamentals of device overstress are reviewed. Relationships among device EOS stressing models are discussed. The causes of EOS and EOS-like events in manufacturing are described and categorized by source and by stress-type. Case histories, including failure analysis and root cause determination, are presented and the few relevant industry specifications are reviewed. An outline for an "EOS control" program similar to ESD control is presented.

Northeast Regional Tutorial Day Two-

MAY 5, 2011

Packaging Principles for the Program Manager

8:30 a.m. - 12:00 p.m.

David E. Swenson, *Affinity Static Control Consulting, LLC*
Shipping electronic parts within a factory, to another factory, distributor, or to an end-user has always been an area of uncertainty within the manufacturing process. To provide clear-cut information on what type of controlled packaging should be used in any situation, the ESD Association released a comprehensive revision of the obsolete industry standard EIA 541-1988. The newer document, ANSI/ESD S541, is the focus of this inclusive session. It provides information and guidance, as well as material specifications, to assist in the design and implementation of a packaging plan for use within an ANSI/ESD S20.20 based ESD Control Program. Current and newly released test method standards suitable for packaging material evaluation will be described. Course credit applies to the ESD Program Manager Certification curriculum. Previous attendance at the "ESD Basics" and "How To's..." tutorials are highly recommended.

Hands-on ESD Test Equipment Workshop: Uses and Pitfalls of ESD Measurements

1:00 p.m. - 4:30 p.m.

Ted Dangelmayer, *Dangelmayer Associates, LLC*

Come join us for this highly interactive hands-on workshop on the proper use of ESD test equipment. Pitfalls of common instruments will be explained as well as the invalid test results that can result. For instance, static locators can yield totally invalid readings when used incorrectly due to voltage suppression. Demonstrations will be used to illustrate both the pitfalls and correct measurement techniques for instruments such as static locators, ionizers, EMI/ESD Event Detectors, and Resistance meters. Find out if static locators can be used accurately to test automation equipment, conveyor belts, document carriers with paper inside, ionizers or rapidly moving operations? Each student will participate in class exercises to perform these tests and to experience the benefits of correct test methods as well as the incorrect results created by the pitfalls. Approximately half of this workshop will be devoted to these hands-on class exercises.

Register Online At <http://esda.org/onlineregistrations.html>

Education

**North Central Regional Tutorial
May 18-19, 2011**

Holiday Inn & Suites, Bloomington, MN

**Seminar 20.20: ESD Program
Development and Assessment
(ANSI/ESD S20.20 Seminar)**

8:00 a.m. - 5:00 p.m. -2 Days

Ron Gibson; John T. Kinnear MSEE, IBM

This seminar provides instruction on designing and implementing an ESD control program based on ANSI/ESD S20.20. The course provides participants with the tools and techniques to prepare for an ESD facility audit. This two-day course is an ESDA certification requirement for in-plant auditors and program managers who are working toward professional ESD certification. The following topics are covered in this course:

- Overview of ANSI/ESD S20.20
- How to approach an assessment
- Administrative elements
- ESD program assessment
- ESD program techniques for different applications
- Technical elements
- Overview of the assessment process
- The audit checklist and follow-up questions

It is recommended that the ESD Program Development and Assessment Seminar be taken after the Certification candidate has taken most of the other Program Manager related tutorials.

Register Online At <http://esda.org/onlineregistrations.html>

ONLINE COURSES

**Grounding in an Electrostatic
Protected Area**

March 15, 2011 • 11:00 a.m. US/Eastern Time

David E. Swenson, Affinity Static Control Consulting, L.L.C

Grounding is perhaps the single most important technical aspect in establishing an electrostatic protected area. The ESD Association standard for grounding, ANSI/ESD S6.1 - Grounding, originally issued in 1991, went through significant revisions in 1999. The document was reaffirmed in 2009 with minor changes.

The ESD Association grounding standard provides potential users with specifications, guidance and suggestions for implementing a grounding/bonding system suitable for nearly any imaginable situation that is related to establishing an electrostatic protected area or EPA. This information is not found anywhere else in industry literature.

ONLINE COURSES *continued*

**Electrostatic Discharge Effects In Integrated
Circuit Technologies**

April 26, 2011 • 11:00 a.m. US/Eastern Time

Charvaka Duvvury Ph.D. Texas Instruments

This course will outline the fundamentals of ESD phenomena and the methods to control the effects of ESD for safe manufacturing of IC devices. The training material will include the nature of ESD transients, their impact on the IC devices, common methods to test for ESD at both the device level and the system board level, and the overall protection techniques. Finally, the course will review the advances in IC technologies that lead to future challenges for ESD development and the resulting important technology roadmap established by the ESD Association.

Air Ionization: Theory and Practice

April 14, 2011 • 1:00 p.m. US/Eastern Time

Arnold Steinman, MSEE, Electronics Workshop

The primary method of static charge control is direct connection to ground for conductors, static dissipative materials, and personnel. But a complete static control program must also deal with isolated conductors, insulating materials, and moving objects that cannot be grounded. Air ionization can neutralize the charge on insulated and isolated objects. This seminar will cover the following topics:

- Importance of Ionization in a Static Control Program
- Ionization Fundamentals and Methods
- Ionizer Selection Criteria and Examples
- ANSI ESD S20.20 Static Control Program Requirements for Ionization

**Register for online courses by visiting
<http://www.esda.org/education.html#ED>
for registration forms**

**For newly scheduled courses check
the education schedule on our
website at
<http://www.esda.org/education.html>**

On-Campus

*Vanderbilt University -
Looking for a Single Event
Upset in Music City*

Dr. Steven H. Voldman

On my first visit to Nashville, Tennessee I knew I was entering a place just a little different. As you enter the airport to the baggage claim, the people movers pass old posters of the Grand Ole Opry and country western singers. Nashville, Tennessee - Music City. Why am I in Nashville Music City? To listen to Hank Williams? No, to visit Vanderbilt University.

Vanderbilt University is a private research university, established by Cornelius Vanderbilt post-Civil War in 1873. Vanderbilt University has more undergraduate students than graduate students, with 12,514 total students, 5,720 graduate students, and is rated as 51st best university in the world! Vanderbilt has a beautiful campus in downtown Nashville with brick architecture. Its courtyards are a living campus arboretum of 300 species of trees. The campus also has a few unusual classical treasures such as a full scale replica of the Parthenon.

Vanderbilt University has one of the largest groups working on radiation and single event upsets in the US – and they are doing research on Single Event Upsets (SEU) causing latchup events – sometimes referred to as Single Event Latchup (SEL). A large research group with many faculty members and a large group of students support this effort. It is integrated with many members of the Institute for Space and Defense Electronics (ISDE). Since latchup lectures and tutorials are more rare than the BBQ ribs in Nashville, a latchup tutorial and ESD lecture was provided for this visit. My host was graduate student Nathaniel



From front to back: Dr. Lloyd Massengill, Director of Engineering at ISDE, Dr. Ron Schrimpf, Director of ISDE, Barry Templeton, Dr. Robert Reed, Daniel Limbrick, Dr. Bharat Bhuvu, Cassandra Hawkins, Becky Borsody, Nick Atkinson, Scooter Ball, Jeff Kaupilla, Nelson Gaspard, Mike McCurdy, Dr. Art Witulski, Nick Pate, Brian Sierawski, Sarah Armstrong, Nathaniel Dodds, Vishwa Ramanchandran, Brian Olson, Daniel Loveless, Pierre Maillard, Michael Clemens, Andrew Sternberg, Nick Hooten, Dr Mike Alles, Matt Gadlage, Jon Ahlbin, Tim Haeflner

Aronson Dodds, whose research is on the SEL events on semiconductor chips. A day tour was arranged with visits to the Dean of Engineering, faculty members, tour of the labs, X-ray lab, proton particle accelerator, a 2-hour latchup tutorial and a 1-hour general talk on the future of ESD, and private conferences with grad students.

Faculty members in this area were Professor Kenneth F. Galloway, Dean of Engineering; Professor Ron D. Schrimpf, Orrin Henry, Professor of Engineering and Director of Institute of Space and Defense Electronics (ISDE); Professor Robert A. Weller, ISDE Fellow; Associate Professor Robert A. Reed, ISDE Fellow; and lastly Professor Bharat L. Bhuvu.

It was a wonderful day of conversation; discussing early days of my pre-ESD career - IBM alpha particle and cosmic ray experience in the early 1980s, to latchup in present advanced foundry technologies, and future collaborative interactions, and of course, foot-

ball. Tennessee football mania was all around with the coming football battle over the weekend. Vanderbilt was playing University of Florida, with faculty of UF arriving to watch the game. Cars and hotels were evident with Florida Gator fans rolling into town, Gator T-shirts, and flags on the cars.

Of course, the Vanderbilt faculty were looking for the Big Single Event Upset – Vanderbilt beating University of Florida. It ended up 55-14 in favor of Florida Gators; as Professor Ron Schrimpf admitted “I like the title of this article. Unfortunately the upset did not happen on the playing field.”

Well, back to the lab to chase SEUs and latchup in semiconductors... a lot easier to control and quantify.

Latchup is alive and well at Vanderbilt University. Maybe even Elvis?

Dr. Steven H. Voldman

ESD on Campus Program

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include EDA tools, ESD for multi-chip packages, the future of analog and mixed-signal designs, and a first-ever factory control seminar discussing the present and future interactions between factory control methods and component ESD withstand levels.

Electronic Design Automation (EDA) Solutions for ESD

Michael Khazhinsky, Silicon Labs

CDM-ESD Protection and Modeling for System in a Package (SiP)

Elyse Rosenbaum, University of Illinois

Implementing ESD Factory Controls to Meet Evolving ESD Component Targets

Carl Newberg, Microstat Laboratories; Kevin Duncan, Seagate Technologies; Julian Montoya, Intel Corporation

The Next Wave of Mixed-Signal Interface Electronics

Boris Murmann, Stanford University

Six discussion groups split into parallel sessions in two evenings form an integral part of our interactive workshop. One or more moderators with extensive expertise on each topic will help to guide the discussion. The actual discussion flow will be at the discretion of the participants in each group. Everyone is encouraged to bring and share relevant data and ideas.

Predictive IC Component Design for System Level ESD

Moderator: Alan Righter, Analog Devices

What Commercial EDA Tools are Proving Useful for IC ESD/LU Design Verification?

Moderators: Harald Gossner, Intel Mobile Communications; Warren Anderson, AMD

Where is the Industry Today in Terms of Adopting the Industry Council Recommendations for ESD Target Levels?

Moderators: Brett Carn, Intel Corporation; David Klein, IDT

What are Reasonable Expectations of Fundamental Device TLP Data from Foundry Fabs?

Moderators: Natarajan Mahadeva Iyer, GLOBALFOUNDRIES, Michael Wu, TSMC; Eugene Worley, Qualcomm

What are the Key Industry Needs from Academia in the Area of ESD/LU Design, Design Verification, and Test?

Moderators: Charvaka Duvvury, Texas Instruments; Elyse Rosenbaum, University of Illinois

Challenges with False Product HBM Fails Due to Tester Waveform Anomalies

Moderator: Scott Ward, Texas Instruments

Finally, the workshop provides an opportunity for special interest

groups (SIGs) to meet. Those SIGs are collaborative working teams focused on achieving specific goals. Some of these groups have been successfully cooperating for several years on important ESD topics – with continued momentum stimulated at the IEW! The formation of SIGs is encouraged as a natural extension of the discussion group topics or from any topic of interest to engineers in search for solutions to common problems.

ESD Electronic Design Automation (EDA)

Coordinator: Michael Khazhinsky, Silicon Labs

Transient Latch-up (TLU)

Coordinator: Wolfgang Stadler, Infineon Technologies

ESD Data Analysis Tools

Coordinators: David Tremouilles, LAAS/CNRS; Dimitri Linten, imec

ESD Parameters for ESD EDA Flow

Coordinator: Harald Gossner, Intel Mobile Communications

2-Pin HBM Testing and Changes to the HBM Standard

Coordinator: Evan Grund, Grund Technical Solutions

The IEW is being held on May 16-19, 2011 at the Stanford Sierra Camp in South Lake Tahoe, CA, USA. Registration information can be found at <http://www.esda.org/iew.html>. The early registration deadline is March 29, 2011. Space is limited, so register early.

Please visit <http://www.esda.org/iew.html> to find full abstracts and speaker biographies.

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Standards

Standards Summary
February 2011 Meeting Series Disneyland Hotel, Anaheim, CA

WG1.0 – Wrist Straps.

- The working group (WG) reviewed and adjudicated comments from the Technical and Administrative Support (TAS) committee on the technical changes made during the five-year review of the work-in-progress (WIP) 1.1 document.
- The document is ready for vote-by-mail (VBM) by the Standards Committee (STDCOM) before the June meeting series.

WG2.0 – Garments.

- The WG reviewed and adjudicated TAS comments on WIP2.1.
- The document is ready for STDCOM VBM before the June meeting series.

WG3.0 – Ionization.

- The WG reviewed and adjudicated TAS comments on WIP3.4.
- The document will be submitted for another STDCOM VBM due to technical changes made from the original VBM comments.
- The WG started the five-year review of STM3.1 and technical changes will be made.

•Steve Heymann has stepped down as WG chair and Kevin Duncan has been appointed as the new WG chair.

WG4.0 – Worksurfaces.

- The WG reviewed and adjudicated TAS comments on WIP4.2.

- A discussion was held about the future of the document – some industry users are using a variation of the procedure.
- The WG discussed a low voltage resistance test and a decision was made to perform initial lab testing. A decision will be made on whether to pursue new work based on the results of the testing and replace the current 4.2 procedure.

WG5.0 – Device Testing.

- The WG discussed revisions to the 2010 ESDA Technology Roadmap. Comments and suggestions have been received from industry users on how to expand the scope of the document. A section may be added on device packaging, device manufacturing, and production equipment.
- A new roadmap will be created for device testing and each device WG chair has been asked to submit five-year goals as to where device testing is going.
- The goal is to have a new roadmap published in January 2012.

Adhoc 5.0 – (CBE) Device Testing.

- A team has been assembled to begin writing a technical report (TR) primer on Charged Board Event (CBE).
- The WG is currently researching current papers that have been published in the industry.



JWG – (HBM) Device Testing.

- The WG reviewed the current status of JWIP-001, which is out for STDCOM VBM and closes March 4.
- A TR is being written as a “user guide” to help explain the changes that were made to ANSI/ESDA/JEDEC JS-001-2010.
- The WG has a goal of publishing the TR prior to the July 2011 release of the standard.
- The WG discussed new short term issues that were not added to the current version and may be submitted for a limited ballot at the end of the year.
- A discussion was held on longer-term changes and improvements that will need to be added to the next revision of the document.

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Standards Summary *continued*

WG5.2 – (MM) Device Testing.

- The WG discussed an action item to combine ANSI/ESD SP5.1.1 and ANSI/ESD SP5.1.2 into the revision and re-designation of ANSI/ESD S5.2 to a standard practice. A decision was made to NOT combine the documents into the current MM document; instead, two new documents with MM only will be published.

- WIP5.2 is ready to be reviewed by TAS.

- A bulletin explaining why S5.2 was re-designated will be published on the website.

JWG – (CDM) Device Testing.

- The WG reviewed activities that took place between meetings. 3 GHz data from three sites has been completed and a sixth round robin site has been added.

- 3 GHz round robin data comparing the JEDEC test head with a 10 ohm test head is still being gathered.

- An IC device round robin for CDM pass / fail level testing has begun.

- A generic term of CCDM (contact CDM) was chosen to describe CDM2.

- Tim Maloney gave a presentation on wafer level contact CDM analysis of TSV.

- John Barth gave a presentation on sparkless CDM testing considerations.

- Alan Righter gave a presentation on initial data from ADI Wilmington Orion tester.

- Marti Farris gave a presentation on initial characterization of devices using Thermo Fisher CDM2 tester.

- Gene Worley gave a presentation on design / modeling of apparatus for evaluating CDM test head frequency response with a network analyzer.

- The WG discussed the status of the joint document and a draft is due to TAS in August 2011.

WG5.4 – (TLU) Device Testing.

- The WG reviewed the status of the re-designation of ANSI/ESD SP5.4 to a TR. The document will be submitted to TAS for review between meeting series.

- The WG discussed the status of a new TR that is being written as a base for a future standard. The WG is planning to submit the document to TAS following the September meeting series.

- Wolfgang Stadler will be leading a SIG on TLU at the 2011 IEW. The outline of the new TR will be discussed for further input.

WG5.5 – (TLP) Device Testing.

- Tim Maloney gave a presentation on transient phenomena and TLP.

- Robert Ashton gave a presentation on time dependent TLP measurements including device heating, SCR turn-on, and transient voltage suppression (TVS) devices.

- Jon Barth gave a presentation on VF-TLP verification element.

- A suggestion was made that a TR be written on data extraction.

- The round robin has concluded on ANSI/ESD SP5.5.2 and a TR will be written between meeting series.

WG5.6 – (HMM) Device Testing.

- A round robin is in progress and discussions are being held with statistician Tim Prass regarding some of the test data.

- A discussion was held regarding the possible submission of an abstract to the Technical Program Committee for an invited paper at the 2011 Symposium. The proposed paper would discuss the variability in results which can be expected due to gun waveform variability.

- A presentation was given by Theo Smedes on the differences of testing between the IEC and ESDA documents, along with lab-to-lab data.

- Nate Peachey stepped down as WG chair and Kathy Muhonen was appointed as the new WG chair.

WG7.0 – Flooring.

- The WG reviewed and adjudicated TAS comments on WIP7.1 and TR7.0.

- The WG reviewed and commented on proposed changes to JEC 4.1 and 4.5 at the request of a WG member representing Switzerland.

WG9.0 – Footwear and WG 97.0 – Footwear Systems.

- The WG reviewed and adjudicated TAS comments on the technical changes made during the five-year review of WIP97.1 and WIP97.2.

- The documents are ready for STDCOM VBM before the June meeting series.

- The WG discussed the status of WIP9.1 and decided to add a footwear system test.

Continued on page 14

Standards

Standards Summary *continued*

WG10.0 – Handlers.

- The WG reviewed WIP10.2 along with recent discharge test data from Arnie Steinman and Vladimir Kraz's discharge test data from 2008.
- Alan Richter is going to send three different package types, along with respective waveforms and charge voltage information, for the WG to complete testing using discharge current targets and antennas for correlation purposes.
- A request has been made by a University of Michigan professor to make a presentation showing latest improvements to long range static charge sensor. The WG recommended that a booth be set up at Symposium again.

WG11.0 – Packaging.

- The WG reviewed round robin data for WIP11.14. If the insulative material is removed from the data, the repeatability looks good.
- The document will be sent for TAS review before the June meeting series.
- WIP11.13 is in STDCOM VBM and closes on February 25.
- The WG reviewed ANSI/ESD STM11.11 and ANSI/ESD STM11.31 for five-year review and no technical changes are expected. The documents will be submitted after the June meetings.

WG12.0 – Seating.

- The WG reviewed comments submitted by five industry users of chairs and technical changes were made.
- The document will be submitted to TAS for review.

WG13.0 – Handtools.

- The WG completed adjudication of STDCOM VBM comments and some technical changes were made.
- Another STDCOM VBM will take place before the June meeting series.
- A discussion will be held on whether to keep the limits in the document and re-designate the document as a standard (S) or move the limits to ANSI/ESD S20.20 and keep the document as a standard test method (STM).
- A presentation was given by Gene Chase on the free space capacitance of hand tools.
- The June 2011 meeting will be primarily focused on non-AC powered hand tools.

WG14.0 – System Level ESD.

- The WG reviewed and adjudicated TAS comments on WIP14.1.
- The document is ready for STDCOM VBM between meeting series.
- Karen Shrier gave a presentation on total ESD solution – device level / PCB level and final assembly protection methods.
- Fabrice Caignet gave a presentation on system level ESD modeling techniques incorporating IBIS models.
- A discussion was held regarding creating an SP versus a TR for EMC scanning.
- The WG reviewed the status of WIP14.4 and will submit the document to TAS between meeting series.
- A round robin was discussed and will hopefully be completed by the June meeting series.

WG15.0 – Gloves.

- The WG started reviewing and adjudicating STDCOM VBM comments.
- The WG plans to finish between meetings.

WG17.0 – Process Assessment.

- The WG wrote the foreword to a future document.
- The WG will be working on the HBM section between meeting series.

WG20.20 – ESD Control Program

- The WG held an organization meeting to begin the five-year review of ANSI/ESD S20.20.
- The discussion included the unique constraints that this revision must take into account including facility certification and continued harmonization with other standards – IEC 61340-5-1 and newly revised JEDEC 625B.
- Technical changes will be made and there is a target date of February 2012 for the release of a draft standard.
- LinkedIn is being used to generate industry input on prospective changes. The WG is being tasked with responding to all LinkedIn comments at the conclusion of the review.

WG53 – Compliance Verification

- The WG reviewed and adjudicated TAS comments on TR53.
- The WG focused on adding missing steps that were identified during the TAS review.

Tech Talk

ESDA/JEDEC HBM standard

The first joint ESDA/JEDEC HBM standard was issued in 2010 with the primary goal to merge two separate but similar standard methods. This was the first step in a two-step process. It was entirely focused on harmonizing differences between the existing ESDA and JEDEC methods and did not address new methodologies or next generation issues. These issues are addressed in the proposed 2011 revision. The purpose of this article is to summarize the most important changes in this revision and the motivation for implementing them.

This revision was made in response to well-documented critical issues which are intrinsic to the relay-matrix HBM testers. When these machines were first introduced over twenty years ago, these issues were not a large problem because devices had relatively low pin count and were considerably less complex. This action is being taken now because device scaling and complexity have brought the industry to the point where the shortcomings of the original test method are having serious effects on test accuracy, productivity and cost, and causing ever increasing testing times. Thousands of ESD pulses are now applied to a single IC component. This would not be seen in any real world ESD environment and it has been shown to induce a premature wearout failure mechanism (such as threshold shifts due to accumulative charge trapping in gate oxides). Test times have significantly increased due to the continued growth in pin count (see Figure 1) and the number of independent power supplies (see Figure 2), as IC

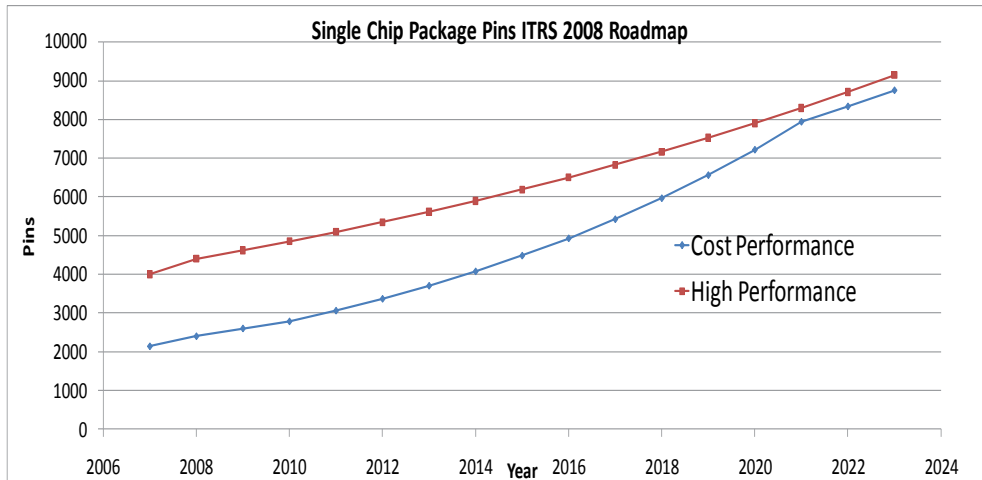


Figure 1: Data from 2008 International Technology Roadmap for Semiconductors (ITRS).

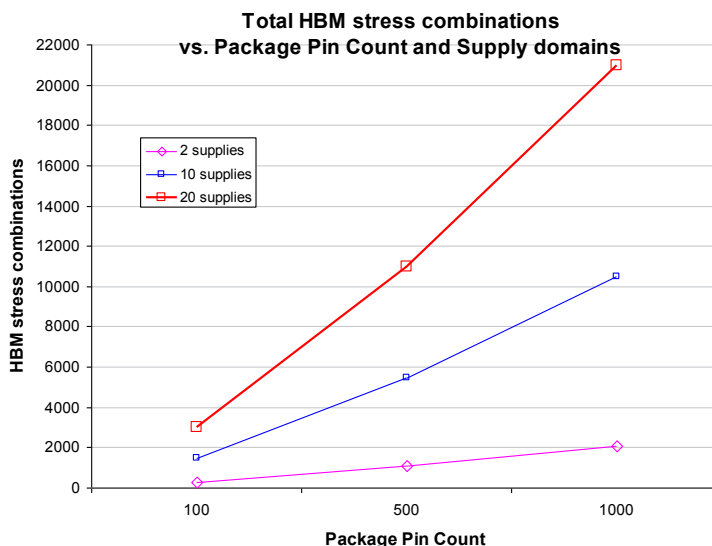


Figure 2: The total number of HBM stress combinations increases by 10X as the number of supply pin groups increase from 2 to 20 supplies.

components increase in their functionality due to the growth in system-on-a-chip (SOC) and multi-chip packages (MCP). The uncontrolled (parasitic) interaction between ICs and testers have increased due to the continued technology scaling, the decrease in power supply voltages, and the complexity of high pin count HBM test equipment. The IC-tester interactions can produce false device failures causing improper

ESD sensitivity classifications. Significant changes to the existing HBM test method are therefore clearly needed to address the HBM testing challenges of modern ICs.

The changes in the 2011 version will be very effective in addressing the most critical problems. However, in the case of IC designs that are not yet on the leading edge of scale and complexity, users may choose not to change their

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test methods in the immediate time frame. Also, the new methods will require some changes to procedures that have become automated and familiar. Adjustments will be needed in device information provided by designers to the personnel executing the tests and new means for generating stress test programs will evolve. Given these transition issues, the 2011 version allows either method to be used. As the industry becomes accustomed to the new methods, it is anticipated that they will gain wider adoption. It should also be noted that there have been no significant changes to the actual stressing method. The current waveform definition and the procedures for verifying compliance remain the same.

To provide a better HBM test method the updated standard has made changes in the following areas:

1. Reduce the HBM test time and premature HBM wearout failure mechanisms by changing the total number of stress pin combinations by:

- a. Simplifying I/O-to-I/O pin combination to a reduced set of pin combinations.
- b. Removing stressing of I/O pins to power supplies that are outside their functional local power domain.

2. Add options to decrease the parasitic interaction of the IC package device under test (DUT) with the HBM tester by:

- a. Enabling the two-pin automated tester option.
- b. Applying pulses of a single polarity for supply pin-to-supply pin testing.

The four major changes made in the JS-001-2011 revision are described below:

1) Most non-supply to non-supply (I/O-to-I/O) eliminated - testing is limited to differential pairs

The existing HBM pin combination I/O-to-I/O (2010 Version, Table 2, row N+1) applies HBM stresses to each I/O pin on terminal A and groups together all of the other I/O pins to terminal B and grounds those pins.

This pin combination has the following drawbacks:

1. Represents a small fraction (<1%) of all possible I/O-to-I/O pin combinations for package with > 100 pins.
2. Was introduced as a compromise due to the excessive test time required to stress all possible I/O-to-I/O pin combinations.
3. Does not represent any possible real ESD situation as the simultaneous grounding of all I/Os in the test or assembly areas is unrealistic.
4. Is redundant to the I/O to supply pin group combinations in most cases.
5. Few failures are found with I/O-to-I/O testing that aren't identified with I/O to power rail testing (and these are mostly identified with differential pairs)
6. May not detect weak ESD paths between I/O pin pairs because the one-to-many I/O test has so many additional paths possibly allowing current to avoid the weak pairs.
7. May lead to false failures in a few cases [1].

This change has a precedent. I/O-to-I/O stress requirements were removed from the JEITA HBM standard, EIAJ ED-4701/300-2, in 2001 and there have been no problems associated

with this change. However, there are known and understood I/O-to-I/O failures possible in some device designs, therefore the JS-001-2011 standard retains the I/O-to-I/O testing for those cases, which include differential pairs. A test targeted towards these pin pairs is expected to provide better information and will likely reduce test time for the IC device.

2) Eliminating "Cross-Domain" testing of non-supply (I/O) pins

Many devices have multiple supplies organized in sets or domains that power different sections of the IC. The typical ESD current paths from an I/O (non-supply) pin to power groups outside its local power domains is from the I/O pin to power rail(s) of its local domain through its power-ground clamp and then between the ground diodes to the different supply domains. As the HBM stress currents repeatedly flow through this current path cumulative stresses can occur on any cross-domain CMOS logic gate that interfaces between the different power domains. This cumulative stress can create unrealistic premature wearout mechanisms due to trapped charge or Vt shifts [2].

In JS-001-2011, this unwanted cumulative stress is greatly reduced. This "cross-domain" stressing is eliminated by requiring that signal pins are stressed only to their associated local supply pin groups. Then, all of the supply pins of each group are stressed to all of the other supply pin groups (as is also done in the current method). Thus the current paths from any I/O pin to any power pin are tested in two steps. This change significantly reduces the total number of pin combinations re-

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quired to test a device, thereby saving significant HBM test time and it also eliminates the cross domain wearout failure mechanism. To take advantage of this new set of pin combinations, additional information is needed to make the association of non-supply pins to their local supply groups.

3) Pin Combinations for Two-Pin Testing

The simplest and most realistic HBM test is to stress all two-pin combinations. Relay-based HBM testers have been engineered to test pins in the one-to-many combinations using relay switching to reduce the total number of combinations required. However, the unintended parasitics of this tester configuration have been shown to affect test results, especially with shrinking device geometries [3]. Issues regarding false failures from these testers for certain device types have been published [4].

The proposed revision (JS-001-2011) simply permits the existing one-to-many pin combination sets to be divided into one-to-one sets so that all devices can be stressed in two-pin combinations. This is an especially important option as it is suspected that tester parasitics produce false failures [Section 6.6 of JS-001-2010].

4) Using “Single Polarity” supply-to-supply stressing

This change addresses problems that occur due to the parasitic relay matrix capacitance of unselected pins. It also removes some redundant pin combinations. We address the redundancy first. When HBM stress is performed between device supplies, each sup-

ply pin is tested to all other supply pin groups. This means that each pin of supply A is tested to supply pin group B and also each pin of supply B is tested to supply pin group A. The redundancy of testing both A to B and B to A with both polarities can be eliminated by testing pins in both directions with a single polarity. Stressing with positive pulses from A to B and from B to A uses ESD current paths similar to stressing from A to B with both positive and negative pulses and also B to A with both polarities. The option for using a single (either positive or negative) polarity allows the stress program to minimize the impact of the interaction between the device and the tester parasitics [3,4,5]. The polarity can be selected to avoid forward biasing the diode clamps that connect voltage rails to I/O pins, and thereby can reduce the amount of the stress current that flows into tester parasitic capacitances. For most technologies the selection of positive polarity stress has proven to be the correct choice. Reducing the DUT-tester interactions allows most of the current that flows from the tester’s Terminal A to be returned through Terminal B, more closely simulating a real event and properly activating the ESD protection circuitry.

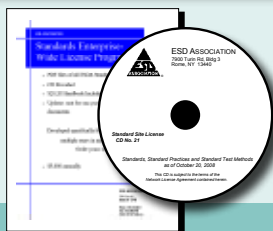
Conclusion

Any change to a test standard, even when that change increases accuracy, may produce differences in the test results for some IC devices. The changes introduced in this revision are optional but preferred; IC devices that were previously classified by the JS-001-2010 may continue to use that classification. Many, but not all, devices will have

the same classification when tested according to JS-001-2010 or JS-001-2011. For the devices that exhibit different classifications, the classification using the improved pin combinations of JS-001-2011 should be used.

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The meeting will begin with a check-in from 4:00 to 4:30 PM. Dinner will be served at 5:00, and the technical presentation will begin at approximately 6:00 PM.

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5/4
5/5

- General Mtg. Factory Tour or a Guest Speaker
- RTP Pt.1 ESD Damage-Ted Dangelmayer + Pt. 2 EOS in Mfg- T.Welsher
- RTP Packaging for PM-D. Swenson + EST Test Eqpt. Worksp - Ted D

SiVa Silicon Valley: Est. 40 Members

3/23
3/24
4/20

- RTP: ESD Calculations and Ionization for Program Mgr.
- RTP: Packaging Principles, System Level IED-ESD Test
- SiVa Local Chapter members meeting

North Central Chapter

3/14
5/18

- Annual Membership Meeting and Dinner
- 5/18>19 RTP Course S20.20

Philippines Chapter

March
6/6

- Monthly General Member Mtgs with Tech Learn Session
- iNARTE Exam, Manila
- Philippines ESD Forum

Symposium

33RD ANNUAL EOS/ESD SYMPOSIUM TUTORIALS & EXHIBITS

September 11-16, 2011 Disneyland Hotel, Anaheim, CA



NEW Demo Day!
Exhibitors will
highlight their products
and services!

Over 40
Tutorials with 12
New or Revised
classes!

Technical Sessions

Education ... The Symposium starts with a set of academic and professional certification Tutorials on Sunday and Monday, then continues on Thursday. All tutorial content was renewed by our distinguished instructors to reflect the latest research and application developments in the past year. **12 new or revised Tutorials will be offered in 2011**

Science ... The Technical Program will span Tuesday to Thursday with outstanding talks presenting on many hot topics related to the phenomena of static electricity, applications, and control methods.

Industry Exhibitors



Workshops

Industry Exhibits ... Generating new research challenges and offering new ESD products and services, our colleagues from many companies will be happy to meet you in the Exhibit Hall, starting with the Welcome Reception on Monday evening till the exhibits close on Wednesday afternoon. Use this unique opportunity to find the ESD product or service you have been looking for during the year or just talk to the professionals with hands-on experience on static control methods, evaluation techniques, ESD hardware and many other ESD business matters.

Workshops ... A place to share professional issues and experiences, find solutions or openly discuss ideas with supporters or critics. The program of workshops on Tuesday and Wednesday afternoon will provide you the forums to talk and comment, receive feedback and learn from colleagues in a 'no necktie' environment. **2011 will offer a new workshop format with no formal panel. Come to the workshops with enthusiasm and get working on your ESD issues!**

2011 will host a new DEMO Day for Exhibitors to share their products and services.

Calendar of Events

March 1-2, 2011

Texas Regional Tutorial
ESD Basics for the Program manager
• How To's of In-Plant ESD Survey and
Evaluation Measurements • ESD On-Chip
Protection in Advanced Technologies
3M Innovation Center, Austin, TX
<http://esda.org/onlineregistrations.html>

March 14, 2011

North Central Chapter Annual Membership
Meeting And Dinner
Crowne Plaza, Appletree Square
Bloomington, MN

March 15, 2011

Grounding in an Electrostatic Area
Online course
[http://www.esda.org/documents/
Grounding3-2011.pdf](http://www.esda.org/documents/grounding3-2011.pdf)

March 23-24, 2011

SiVa RTP
Calculations • ESD Standards Overview
for the Program Manager • System Level
ESD/EMI: Testing to IEC and Other
Standards • Ionization and Answers for
the Program Manager
AMD Commons Building, 991 Stewart
Drive Sunnyvale CA
<http://esda.org/onlineregistrations.html>

March 23, 2011

Northeast Local Chapter Meeting

April 6-7, 2011

Electronics New England
Boston Convention & Exhibition Center
Boston, MA
www.Electronics-NE.com

April 10-14, 2011

Electrostatics 2011 - 13th International
Conference on Electrostatics, Bangor
University, Wales, UK
www.electrostatics2011.org

April 14, 2011

Air Ionization: Issues and Answers
Online course
[http://www.esda.org/documents/
Airionization4-14-2011.pdf](http://www.esda.org/documents/Airionization4-14-2011.pdf)

April, 20th, 2011

SiVa Local Chapter members Meeting
for Technical Presentation information go to
www.esdiscovery.com

April 26, 2011

ESD Effects
Online course
[http://www.esda.org/documents/
ESDEffects4-26-2011.pdf](http://www.esda.org/documents/ESDEffects4-26-2011.pdf)

May 4-5, 2011

Northeast Local Chapter RTP
ESD Damage - the Surprisingly Dominant
Failure Mechanism • Sources of and
Protection from Electrical Overstress
(EOS) in Manufacturing and Test •
Packaging • ESD Test Equipment
Workshop: Uses and Pitfalls of ESD
Measurements
<http://esda.org/onlineregistrations.html>

May 16-19, 2011

5th Annual International Electrostatic
Discharge Workshop (IEW)
Stanford Sierra Conference Center, Lake
Tahoe, CA

May 18-19, 2011

NC RTP
ESD Program Development &
Assessment (ANSI/ESD S20.20 Seminar)
Holiday Inn & Suites Bloomington, MN
<http://esda.org/onlineregistrations.html>

June 7-12, 2011

ESD Association Meeting Series,
Sheraton Mission Valley San Diego
Hotel, San Diego, CA

June 13-14, 2011

ESDA Essentials for Device Design
Sheraton Mission Valley San Diego
Hotel, San Diego, CA

June 14-16, 2011

2011 Annual Meeting of the
Electrostatics Society of America
Case Western Reserve University,
Cleveland, OH, USA
<http://www.electrostatics.org/conferences>

September 8-11, 2011

ESD Association Meeting Series,
Disneyland Hotel, Anaheim, CA

September 11-16, 2011

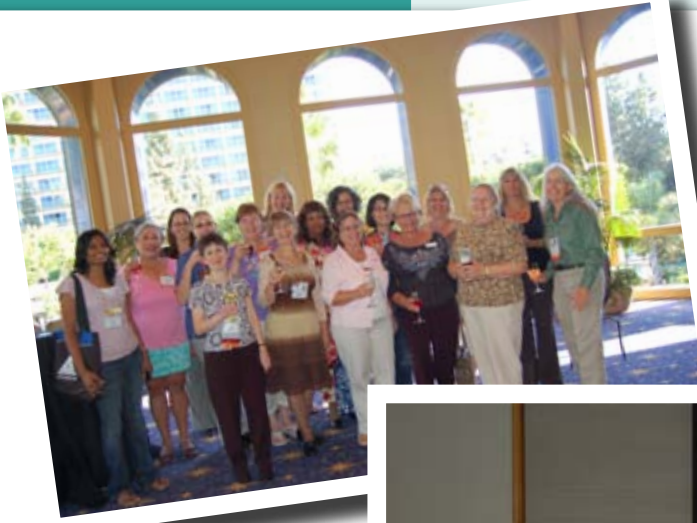
EOS/ESD Symposium and Tutorials,
Disneyland Hotel, Anaheim, CA



For a complete selection of ESD publications and products from Standards and Technical Reports to Training videos download our latest press order catalog at:

<http://www.esda.org/documents/PressCatalog.pdf>

Photo Corner



Womens reception from Disney's 2009 Symposium



A Disney moment!



*A magic show for the BoD!
Courtesy of Brennan Pimpinella*

Editorial Deadlines

Threshold™ is published six times a year by the ESD Association, a not-for-profit corporation. It strives for the advancement of theory and practice of electrical overstress avoidance and of allied arts and sciences and the maintenance of a high professional standing among its members and others.

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Threshold™ Publication Schedule

Issue	Deadlines
January/February	Nov. 19
March/April	Feb. 1
May/June	April 1
July/August	June 1
September/October	Aug. 1
November/December	Oct. 1

Threshold Institutional Listings

Space in the Threshold Institutional Listings, which appear at the bottom of newsletter pages, can be purchased for \$600.00 for six consecutive issues. Listings will also appear in the online calendar. Larger contributions are welcome. No agency fee is granted for soliciting such contributions. Inquiries, or contributions made payable to the ESD Association, should be sent to:
ESD Association, 7900 Turin Rd., Bldg. 3, Rome, NY 13440-2069 Tel: (315) 339-6937, Fax: (315) 339-6793, e-mail: info@esda.org.

Newsletter Staff

Editor

Terry Finn
ESD Association
7900 Turin Road, Bldg. 3, Rome, NY 13440
Tel: 315-339-6937 Fax: 315-339-6793
E-mail: info@esda.org

Associate Editors

David E. Swenson
Affinity Static Control Consulting, L.L.C.

Production Design and Test

Steve Voldman
Intersil Corporation

Leo G. Henry
ESD/TLP Consultants, L.L.C.

Technology

Charvaka Duvvury
Texas Instruments

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Additional Editorial Assistance

Marti Farris, Intel Corporation

ESD Association Headquarters Staff

Lisa Pimpinella, Director of Operations
Christina Earl, Standards Program Manager
Terry Finn, Marketing & Communications Program Manager
Karen Macri, Administrator



7900 Turin Road, Bldg. 3, Rome, NY 13440-2069
Tel: (315) 339-6937 • Fax: (315) 339-6793 • E-mail: info@esda.org • Web: www.esda.org