

News bits

ESD Design Seminar

An ESD Design Seminar will be held May 24-25, 2004 at ESD Association headquarters in Rome, NY. For more information, or to obtain a registration form, contact the Association at 315-339-6937 or follow this link: www.esda.org/education.html

Volunteer spotlight

The ESDA has added a new section to the web site highlighting Volunteer Activities. The Volunteer Spotlight will focus each month on a different volunteer and their contributions to the Association. The first spotlight focuses on Larry Burich, Lockheed Martin.

Look for a new Volunteer Spotlight at the beginning of every month at the following link: www.esda.org/csp.html

Exhibit space available

More than 40 exhibitors have already committed to the 2004 EOS/ESD Symposium. There is still space available—call today to reserve yours. For information on exhibiting, contact Association headquarters by phone: 315-339-6937, fax: 315-339-6793 or e-mail: info@esda.org.

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THRESHOLD™

Volume 20, No. 3

May/June 2004

2004 EOS/ESD Symposium

Create a customized Symposium experience

The EOS/ESD Symposium continues to be the best source for ESD information and solutions. Attendees will be able to customize their Symposium experience to concentrate on their specific areas of interest.

To help plan your participation, the Symposium is programmed along three technical tracks: ESD Test, Failure Analysis, and Systems; Factory, Materials, and ESD Control; and Device, Design, and Technology. These tracks serve as guidelines only; you may attend any event or session you wish.

Technical Tracks

Track 1
ESD Test, Failure Analysis,
and Systems

If you need to understand failure models, troubleshoot ESD failures, test for or evaluate component ESD susceptibility, or develop systems or protection schemes, you will find the following tutorials, techni-

Continued on page 2

EOS/ESD Symposium and Exhibits Program and Schedule Summary

September 19-23, 2004

Gaylord Texan Resort and Conference Center, Grapevine (Dallas), TX
(Program Subject to Change)

Sunday, September 19

Registration Opens
Standards Meetings
ANSI/ESD S20.20 Seminar, Part 1
Tutorials

Monday, September 20

Registration
ANSI/ESD S20.20 Seminar, Part 2
Tutorials
Welcome Reception (Exhibit Hall)
Exhibits Open (p.m. only)

Tuesday, September 21

Registration
Awards Breakfast
Plenary Session, *The Evolution of Failure Analysis to Keep up with the Semiconductor Industry*
Exhibits

Tuesday, September 21 (continued)

Technical Sessions
Professional and Technical Women's Reception

Wednesday, September 22

Registration
Technical Sessions
Association Luncheon & Annual Meeting
Exhibits
Workshops

Thursday, September 23

Registration
Technical Sessions
Tutorials

Friday, September 24

ESDC Technician Exam
ESDC Engineer Exam

Symposium

Continued from page 1

Create a customized Symposium experience

cal sessions and workshops to be of special interest:

Tutorials

- System Level ESD/EMI-Part 1: Principles, Design Troubleshooting and Demonstrations (Sunday)
- System Level ESD/EMI-Part 2: Testing to IEC and Other Standards (Sunday)
- EOS/ESD Failure Models and Mechanisms (Monday)
- Device Testing-Component Level-HBM, CDM, MM & TLP (Monday)
- Electrostatic Calculations for the ESD Engineer (Thursday)
- Design of TLP-Systems and Applications of the Very-Fast TLP (Thursday)
- Transmission Line Pulse Measurements: Parametric Analyzer for ESD On-Chip Protection (Thursday)

Technical Sessions

- Plenary Session—The Evolution of Failure Analysis to Keep up with the

- Semiconductor Industry (Tuesday)
- System Level and Other ESD Issues (Tuesday)
- Characterization of On-Chip Protection (Wednesday)
- Novel TLP Testers (Thursday)

Workshops

- Can TLP Go Beyond HBM & CDM? (Wednesday)
- HBM-TLP Testing Miscorrelation: Experiences, Explanations, Solutions (Wednesday)

Track 2

Factory, Materials, and ESD Control

Targeted to those responsible for the factory floor, standards, material selection, or ESD program management, this track offers sessions and activities specially focused on providing the information and resources needed to address and solve ESD problems. Choose from tutorials,

technical sessions, and workshops such as the following:

Tutorials

- ESD Basics for the Program Manager (Sunday)
- Air Ionization: Issues and Answers (Monday)
- How To's of In-Plant ESD Survey and Evaluation Measurements (Monday)
- Packaging Principles for the Program Manager (Monday)
- ESD Handling and Tool Design Practices for Extremely Sensitive ESD Devices (Monday)
- ESD Standards Basics for EPA (Thursday)
- CleanRoom Considerations for the Program Manager (Thursday)

Technical Sessions

- MR Heads-Processing (Tuesday)
- Factory and Materials (Wednesday)

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List of Exhibitors

As of April 1, 2004

- 3M Electronic & Interconnect Solutions Division
- ACL/Staticide Inc.
- Aesops, Inc.
- Asiatic Fiber Corp.
- Associated/ACC International, Ltd.
- Barth Electronics, Inc.
- Botron Co. Inc.
- Century Container Corporation
- CIBA Specialty Chemicals
- Conductive Containers, Inc.
- Credence Technologies, Inc.
- Desco
- Dou Yee Enterprises
- Electronic Polymers, Inc.
- Electro-Tech Systems, Inc.
- ESD Consultancy Sdn. Bhd.
- ESD TLP Consulting

- Flexco
- H.C. Starck, Inc.
- ION Systems
- ITW-Richmond Technology, Inc.
- Kreha Corporation of America
- Monroe Electronics, Inc.
- Noveon Static Control
- NOVX Corporation
- Oryx Instruments
- Prostat Corporation
- RTP Company
- Sarnoff Corp.
- Simco Static Control & Cleanroom Products
- Static Control Components
- Static Solutions, Inc.
- Statico
- Stephen Halperin & Associates
- Tech Wear Inc.
- Tek Stil Concepts Inc.
- Thermo

- Trek Inc.
- Vidaro Corp.
- Worldstat SRL

Sponsor

ESD Association

Exhibit Hours

- Monday, September 20
7:00 p.m.-10:00 p.m.
- Tuesday, September 21
9:00 a.m.-5:00 p.m.
- Wednesday, September 22
9:00 a.m.-noon, 2:00 p.m.-4:00 p.m.

Information on exhibiting may be obtained by contacting Lisa Pimpinella, ESD Association, 7900 Turin Road, Building 3, Rome, NY 13440, Phone: 315-339-6937, Fax: 315-339-6793, e-mail: info@esda.org.

Symposium

Continued from page 2

Create a customized Symposium experience

Magnetic Recording Heads (Thursday)

Workshops

Automated Equipment, ESD and Grounding Issues (Wednesday)
Common Auditing Issues (Wednesday)
ESD in Cleanrooms (Wednesday)
Ionization Issues (Wednesday)
ESD in Magnetic Recording (Wednesday)

Track 3 Device, Design, and Technology

Advancing and changing technologies continually challenge designers and users of sensitive devices to seek new EOS/ESD solutions. At this year's Symposium,

you can explore the latest research and information on device technologies. Choose from tutorials, technical sessions and workshops such as the following:

Tutorials

ESD On-Chip Protection in Advanced Technologies (Sunday)
On-Chip Electrostatic Discharge Protection in RF Technologies (Monday)
SPICE-Based ESD Protection Design Utilizing Diodes and Active MOSFET Rail Clamp Circuits (Monday)
Circuit Modeling and Simulation for On-Chip Protection (Monday)
Latchup Physics and Design (Monday)
Troubleshooting On-Chip ESD Failures (Thursday)

Device Technology and Failure Analysis Overview (Thursday)

Technical Sessions

RFIC and Novel Protection Devices (Tuesday)
Analysis and Modeling of ESD Design Failures (Tuesday)
On-Chip Protection Strategies, Physics and Modeling (Tuesday)
Tester—Device Effects (Tuesday)
Characterization of On-Chip Protection (Wednesday)

Workshops

Silicon Technology Scaling and ESD Reliability-Roadmap and Reality (Wednesday)

Symposium Registration and Fees

Advance Fees
On or Before
August 6, 2004

On-Site Fees
After
August 6, 2004

Save by registering early

You can save time and money by registering in advance. Advance registration fees are valid only if received no later than **August 6, 2004**. Registrations received after this date will be processed at the on-site fees.

You can save hundreds of dollars by registering early. Attendees who participate in the "Total Symposium Experience" and full-time students will save even more.

To register, use the registration form in the program you will receive in the mail in June, download the form from the ESD Association web site (www.esda.org), or contact ESDA headquarters by phone at 315-339-6937, by fax at 315-339-6793, or by e-mail at info@esda.org.

Symposium

ESD Association Members	\$495	\$695
Non-Members	\$595	\$695

Tutorials

Sunday (Full Day)	\$475	\$550
Monday (Full Day)	\$475	\$550
Thursday (Full Day)	\$475	\$550
Thursday (Half Day, AM or PM)	\$275	\$275

Student Fees

50% discount for full-time students.
Proof of enrollment required. Student fees apply only to Symposium or Tutorial registration and do not apply to Bundled Fees.

Total Symposium Experience: Save with Bundled Fees.

(Symposium plus 3 full days of tutorials.)		
ESD Association Members	\$1,725	\$2,110
Non-Members	\$1,815	\$2,110

S20.20 Seminar

(Attendance limited to first 30 registrants)	\$1,495	\$1,495
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Exhibits Only*

No Charge	No Charge
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*Pre-registration not required for exhibits only.

From the president

Serving Industry in Asia



Ed Weggeland

Three of our experienced Program Managers and Educators traveled to Singapore in March to deliver seminars and information.

On Tuesday, March 23 we invited selected local industry managers to a luncheon presentation. 26 managers from a cross section of electronic companies attended and listened to Ron Gibson tell about the "State of



Ron Gibson

the ESD Science", what they could expect in the future in terms of ESD sensitivity levels and how they can prepare their process to remain competitive on a global basis. The attendees expressed their satisfaction with this learning experience. We will now make appropriate modifications to this management information program and plan on delivering it again in as many venues as possible.

On Wednesday and Thursday, March 24-25 we gave certification prep course seminars. Steve Halperin delivered our new ESD Basics and Auditing sections to 40 at-



Steve Halperin

tendees.

Ron Gibson and John Kinnear delivered 2 days of our S20.20 Program Managers module to 17 attendees.

Soon, the positive reaction spread throughout the region and requests for repeats began accumulating from Malaysia, Thailand, Taiwan, Philippines and China.

We asked attendees for feedback and received much praise along with ratings between 4 and 5 (5 is the best rating on our attendee questionnaire forms).



John Kinnear

Association news

What's New On The ESDA web site

More Organized Main Page

The main page of the web site has been reorganized to make items easier to find. (www.esda.org)

2004 Symposium Exhibitors

View an updated list of exhibitors who have reserved space at the 2004 EOS/ESD Symposium. (www.esda.org/exhibits.html)

Standards Activity Update

A complete report of standards activities from the last Standards Meeting Series, held February 19-22, 2004 in Los Angeles. (www.esda.org/standards.html#update)

June Standards Meeting Schedule

A complete schedule for the upcoming Standards Meeting Series, scheduled for June 3-8, 2004 in Grapevine (Dallas), TX. (www.esda.org/standards.html#schedule)

Volunteer Spotlight

The ESD Association has added a new section to the web site highlighting Volun-

teer Activities. The Volunteer Spotlight will focus on a different volunteer each month and their contributions to the Association. The first Spotlight is on Larry Burich. (www.esda.org/csp.html)

Our event co-sponsors Pro-Pack Pte. Ltd. and PSB Corporation assisted us with venue, logistics and marketing, for which we give our thanks and appreciation. Special recognition is appropriate for Steve Halperin, Ron Gibson and John Kinnear because they have never worked as long or hard at delivering these programs. Their audiences made for very lively and extended Q&A sessions. By the end of the 3-day programs, they all felt exhausted and ready to board their flights to get some alone time and rest. As a seasoned foreign traveler, I can attest to how they felt.

We have now officially broken ESDA ground in SE Asia and have come away with very high expectations for our continu-

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ESD Design Seminar

The ESD Association has scheduled an ESD Design Seminar May 24 & 25, 2004 in Rome, NY. (www.esda.org/news.html or www.esda.org/education.html)

Three new FREE downloads

(www.esda.org/standards.html)

View or download these standards documents:

- ANSI/ESD STM5.1-2001: Electrostatic Discharge Sensitivity Testing—Human Body Model (HBM) Component Level
- ANSI/ESD STM5.2-1999: Electrostatic Discharge Sensitivity Testing—Machine Model (MM) Component Level
- ANSI/ESD STM5.3.1-1999: Charged Device Model (CDM)—Component Level

All digitizing scopes (with the same Band Width) are not created equal



Leo G. Henry

Over the last few years I have read many articles on oscilloscopes in several electronic magazines. A few of them have made me pause and think about going back to engineering school to do research, yes, on scopes. One author was careful to point out that statements about “the performance” of new and improved scopes must be carefully qualified. Here is one example of a pronouncement:

“This new scope delivers the highest performance solution for connecting, triggering, acquiring and analyzing single-shot or repetitive high-speed signals on multiple channels to customers whose designs push technology limits and compete for fast delivery in the marketplace”.

That was a ‘mouthful’! This qualification check is specifically true when it comes to specifying the scope’s Bandwidth (BW), Rise time (Tr) and sampling rate for capturing single-shot events.

Breakthrough

The situation became more acute when I received an email last month that included the announcement of a company’s breakthrough with respect to scope BW. The scope was an 8 GHz BW 4-channel Digital Storage Oscilloscope (DSO) with 20 GS/sec sampling rate. After saying that the new series raises the industry standard for signal capture and integrity, the announcement proceeded to quote the rise time in the 20-80% region. There was no mention of the traditional 10-90% range,

so I called the manufacturing company. I was told that most customers are now asking for the 20-80% rise time domain, and no, none of these customers have anything to do with ESD or TLP Testing for ESD design verification and qualification of ICs.

I could have shed a tear, knowing how important the scope is to the ESD device design and test community, but my system was still “dry” from those previous articles I mentioned earlier. These customers say they are working with rapidly increasing bit and clock rates in complex digital architectures, are working with leading-edge applications such as XAUI, PCI-Express and Infini-band in the communications, computer, and semiconductor industries and are tasked with connecting, triggering, acquiring and analyzing fast, multiple, complex, signals simultaneously.

Rise Times

I then indicated to the manufacturing company that I was still puzzled by the numbers quoted for the scope’s rise times and that I needed additional clarification. I needed to know why the “time tested” Tr equation of $0.35/BW(\text{GHz})$ was not producing the same rise time numbers as is seen in their announcements. For the 8GHz DSO, the announcement quoted a Tr of 35 psec (20%-80%) with DSP turned on, but the time-tested equation (TTE) that I used gave a Tr of 44 psec (10%-90%).

I could not see how the simple approximation was so far off from their numbers. First I was told that it was a marketing decision to use those numbers in the announcement, so I pressed for a better explanation. Then I was handed over to three different engineers; this is what I found out:

The engineer explained that they have changed the way that they are doing things, measuring things and calculating things. Historically, she said, oscilloscope frequency response tended to approximately follow the rule: **Bandwidth x risetime \approx 0.35** (where the rise time is in pico-seconds, and the BW is in GHz). This corresponds to a specific filter roll-off in the frequency domain. Today, at the high end, most real-time digital oscilloscopes more closely follow a new rule: **Bandwidth x rise time \approx 0.45**. This risetime factor corresponds to a much steeper frequency roll-off above the specified bandwidth. The steeper roll-off is more desirable in digital oscilloscopes that over-sample by 4x, 3x, and because it prevents aliasing by eliminating any signal above the Nyquist frequency (1/2 the sample rate - the minimum sample rate required for accurate signal representation).

Time-Tested Equation

I then presented the following table with DSOs and DPOs (Digital Phosphor Oscilloscopes) with a view to understanding why the time-tested equation (TTE) at 10%-90% did not give the same Tr numbers as they have quoted. Further, why are their numbers larger? It is to be noted that earlier scopes all had the TTE numbers.

500 MHz DPO using TTE is 700 psec.	TEK # is 800 psec
1.0 GHz DPO using TTE is 350 psec.	TEK # is 400 psec
4.0 GHz DPO using TTE is ~ 78 psec.	TEK # is 100 psec
6.0 GHz DSO using TTE is ~ 58 psec.	TEK # is 70 psec
7.0 GHz DSO using TTE is ~ 50 psec.	TEK # is 62 psec
8.0 GHz DSO using TTE is ~44 psec.	TEK # is 50 psec

She continued: “This number (factor) depends on the shape of the oscilloscope’s frequency response curve and pulse rise time response. Oscillo-

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Industry Update

IEDM held December 7-10, 2003 in Washington D.C.

by
Charvaka Duvvury
Texas Instruments
ESD Assoc. Board of Directors

As we move forward with the aggressive scaling of silicon technologies, the potential impact on ESD continues to be of increasing concern. Of course, since the humans that handle the IC's are not being scaled accordingly, the HBM threat at best remains the same! No further comment is necessary.

New Column

To keep up with these new developments *Threshold*TM is launching a new column where the latest trends in technology will be summarized, especially as gathered from the papers presented at other electronics conferences. Whether they have direct impact on ESD or not, it is hoped that the presented highlights are of general interest. In addition, a brief description and significance of the pertinent ESD papers presented at these conferences will be summarized.

Two special conferences covered in this issue are the International Electron Devices Meeting, commonly known as the IEDM, and the International Reliability Physics Symposium (IRPS).

IEDM

The IEDM is a major device physics and technology development conference that is held every year with an attendance of about 1,500 to 2,000 people. Approximately 240 papers are presented each year in 8 parallel sessions. ESD has gained enough importance at this conference that now 3-4 papers on the ESD topic are accepted regularly. The focus of these papers tends to be mainly on device effects.

IEDM 2003

At the IEDM 2003, held in Washington D.C. December 7-10, 2003, there were several new exciting developments for the industry. These are:

- Electronic Cloth – you may soon have to wear your computer!
- Ambient Intelligence with electronics

woven into carpets – now, that is really challenging for ESD!

- Artificial skin for robots – new robotic model for the Standards?!
- Polycrystalline on transparent plastic or silicon on glass – no package to test
- Organic Thin Film Transistors for RF Tags
- Optical MEMs Switches

Summary of the ESD Papers at IEDM 2003:

Technology Scaling Effects on the ESD Design Parameters in Sub-100nm CMOS Transistors

by Gianluca Boselli, John Rodriguez, Charvaka Duvvury, Vijay Reddy, P.R. Chidambaram, and Biran Hornung, Texas Instruments.

This paper reported a new phenomenon showing an unexpected drastic reduction of the NMOS and PMOS triggering voltage (V_{t1}) under ESD conditions for a 90 nm CMOS technology. This severe effect comes from technology scaling through

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IRPS held April 25-29, 2004 in Phoenix, Arizona

by
Steve Voldman, IEEE Fellow
IBM Microelectronics
ESD Assoc. Board of Directors

The 2004 International Reliability Physics Symposium was held April 25-29 in Phoenix, Arizona. Continuing the trend started last year, a special session addressing Latchup was included in the technical program, as well as many interesting technical sessions on ESD. This is the first year that a tutorial on Latchup was offered at IRPS.

A full day tutorial containing Latchup, ESD Device and ESD Testing Expertise was held on Sunday, April 25:

- Latchup and ESD in Advanced Technologies: S. Voldman of IBM Microelectronics
- ESD Protection Design in CMOS: T.

Maloney of Intel Corporation

- ESD Testing: H. Gieser of Fraunhofer IZM

A four paper session discussing CMOS Latchup was held on Tuesday, April 27. The special Latchup session contained discussion on state-of-the-art issues such as latchup solutions. The following publications were presented:

- *Contention-induced Latchup* by J. Mechler of the IBM Microelectronics ASIC team.
- *Model-based Guidelines to Suppress Cable Discharge Events (CDE) induced latchup in CMOS Integrated Circuits*, by Kiran Chatty of IBM Microelectronics.
- *The Influence of Deep Trench and Substrate Resistance on the Latchup Robustness in a BiCMOS Silicon Germanium Technology*, by Steven

Voldman of IBM Microelectronics, and undergraduate Anne Watson of Pennsylvania State University.

- *The Influence of Heavily Doped Buried Layer Implants on Electrostatic Discharge, Latchup and Silicon Germanium Bipolar Transistors in a BiCMOS SiGe Technology*, by Steven H. Voldman, and L. Lanzerotti of IBM Microelectronics, Wes Morris of Silicon Engineering and Len Rubin of Axcelis Corporation.

Additionally, several ESD poster sessions were held on Tuesday, April 27:

- *Chip-level ESD simulation for fail detection and design guidance* by S. Druen et al of Technical University of Munich
- *Increased ESD robustness of a lat-*

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Industry update

*Continued from page 6***IEDM held December 7-10, 2003 in Washington D.C.**

merging of the pocket implants at the transistor source and drain that are necessary for control of the transistors for their performance and leakage. This can have serious impact for protection circuit designs and burn-in reliability conditions thus pointing to the constant need of monitoring technology developments for ESD reliability.

Implementation of Temperature Dependent Contact Resistance Model for the Analysis of Deep Submicron Devices under ESD

by Jung-Hoon Chun, Yang Liu, Charvaka Duvvury, and Robert Dutton, Stanford and Texas Instruments.

Modeling for ESD is an extremely challenging task. This paper is an important

step forward to model the silicide contact resistivity and its dependence on temperature. More work continues in developing thermal simulators for ESD understanding and predictive capability.

Diode-Triggered SCR (DTSCR) for RF-ESD Protection of BiCMOS SiGe HBTs and CMOS Ultra-Thin Gate Oxides

by Markus Mergens, Christian Russ, Koen Verhaege, John Armor, Phillip Jozwiak, Russ Mohn, Bart Keppens, and Con Son Trihn, Sarnoff Europe.

This paper described a novel diode-chain triggered SCR ESD protection in low voltage (1.8 V) applications. This new device enables HBM and CDM ESD protection design of ultra-sensitive IC nodes such as advanced BiCMOS ultra-thin gate oxide CMOS.

*Continued from page 6***IRPS held April 25-29, 2004 in Phoenix, Arizona**

eral npn structure in advanced CMOS by V. Vassilev of IMEC

- High current characteristics of Copper interconnect under TLP Stress and ESD zapping by J. H. Lee of Taiwan Semiconductor Manufacturing Corporation
- Comparison of Ultra-High Thin Gate Oxide ESD Protection Capability of Silicided and Silicide Block NFETs by J. H. Lee of Taiwan Semiconductor Manufacturing Corporation

A four paper session discussing On-chip ESD Protection was held on Wednesday, April 28. These publications were presented:

- Native NMOS triggered SCR (NANSCR) for ESD protection in 0.13 μ m CMOS integrated circuits by Prof. Ming Dou Ker and C. Hsu of Taiwan National Chiao-Tung University
- Base pushout driven snapback in parasitic bipolar devices between different power domains by U. Glaser of Integrated System Lab and Infineon Technologies
- Effects of hot spot hopping and drain ballasting in integrated vertical DMOS devices under TLP stress by P. Moens

et al of AMI Semiconductors

- Gate Dielectric Breakdown: A focus on ESD Protection by Bonnie Weir of Agere Systems
- A PMOSFET ESD Failure caused by Localized Charge Injection by J. Chun of Stanford University

To top it all off, in the Compound Semiconductor Session held on Thursday, April 29, a paper relating to ESD was presented:

- Bipolar SCR ESD protection in a 0.25- μ m Silicon Germanium process using sub-collector modifications by Vladimir Vashenko of National Semiconductor.

For a reliability physics symposium, that is a lot of ESD and Latchup issues. For all those ESD engineers hungry for more ESD and Latchup information, the 2004 IRPS offered plenty to hold you over until the 2004 EOS/ESD Symposium! Proceedings from IRPS 2004 and past symposia are available for purchase from the IRPS web site at www.irps.org.

The material discussed at IRPS 2004 illustrates the current trend: the ESD field is growing as semiconductor devices are shrinking!!

Standards

Final Schedule

June 2004 ESD Association Standards Meeting Series

Gaylord Texan Resort & Conference Center

Grapevine (Dallas), TX

June 3-8, 2004

Thursday, June 3, 2004

8:00 AM TAS

Friday, June 4, 2004

7:00 AM TAS

8:00 AM Device Testing WG-5
Ionization WG-3
Grounding WG-6

1:00 PM Handlers WG-10

Saturday, June 5, 2004

7:00 AM TAS

8:00 AM Device Testing WG-5
Work Stations WG-53
Cleanrooms WG-55

1:00 PM Packaging WG-11
Garments WG-2

5:30 PM Working Group Chairs

6:30 PM ESDA Mixer

Sunday, June 6, 2004

7:00 AM TAS

8:00 AM Flooring WG-7
Simulators WG-14
Gloves WG-15
ICE

1:00 PM Standards Committee

5:00 PM Technical Liaison

6:00 PM Executive Committee

Monday, June 7, 2004

8:00 AM Human Resources

10:00 AM Marketing & Communications

1:00 PM Technology Road Map

2:00 PM Steering

Tuesday, June 8, 2004

8:00 AM Board of Directors

From the Threshold chair

Continued from page 5

All digitizing scopes (with the same Band Width) are not created equal

scopes with a bandwidth of <1GHz typically have a 0.35 value, while oscilloscopes with a bandwidth >1GHz usually have a value between 0.40 and 0.45.” So here is my question. Did you guys in the testing business know about all of this stuff? I have never heard these ideas/changes discussed at the Device Testing Working Group meetings. Have we been making decisions on scope requirements based on inadequate data?

In the case of the TDS6804B (8GHz BW) specifically, she said, you will notice that it says: 62 psec (10-90%) (typical). The “typical” means that it is not even calculated using the above calculation, but takes several of our scopes, measures it, and gets the average of it. This means that this spec is not warranted. If you do the calculation with 62 psec, you will get 0.434, which is within the numbers given above.

So there are no rules, I pined? What about the quoted numbers for the 20-80% domain as shown below?

SCOPE	Tr @ 10%-90%	Tr @ 20%-80%
6 GHz DSO	70 psec ?	53 psec
7 GHz DSO	62 psec?	43 psec
8 GHz DSO	50 psec?	35 psec

For ESD Testing & TLP testing for the Qualification and ESD design development of product, we do NOT use these numbers. Please tell us what formula is being used for the 20-80%?

Because we are not using the formula above, she continued, you get both 10-90 and 20-80 the same way. You measure a rising edge, then to find the 50%, you go down to the 10% and up to the 90% (or down to the 20% and up to the 80%) and find the delta V over delta t value, which is

the definition of risetime.

Why are you making this big distinction between performance BW and the true analog BW? If the analog BW (at -3-dB) of the scope produces the true risetime of the system, why the performance BW? Where is this used? I have read this before, but never “homed” in on it as I am doing now. Please clarify.

Her response: I assume that you mean the Digital Signal Processing (DSP) enhancement bandwidth when you say performance bandwidth. The reason we are making the distinction between analog and DSP bandwidth is that we do not want to mislead our customers. Some customers will welcome the extra bandwidth that is brought by our DSP technique, but others will not want digital smoothing, so we give both specs, and give customers the ability to turn it (DSP) off. As to how DSP achieves the extra bandwidth, our engineers are putting together a white paper on this subject, but have not yet published it.

Conclusion

My summary is that we need to be careful about announcements of new products with enhanced features. We can trust, but we need to verify, because in this case: ALL Digitizing Scopes (with the same BW) Are Not Created Equal.

The example is the comparison between the older 1GHz 7104 (350 psec Tr & 250 GS/s on one channel) with the 1GHz TDS-7104 (400 psec Tr & 10 GS/s on one channel) or the comparison between the 500 MHz (700 psec Tr) and the 500 MHz DPO (800 psec Tr). Here we see that we need to be sure that we are comparing equivalent rise times in addition to the BWs. In the previous examples, we need to be sure that we are talking about equivalent time domain (10%-90% or 20%-80%).

Meanwhile, please take some time and read or re-read “The 10 steps to Choosing The Right Oscilloscope”, an HP technical report, 2001, found on the HP website.

Stay tuned because it is the opinion of some of the DT members that this breakthrough will help the ESD-VF-TLP community in its characterization of product.

Be Happy



leogesd@pacbell.net

From the president

Continued from page 4

Serving industry in Asia

ing plans to “Serve Industry” on a global basis. Over the course of the next months we will discuss plan proposals to expand these types of programs, including Device Design Seminars, into additional countries and markets.

The level of interest in our programs and products in the Asian markets is very high and their quest for knowledge and solutions to their ESD problems is dramatic and clearly evident. As in the past, we will respond to the demands of our industry and customers in our typical professional manner.

I take great pride in our Association, what we deliver to industry, and the people who work so hard to make this possible. So many of our volunteers contribute to the end result – thank you all.

Association news

ESDA Certification Programs: Program Manager and Device/Design Professionals

In the tradition of providing valuable education opportunities to our membership, the ESD Association now offers Professional Certification for ESD Control Program Managers and for Device/Design Technical specialists. Now you can be recognized for having learned the core material in either of these two disciplines.

The impact of the ANSI/ESD S20.20 ESD Control Program on the global industry has been extraordinary. The ESDA's Board of Directors recognized the need to offer a certification program for individuals that are involved in designing, implementing, managing and auditing ESD control programs in their facilities. The Program Manager

Certification program was announced in 2003 to serve that purpose. In addition, the needs of the technical community for certification of various technical specialties are apparent. The ESDA is pleased to now offer a certification program for ESD Device/Design professionals as well.

These certifications will provide the recognition that certain individuals have demonstrated expertise in the disciplines required for mastery of Program Management or Design of ESD protection circuits. Requirements for certification will include, as a minimum, attending required prerequisite tutorials and passing a final exam. Sign up at Symposium and start earning

your credits! Many of the prerequisite courses are available in the 2004 Symposium tutorial program (watch for the Symposium Program brochure for the list) and additional courses are in development. Note that not all of the courses can be offered every year, although we will try our best to offer as many as possible.

Please check out the ESD Association web site at www.esda.org for announcements regarding these exciting and important new offerings. Details of these Certification Programs also will be available at the EOS/ESD Symposium; just stop by the ESD Association booth for more information.

Local chapter news

Philippine ESD Forum successfully launched

The 1st Philippine Electrostatic Discharge Forum, the Premier Learning Conference on Electrostatic Discharge, was successfully launched March 17-18, 2004 at the New World Renaissance Hotel in Makati City, Philippines. The event was organized by the ASEMEP Electrostatic Discharge Council (AEC), and sponsored by the Semiconductors and Electronics Industries in the Philippines (SEIPI) and the Association of Semiconductor & Electronics Manufacturing Engineers of the Philippines (ASEMEP).

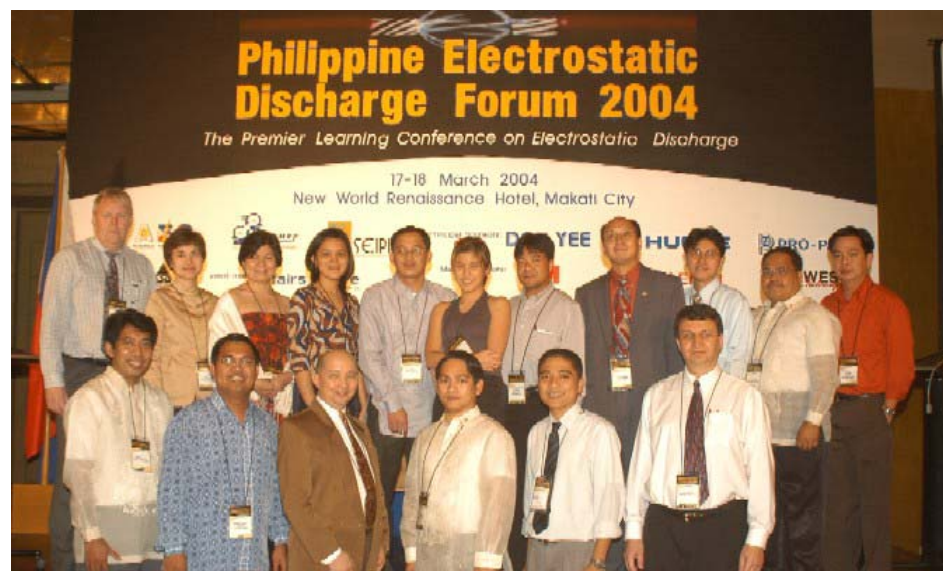
Mr. Ed Weggeland, the current President of the ESD Association, was scheduled to give the keynote address and a tutorial. However, a personal emergency prevented him from attending and on his behalf, Mr. Cesar Moll, ASEMEP's immediate past chairman gave the keynote address and Mr. Jess Muñoz, current AEC chairman delivered the tutorial.

Local speakers included Department of Science and Technology Undersecretary Fortunato dela Peña who graced the event as the Inspirational Speaker, Dr. Romeric Pobre from De La Salle University-Manila, and Mr. Nido Calida from Hugle Technologies.

International speakers included Dr. Wei Guan from Ion Systems, Mr. Lei Zhi Pei from Setsco Services Pte. Ltd., Mr. Vladimir Kraz from Credence Technologies, Mr. Toshikazu Numaguchi of 3M Japan and Mr. Jos van de Giesen of Philips Semiconductors Nijmegen, The Netherlands.

The event had 6 exhibiting companies and more than 200 participants represent-

ing 38 different companies. In the Philippines, these companies are located in Metro Manila, Baguio, Cebu, Subic, Cavite and Laguna. The international delegates represented companies in Singapore, Malaysia, Thailand, Taiwan and Hong Kong. The event also marked the first Asian venue for the NARTE ESD certification exam with 40 ESD practitioners taking the test.



The ASEMEP, AEC, event organizers, speakers and exhibitors pose for a group picture at the conclusion of the forum.

Calendar

May 2004

NEPCON East: May 4-6, 2004, Hynes Convention Center, Boston, MA; www.nepconeast.com

ESD Northwest Chapter Membership Meeting: May 11, 2004, Vanguard EMS, Beaverton, OR; www.esdnw.org

Texas ESD Association Meeting: May 18, 2004, Regional Tutorial Program-Topics include ESD Basics, S20.20 Program Implementation, Factory Auditing, Q&A and Wrap Up; 3M Innovation Center, Austin, TX; www.centxesdassoc.homestead.com

ESDiscovery 2004: May 18, 2004, Silicon Valley EOS/ESD Society; AMD Campus Common Building, Sunnyvale, CA; www.esdsiva.org

SMTA Medical Electronics Symposium: May 19-20, 2004, Marriott Minneapolis Airport Hotel, Bloomington, MN; www.smta.org

ESD Design Seminar: May 24-25, 2004; ESD Association headquarters, Rome, NY; www.esda.org

IEEE International Symposium on Power Semiconductor Devices & IC's: May 24-27, 2004; Kitakyushu International Conference Center, Kitakyushu, Japan; www.ieee.org

ESDiscovery ASIA 2004: May 26-June 1, 2004 in Singapore, Penang, and Shanghai, presented by the Silicon Valley EOS/ESD Society; www.esdsiva.org

June 2004

ESDA Standards and Committee Meetings: June 3-8, 2004; Gaylord Texan Resort and Conference Center, Grapevine (Dallas), Texas; www.esda.org

ESD Northwest Chapter Board Meeting: June 8, 2004, Vanguard EMS, Beaverton, OR; www.esdnw.org

July 2004

ESD Northwest Chapter Membership Meeting: July 13, 2004, Vanguard EMS, Beaverton, OR; www.esdnw.org

August 2004

ESD Northwest Chapter Board Meeting: August 10, 2004, Vanguard EMS, Beaverton, OR; www.esdnw.org

September 2004

ESD Northwest Chapter Membership Meeting: September 14, 2004, Vanguard EMS, Beaverton, OR; www.esdnw.org

ESDA Standards and Committee Meetings: September 19-23, 2004, Gaylord Texan Resort and Conference Center, Grapevine (Dallas), Texas; www.esda.org

EOS/ESD Symposium: September 19-23, 2004, Gaylord Texan Resort and Conference Center, Grapevine (Dallas), Texas; www.esda.org

ESD Certification Exams: September 24,

2004, Gaylord Texan Resort and Conference Center, Grapevine (Dallas), Texas; www.esda.org

October 2004

ESD Northwest Chapter Board Meeting: October 12, 2004, Vanguard EMS, Beaverton, OR; www.esdnw.org

NEPCON Texas: October 20-21, 2004, Arlington Convention Center, Arlington (Dallas), TX; www.nepcontexas.com

November 2004

ESD Northwest Chapter Membership Meeting: November 9, 2004, Vanguard EMS, Beaverton, OR; www.esdnw.org

December 2004

ESD Northwest Chapter Board Meeting: December 14, 2004, Vanguard EMS, Beaverton, OR; www.esdnw.org

Association news

Register now for May 24-25 ESD design seminar

There is still time to register for the ESD design seminar scheduled for May 24-25, 2004, at the ESD Association Headquarters in Rome, NY

Created specifically to meet the needs of persons responsible for ESD protection in circuit design, this two-day seminar program includes in-depth technical education in a number of specific areas including the following:

ESD in the Industrial Semiconductor IC Context: What is ESD? Why is it important? What methods are used to control it?

ESD Models and ESD Testing: Description of the three models and model issues from the designer's point of view.

ESD Device Operation: Fundamentals of MOS device operation, the role of PMOS, BiCMOS and the similarity of the techniques for CMOS, bipolar devices, DENMOS and LDMOS devices and protection techniques.

ESD Circuit Operation: Operation of and issues with NMOS circuits, including

implementation, simulation, and experimental results.

Technology Impact on ESD Design Choices: Review of ESD protection design options as a function of technology and process fluctuations.

Special Circuit Requirements and Their Impact on ESD: Mixed voltage protection, RF and analog protection, BiCMOS, high voltage protection, and new latchup effects.

CDM ESD Protection: Concerns and considerations; fast enough diodes, transistors, and SCRs; the on-chip CDM event.

Design Examples and Case Studies: Layout methods, ESD rules, new design methods, case studies of protection design problems, and class exercises.

Instructors for the seminar are Charvaka Duvvury, Ph. D., Texas Instruments, and James W. Miller, Motorola.

Detailed information and a registration form may be downloaded from the ESDA Web site, www.esda.org. For more information on the ESD Design Seminar, contact ESDA headquarters.

Institutional Listings

<p>Howell Packaging, Division of F.M. Howell & Company P.O. Box 286, Elmira, NY 14902 Tel: 607-734-6291 Fax: 607-734-8667 Designers & Manufacturers of ESD Protective Packaging, Paperboard & Thermoformed Plastic, In-House Testing</p>	<p>DESCO 3651 Walnut Avenue, Chino, CA 91710 Tel: 909-627-8178 Fax: 909-627-7449 www.desco.com Manufacturer of ESD control products including wrist straps, mats, foot grounders, ionizers, shielding bags, floor finish & more</p>
<p>Conductive Containers, Inc. 4500 Quebec Ave. North, New Hope, MN 55428 Tel: 1-800-FARADAY Fax: 763-537-1738 www.corstat.com Manufacturer of CORSTAT conductive corrugated products and ESD safe thermoformed plastic designs for shipping, storage & handling.</p>	<p>3M Electronic Solutions Division Tel: 1-800-328-1368 www.3M.com/eisd Manufacturer of static control permanent flooring, wrist/heel straps, static shielding bags, & testing/monitoring equipment</p>
<p>VPI 3123 S. 9th St., P.O. Box 451, Sheboygan, WI 53082-0451 Tel: 800-874-4240 Fax: 920-458-1368 E-mail: floor@vpiflooring.com www.vpiflooring.com Manufacturer of ESD Control Solid Vinyl Floor Tile</p>	<p>TREK, INC. 11601 Maple Ridge Road, Medina, NY 14103 Tel: 585-798-3140 Fax: 585-798-3106 Web: www.trekinc.com Manufacturer and designer of instrumentation and sensors for measuring surface voltage, ionizer performance, and surface resistivity</p>
<p>Kenflex Corporation 460 NE Hemlock, Suite A, Redmond, OR 97756 Tel: 541-923-4765 Fax: 541-923-4190 sales@kenflex.com Manufactures FLEXCELL®, FLEXSTAND®, FLEXTOTE® circuit board transport and protection units, also on Web. For additional information: www.kenflex.com</p>	<p>ACL Staticide 1960 E. Devon Avenue, Elk Grove Village, IL 60007 Tel: 847-981-9212 Fax: 847-981-9278 www.aclstaticide.com Cleanroom products, topical antistats, floor finishes and coatings, static detection meters, monitors, computer cleaning products</p>
<p>ESDSYSTEMS.com 432 Northboro Rd. Central, Marlboro, MA 01752-1823 Tel: 508-485-7390 Fax: 508-480-0257 www.esdsystems.com A full line of ESD control products: wrist straps/foot grounders/mats/ ionizers/floor finish/shielding bags/smocks/testers & more</p>	<p>Wolfgang Warmbier Untere Giesswiesen 21, D-78247 Hilzingen, Germany Tel: 49-7731-86880 Fax: 49-7731-868832 www.warmbier.com ISO 9002 certified for advice, supply and manufacturing of static control materials and systems</p>
<p>Monroe Electronics 100 Housel Avenue, Lyndonville, NY 14098 Tel: 585-765-2254 Fax: 585-765-9330 E-mail: electrostatics@monroe-electronics.com www.monroe-electronics.com Full line manufacturer of static measurement equipment</p>	<p>Static Solutions Inc. 331 Boston Post Rd.-East, Marlboro, MA 01752 Tel: 508-480-0700 Fax: 508-485-3353 www.staticsolutions.com Manufacturer of patented ESD, Cleanroom & Maintenance products including Ohm-Stat™ combination & resistivity meters, Ohm-Shield™, coatings, floor finish, and paint, Ohm-Cide™ EPA cleaners, Stat-o-Flex™ class zero wriststrap and more.</p>
<p>HMS Compounds, Inc. P.O. Box 388, Mansfield, TX 76063 Tel: 817-468-3099 Fax: 817-468-3122 www.hmscompounds.com Manufacturers of Conductive and Static Dissipative Thermoplastic Sheet and Roll Stock for ESD Protection</p>	<p>VPI Mirrex Corp. 1389 School House Road, Delaware City, DE 19706 Tel: 302-836-5950 Fax: 302-836-7571 www.vpicorp.com Manufacturer of ESD thermoplastic materials for the display and protection of static sensitive components</p>
<p>Saint-Gobain Advanced Ceramics 1225 Aeroplaza Drive, Colorado Springs, CO 80916 Tel: 719-637-8737 Fax: 719-380-5591 E-mail: william.losch@saint-gobain.com Manufacturer of Cerastat™ ESD ceramics products to customers' prints: tools, fixtures, wear parts for data storage & other electronic industries</p>	<p>RMV Technology Group, LLC ESD Materials Testing (paper, polymers, foam) Tel: 925-673-0225 www.esdrmv.com Fax: 925-672-3316 NARTE Certified ESD Engineer on Staff & Certified DVBE S20.20 Program Leadership, Materials Evaluation & ESD Product Qualification Comprehensive ESD Audits, On-Site Seminars & Employee Training</p>
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<p style="text-align: center;">Molded Fiber Glass Tray Co.</p> <p>6175 US Highway 6, Linesville, PA 16424 Tel: 800-458-6050 Fax: 814-683-4504 e-mail: info@mfgtray.com Manufacturer of static dissipative and conductive trays and containers for static protection of sensitive parts.</p>	<p style="text-align: center;">Vermason Ltd.</p> <p>1 Avenue One, Letchworth, Herts., SG6 2HB, England Tel: +44 1462 672005 Fax: +44 1462 670440 sales@vermason.co.uk Manufacturer of ESD products. For more information, www.vermason.com</p>
<p style="text-align: center;">Tech Wear</p> <p>2205 Faraday Ave., Suite B, Carlsbad, CA 92008 Tel: 760-438-7788 Fax: 760-438-6868 Email: kay@techwear.com www.techwear.com Industry leader in static control garments, including groundable cleanroom garment systems.</p>	<p style="text-align: center;">TOPLINE-ELME</p> <p>7331A Garden Grove Blvd., Garden Grove, CA 92841 Tel: (800)776-9888 Email: info@ESD.TV www.ESD.TV Full line ESD products including shoes, garments, chairs, brushes, mats, gloves. Maximum comfort.</p>
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More institutional listings, previous page

Threshold

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ThresholdTM Publication Schedule

Issue	Deadlines
July/August	June 1
September/October	Aug. 1
November/December	Oct. 1
January/February	Nov. 19
March/April	Feb. 1
May/June	April 1



7900 Turin Road, Building 3
Rome, NY 13440-2069
Tel: (315) 339-6937 Fax: (315) 339-6793
E-mail: info@esda.org
Web: www.esda.org

Newsletter Staff

Threshold Chair

Leo G. Henry, Ph.D.
ESD/EMI/TLP Consultants
P.O. Box 1665, Fremont, CA 94538
Tel: 510-657-5252 Fax: 510-657-9661
E-mail: leogesd@pacbell.net

Board of Directors Sponsor

Craig Zander
Restronics Company, Inc.
7125 Washington Ave., So., Edina, MN 55439
Tel: 952-941-9135
E-mail: czander@restronics.com

Editor

Terri DeMario
ESD Association
7900 Turin Road, Bldg. 3, Rome, NY 13440
Tel: 315-339-6937 Fax: 315-339-6793
E-mail: info@esda.org

Associate Editors

Development

Ed Weggeland, Static Control Components, Inc.

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