## EOS/ESD Symposium Outstanding Paper (Best Presentation) Awards

**1983** “The Room Air Ionization System, a Better Alternative than 40% Relative Humidity”
**C. F. Mykkanen and D.R. Blinde**

**1984** “The Effectiveness of Antistatic Bags in Screening Semiconductor Components Against ESD Transients”
**TIE** **G.C. Holmes**

**1984** “A Realistic and Systematic ESD Control Plan”
**G.T. Dangelmayer**

**1985** “A Technique for Real-Time Examination of Sub-Surface EOS/ESD Damage in Integrated Circuits”
**C.T. Amos and C.E. Stephens**

**1986** “Thick Oxide Device ESD Performance Under Process Variations”
**R.A. Mc Phee, C. Duvvury, R.N. Rountree, H. Domingos**

**1987** “ESD Protection Structures to Survive the Charged Device Model (CDM)”
**L.R. Avery**

**TIE**
**1988** “A Process-Tolerant Input Protection Circuit for Advanced CMOS Processes”
**Robert Rountree, Charvaka Duvvury, Tatsuro Maki, Harvey Stiegler**

**1988** “Triboelectricity and Surface Resistivity Do Not Correlate”
**Steven L. Fowler**

**1989** “Understanding Pink Poly”
**Marvin R. Havens**

**1990** “Electrostatic Discharge Protection for a 4-Mbit DRAM”
**Mark D. Jaffe**

**1991** “Implementation of Computer-Based ESD Training: A Case Study Comparing the Computer Approach With

Traditional Classroom Techniques”
**Joanne Woodward-Jack**

**1992** “ESD Protection In a 3.3V Sub-Micron Silicided CMOS Technology”
**David Krakauer and Kaizod Mistry**

**1993** “The Identification and Analysis of Latent ESD Damage
on CMOS Input Gates”
**Jim Colvin**

**1994** “The Impact of Technology Scaling on ESD Robustness and Protection Circuit Design”
**Ajith Amerasekera and Charvaka Duvvury**

**1995** “Advanced CMOS protection Device Trigger Mechanisms
During CDM”
**Charvaka Duvvury and Ajith Amerasekera**

**1996** “Recommendations to Further Improvements of HBM ESD
Component Specifications”
**Koen Verhaege, Christian Russ, G. Groeseneken, Donna Robinson-Hahn, Don Lin, Marty Farris, Jeff Scanlon, J.Veltri**

**1997** “ESD Robustness and Scaling Implications of Aluminum and
Copper Interconnects in Advanced SemiConductor Technology”
**Steven Voldman**

**1998** **“**Magneto Optical Static Event Detector**”**
**N. Jacksen, Wayne Tan, Don Boehm**

**1999** “An Anti-Snapback Circuit Technique for Inhibiting Parasitic Bipolar Conduction During EOS/ESD Events”
**Jeremy Smith**

**2000** “Wafer Cost Reduction through Design of High Performance Fully Silicided ESD Devices”
**Koen Verhaege, Christian Russ**

**2001** “Multi-Finger Turn-on Circuits and Design Techniques for Enhanced ESD Performance and Width-Scaling”
**Markus P. J. Mergens, Koen G. Verhaege, Christian C. Russ, John Armer, Phillip C. Jozwiak, Girija Kolluri, Leslie R. Avery**

**2002** "Efficient pnp Characteristics of pMOS Transistors in Sub-0.13 μm ESD Protection Circuits"
**G. Boselli, C. Duvvury, V. Reddy, Texas Instruments Inc.**

**2003** " Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies"
**M. Stockinger, J.W. Miller, M.G. Khazhinsky, C.A. Torres, J.C. Weldon, B.D. Preble, M.J. Bayer, M. Akers, Motorola; V.G. Kamat, Synopsis, Inc.**

**2004** "Engineering Single NMOS and PMOS Output Buffers for Maximum Failure Voltage in Advanced CMOS Technologies"
**M.G. Khazhinsky, J.W. Miller, M. Stockinger, J.C. Weldon Freescale Semiconductor, Inc.**

**2005** Analysis of ESD Protection Components in 65nm CMOS Technology: Scaling Perspective and Impact on ESD Design Window
**G. Boselli, J. Rodriquez, C. Duvvury, J. Smith, Texas Instruments, Inc.**

**2006** HBM Stress of No-Connect IC Pins and Subsequent Arc-Over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed Neighbor Pins
**H. Kunz, C. Duvvury, J. Brodsky, P. Chakraborty, A. Jahanzeb, S. Marum, L. Ting, J. Schichl, Texas Instruments, Inc.**

**2007** CDM Peak Current Variations and Impact Upon CDM Performance Thresholds
**Agha Jahanzeb, Yen-Yi Lin, Steve Marum, Joe Schichl, Charvaka Duvvury**

**2008** HBM ESD Failures Caused by a Parasitic Pre-Discharge Current Spike
**Melanie Etherton, James Miller, Freescale Semiconductor, Inc.; Victor Axelrod, Haim Marom, Freescale Semiconductor Isreal; Tom Meuse, Thermo Fisher Scientific**

**2009** A DRC-based Check Tool for ESD Layout Verification
**T. Smedes, N. Trivedi, J. Fleurimont, A.J. Huitsing, P.C. de Jong, W. Scheucher, J. van Zwol, NXP Semiconductors**

**2010** The Relevance of Long-Duration TLP Stress on System Level ESD Design
**Gianluca Boselli, Akram Salman, Jonathan Brodsky, and Hans Kunz,**
**Texas Instruments, Inc.**