

ESD Open Forum

Conformity—2007
Provided by the ESD Association

Question: Does CDM have a defined Class Zero?

Answer: The CDM ANSI/ESDA standard [1 *STM-5.3.1 Charged Device Model (CDM)-Component Level*] does not have a defined class Zero (0), but the lowest class (C1 <125 volts) in the document, is being used (established or not) by the ESD community to represent class Zero. The C represents the fact that it is a CDM classification. The HBM ANSI/ESDA STM standard has a class Zero (0) which is specified as < 250 volts, but must not be equal to 250 volts, so be aware of the simple mathematical difference.

Question: What is the ESD Threshold Voltage for future electronic chips in terms of CDM?

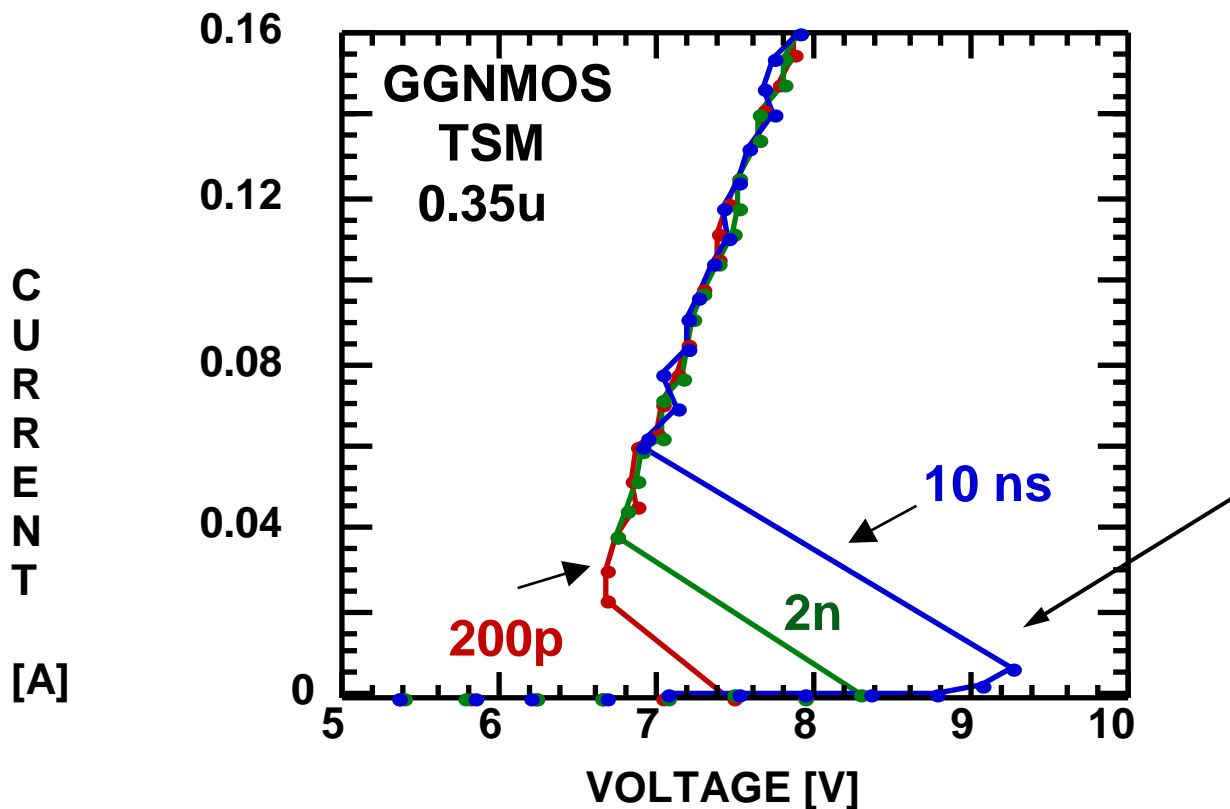
Answer: As you are aware, the consumers' insatiable desire to have things work faster and take up less space in turn forces manufacturers to require their design engineer to continuously improve their designs. So the smaller ESD protection feature sizes of the components, the circuits and the chips result in reduced ESD threshold susceptibility. The ESDA ESD Technology roadmap (www.esda.org) shows the device esd sensitivity trends from 1980 to 2010 for all three ESD models of HBM, MM and CDM. The table below taken from the roadmap shows what the roadmap predicts for CDM- by the year 2010. The worst case threshold will be down to 10Volts and possibly lower.

CDM ESD roadmap	Year 2000	Year 2005	Year 2010
Max V – the best	1000 V	800 V	600 V
Min-V – the worst	400 V	200 V	10 V

Question: For the case of CDM, if the industry expert says the future CDM threshold would be X voltage, then would it mean that when measured with a field voltage meter at 1 inch distance, the reading shown should be not more than the X value in order to prevent damage due to CDM?

Answer: Long question, but good question. This assumption is incorrect because firstly, the simple physics says that the voltage measured by the Field Voltage Meter (FVM) is not only proportional to the charge associated with the field that it is measuring, but is also indirectly proportional to the capacitance, which changes with distance. The 1 inch is for all intent and purposes an arbitrarily accepted number used in industry to gauge the approximate strength of a field, but not to be used for ESD device threshold measurements nor calculations which is an almost “exact” science. If you were to move the FVM further or closer (to the device in the field) than 1 inch, the measured voltage would change.

Secondly, the design strategy used by CDM ESD designers to protect their circuits from very fast transients (a combined $\ll 200$ pico-second rise time and $\ll 10$ nano-second pulse width) due to charge build up on the device bears little relationship mathematically to the actual field in which the device is placed. No correlation exists as yet. An empirical equation needs to be developed, and data collected or vice versa. The design focus is mostly on the transient behaviour of the protection structure. It is not only at what voltage will the ESD structure turn on, but also how fast must the transient be before the structure turns on. A simple look at the I-V curves (shown below) from a device stressed on a TLP Simulator/Tester shows that at different rise times (20.0 nsec , 2.0 nsec and 0.20 nsec), the turn on voltages are quite different.



Rise time dependent triggering behavior- Bart et al.

Question: CDM Failure is the future failure?

Answer: You are so correct that the World Council on ESD, a consortium of 18-20 of the top IC manufacturing companies in the world and 11 associate members, has made their general goal/mission to review the ESD robustness HBM, MM and CDM requirements of modern IC products for allowing safe handling and mounting in an ESD protected area.

Question: What type of industry would be much affected by CDM Failure in the future?

Answer: The storage industry (hard disk drive etc) has been impacted by this much lower level CDM ESD failure threshold for many years now, so their learning curve may be ahead of the electronics and flat panel industries, which include the medical products, the telecommunications products, the consumer electronics/products and the computer products etc etc.

References:

1. *ANSI/ESD STM-5.3.1-Charged Device Model (CDM)--Component Level*, ESD Association, Rome, NY.
2. ESDA ESD technology roadmap www.esda.org.

About the author

This article was prepared on behalf of the ESD Association by Dr. Leo G. Henry, an IEEE Senior member. He is a member of the ESDA's Board of Directors, with Chair responsibilities for the National ESD Symposium Workshop and the Device Design Certification Program. Dr. Henry is also chair/facilitator for the ESDA's Device Testing Standard Committee (WG-5.0) that has several subgroups (HBM, CDM, MM, HMM, TLU and TLP). Dr. Henry is presently the Chief Engineer at ESD/TLP Consultants LLC, located in Silicon Valley, Fremont, CA. LeoG has B.S. and M.S. degrees in Physics from the University of the West Indies, and M.S. & PhD degrees in Materials Science & Engineering from U.C. Berkeley, CA, USA. He can be reached at 510-657-5252 (office) or 510-708-5252 (Mobile) and at leogesd@pacbell.net or leogesd@ieee.org.

About the ESD Association

Founded in 1982, the ESDA is a not-for-profit, professional organization directed by volunteers dedicated to furthering the technology and understanding of electrostatic discharge. The Association sponsors education programs, develops ESD standards, holds an annual technical symposium, and fosters the exchange of technical information among its members and others. **Additional information may be obtained by contacting the ESD Association, 7900 Turin Rd., Bldg. 3, Rome, NY 13440-2069 USA. Phone: 315-339-6937. Fax: 315-339-6793. Email: info@esda.org. Website: www.esda.org.**