

# DEVICE DESIGN SEMINAR

## ON-CHIP ESD PROTECTION DESIGN OVERVIEW AND PRACTICAL EXAMPLES

**May 11, 2012**

Imec, Kapeldreef 75 B-3001, Heverlee, Belgium  
Lunch and refreshments provided

**MAY 11, 2012 • 9:00 AM - 6:00 PM (9:00 – 18:00)**

### On-Chip ESD Protection Design Overview and Practical Examples

Instructors: *Charvaka Duvvury, Texas Instruments; James W. Miller, Freescale Semiconductor*

Objective: The course objective is to give an overview about the importance of ESD to the electronics industry; review the protection design techniques based on device understanding and circuit performance impact, define options for protection designs, provide simulation methods, and summarize the state-of-the-art technology trends and the challenges for maintaining ESD reliability. Part I will establish the fundamental ESD aspects followed by an overview of ESD design techniques and device effects leading to the latest technologies. Part II will address more practical design methods with a focus on active rail clamp based ESD protection.

#### **Part I: 9:00 a.m. - 1:00 p.m. (9:00 - 13:00)**

Introduction to the ESD Phenomena  
ESD Control  
Test Methods  
Device Physics and Device Phenomenon  
Design Methods for on-Chip Protection  
Modeling and Simulation Approaches  
Impact from Sub-100nm Technologies  
High Speed Design Effects  
High Voltage and Analog Design Effects  
Sub-50nm Effects  
Component to System Level Protection  
ESD Roadmap

#### **Part II: 2:00 p.m. - 6:00 p.m. (14:00 - 18:00)**

Introduction to Different ESD Design Strategies  
Key Devices in the ESD Designer's Toolkit  
SPICE Compact Models for the ESD Devices  
MOSFET Rail Clamp ESD Protection  
ESD Hardening Fragile I/O Receivers and Drivers  
Advantages of Distributed Rail Clamp Networks  
Trigger Circuit Design  
Kit-Based Remote Clamp ESD Network Design Example  
Full Custom Distributed ESD Network Design Example  
ESD Protection Design for the IC Core Region

#### ABOUT THE INSTRUCTORS

**Charvaka Duvvury** is a Texas Instruments Fellow working in the Silicon Technology Development Group. His current work is on development and company wide support on ESD for the nanometer submicron CMOS technologies. Charvaka has made numerous international presentations on ESD phenomena and protection design. He received his Ph.D. in Engineering Science from the University of Toledo. After working as a Post-Doctoral Fellow in Physics at the University of Alberta in Canada, he joined Texas Instruments in 1977. He has published over 140 papers in technical journals and conferences and holds 70 patents. He has co-authored books on hot carriers, modeling of electrical overstress, and ESD reliability phenomena and protection design. (John Wiley & Sons, 1995, and 2nd Edition in 2002). He is a recipient of the Outstanding Contributions Award from the EOS/ESD Symposium (1990), Outstanding Mentor Award from the SRC (1994), numerous Best Paper and Best Presentation awards from the EOS/ESD Symposium. He has served as the General Chairman both in 1994 and in 2005. He has been a contributing Editor for the IEEE Transactions on Device and Materials Reliability (TDMR) from 2001-2011. Charvaka has been a member of the ESD Association Board of Directors since 1997, promoting university education and research in ESD. He is a co-chair of the Industry Council on ESD Target Levels. Charvaka is also a Fellow of the IEEE.

**James W. Miller** is a Distinguished Member of the Technical Staff in the Microcontroller Solutions Group at Freescale Semiconductor in Austin, Texas. He leads a team responsible for developing and deploying to products ESD and latch-up solutions in advanced CMOS technologies. Mr. Miller received the B.S. and M.S. degrees in Physics from Stephen F. Austin State University. He has served several years on the Technical Program Committees of the IRPS and the EOS/ESD Symposium. Jim is also a past General Chair and Technical Program Chair of the Integrated Reliability Workshop, and was a co-organizer of the similarly formatted International ESD Workshop. He has co-authored over 50 external papers, presentations and tutorials on ESD network design, transistor reliability, failure analysis and I/O physical architecture. He was a co-recipient of several EOS/ESD Symposium Best Paper and Best Presentation awards. Jim currently holds over two dozen patents, with several pending.



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Cancellation & refund requests will be honored if received in writing no later than March 27th 2012, and are subject to a \$50 fee. Any other approved dispositions will also be assessed a \$50 fee.

### Payment Information

Payment is required at time of registration. Only checks drawn in U.S. currency on a U.S. bank that is a member of the Federal Reserve will be accepted; make checks payable to ESD Association. Visa®, Mastercard®, and American Express® and Discover® are accepted.

Amount enclosed \$ \_\_\_\_\_  Check  Credit Card

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