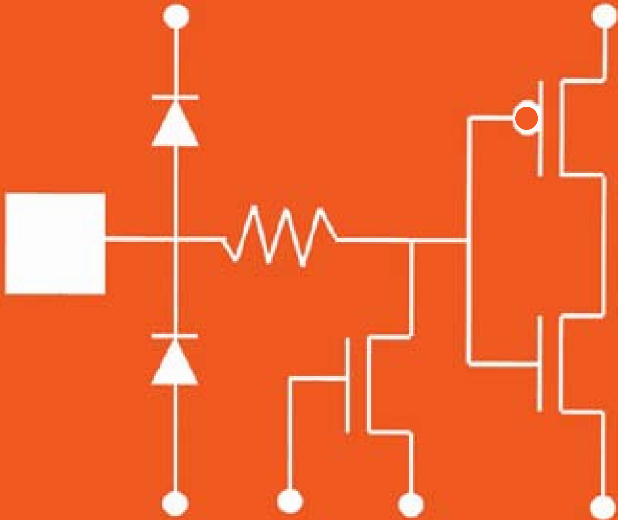
Device

Design

Certification



# ESD Device Design
## Professional

This twelve-course program provides the attendee with the information required to successfully participate in any ESD device protection design program. The student can take any one course, or all twelve courses, to broaden their capabilities in ESD design of device protection.

Upon completion of all twelve courses, and the successful completion of an exam, the attendee can also become an ESD Certified Professional in Device/Design from the ESD Association. Device Design ESD Professional Certification demonstrates knowledge, experience and competency in the area of ESD design for device protection.

As technology progresses to smaller features, the susceptibility to ESD increases so improved protection design requires engineers with up-to-date knowledge to maintain production yields at the highest levels. Taking the course will result in self-development, career advancement and potential employment opportunities.

ESD Device Design Certification designation was developed for individuals that are involved in designing, characterizing and implementing improved ESD protection designs. This end engineer should be able to demonstrate knowledge, experience and competency with ESD protection design.

The following Device Design (DD) courses are offered every year at Symposium and at other times throughout the year. An attendee may receive credit for having taken any of the required Device Design classes if the class was taken in 2003 or later. Included on the following pages are ESD Device Design course descriptions along with check boxes in the bottom right-hand corner. Use the check boxes to help you keep track of your course completion status. Additional information may be obtained at http://www.esda.org/device design.html.

# Course Listings

- ESD On-Chip Protection in Advanced Technologies* (full-day)
- System Level ESD/EMI: Testing to IEC and Other Standards (half-day)
- On-Chip ESD Protection in RF Technologies (half-day)
- SPICE-Based ESD Protection Design Utilizing Diodes and Active MOSFET Rail Clamp Circuits* (half-day)
- EOS/ESD Failure Models and Mechanisms* (half-day)
- Circuit Modeling and Simulation for On-Chip Protection (quarter-day)
- Latch-up D\mg]Wg UbX 8Yg][ b (quarter-day)
- Troubleshooting On-Chip ESD Failures (half-day)
- Transmission Line Pulse Measurements: Parametric Analyzer for ESD On-Chip Protection (quarter-day)
- 7 \Uf[ Y 8Yj ]WY A cXY` D\Ybca YbU UbX 8Yg][ b* (quarter-day)
- Impact of Technology Scaling on ESD High Current D\Ybca YbU UbX a d`]WUh]cbg Zcf Fc Vi gh 9G8 8Yg][ b (<U`Z-day)
- Device Testing--IC Component Level: HBM, CDM, MM, and TLP (half-day)

*** Please Note:** The ESD Association regularly offers (outside of the symposium) the Device/Design Seminar, a two-day course that fulfills the requirements for these classes.

**Also Note:** A student can complete the requirements in one to three years.

# ESD On-Chip Protection
## in Advanced Technologies

This tutorial addresses important issues in the design of IC protection circuits built with advanced deep sub-micron CMOS technologies, including silicon-on-insulator (SOI) and high voltage MOSFETs. The tutorial will present fundamental aspects of ESD protection design such as basic NMOS and SCR concepts, as well as gate-biased and substrate driven NMOS protection concepts. Protection design methods to meet the human body model (HBM), machine model (MM), and charged device model (CDM) will be presented. Other topics to be covered include BiCMOS protection circuits, mixed voltage protection, and compatibility to latch-up. Specific design examples will be presented to assist in understanding the methods for design synthesis. This tutorial is useful for design, device, process, product, failure analysis, and reliability engineers, and will assist those attending other design-related tutorials. Attendees should have a minimum knowledge of MOS device operation in integrated circuits.

## Learning Outcome

Participants who take this full-day tutorial will acquire a basic understanding of the nature of ESD as it applies to the various commonly used stress models of HBM, MM, and CDM. The tutorial most importantly enables the attendee to successfully recognize the various on-chip protection methods that one should implement based on the process technology and the particular circuit application. After completing the course the attendee should be able to formulate ESD protection strategy for a complete I/O chip and be able to champion as an ESD designer and build up his/her expertise in specific areas by choosing to attend some of the other specialized tutorials with the acquired background information from this class.

# System Level ESD/EMI:

## Testing to IEC and Other Standards

This tutorial is intended to help those tasked with testing products to IEC and other system level ESD standards by providing detailed information on IEC 61000-4-2, the most widely used standard, and highlighting the harmonization and differences between IEC, ANSI, Telcordia, and some automotive ESD standards. We will answer common questions regarding test setups, test points and procedures. Key issues will be addressed, including:

Differences between "verification" and "calibration" and when is each required; the influence of ESDA WG14.1 (TR) on IEC and how it affects the calibration; and verification procedures

Test set-up requirements, the test environment; ground connections and return paths and ground plane effects

Testing procedures with demonstration on actual products; how the tester affects test results; and problems with test result variations due to simulator influences

What points need to be tested and why; guidance on determining "operator accessible" points and ports; exempted points and ports; and what to do around connectors and connector pins

ANSI and other ESD Standards; the drive toward harmonization with IEC; why standards will probably never be the same as IEC; and the scope of different standards. The system level ESD tutorial will cover several facets of ESD as applied to electronic systems.

## Learning Outcome

Those attending this course will understand the requirements for system level ESD/EMI testing. This half-day course is intended to help those tasked with testing products to IEC and other system level ESD standards by providing detailed information on IEC 61000-4-2, the most widely used standard, and highlighting the harmonization and differences between IEC, ANSI, Telcordia, and some automotive ESD standards.

# On-Chip ESD Protection
## in RF Technologies

With the growth of high-speed telecommunications and wireless technology, it is increasingly important for engineers to understand the design of radio frequency (RF) applications and their sensitivity to electrostatic discharge (ESD) phenomena. In this tutorial, a new "RF ESD design discipline" is discussed, along with ESD protection in RF CMOS, RF LDMOS, BiCMOS Silicon Germanium, Gallium Arsenide technology and RF silicon on insulator (SOI) technology. The tutorial focuses on RF ESD testing, device physics, design layout, circuits and design systems. It provides information on RF ESD testing methodologies, RF degradation effects, and failure mechanisms for devices, circuits and systems. A clear insight into the design and co-synthesis of ESD circuits and RF technology for protection against electrical overstress (EOS) and ESD is presented. This course covers methods for co-synthesizing ESD networks for RF applications to achieve improved performance and ESD protection of semiconductor chips. Attendees will discuss RF ESD design methods for narrowband and broadband applications: capacitance load transformation, matching network co-synthesis, capacitance shunts, inductive shunts, impedance isolation, load cancellation methods, distributed loads, emitter degeneration, buffering and ballasting. In addition, RF ESD mixed-signal design integration and synthesis of digital, analog and RF circuitry is discussed. State-of-the-art examples of RF ESD design computer aided design (CAD) methodologies used today in the RF ESD design are discussed. Alternative off-chip protection methods and structures, such as spark gaps, FEDs, and transient suppression concepts being practiced today will be shown.

## Learning Outcome

Those attending this course will understand the RF ESD testing, RF ESD failure criteria, RF ESD design methods, RF ESD design synthesis, RF ESD circuits, and RF CAD design methodologies. The course will focus on RF CMOS, RF Silicon Germanium and RF Gallium Arsenide technology. This 3 hour course is intended to help those tasked with testing and designing of RF ESD devices.

# SPICE-Based Protection Design

## Utilizing Diodes & Active MOSFET Rail Clamp Circuits

Over the past 10 years, there has been a gradual revolution in the world of ESD design for advanced technology CMOS ICs. On-chip ESD networks built with non-snapback ESD devices and circuits, including simple forward biased diodes and active MOSFET rail clamp circuits have increasingly replaced once-prevalent networks built with snapback ESD devices, including avalanche-triggered lateral bipolar transistors and SCRs. Non-snapback devices enjoy several advantages in process portability, scalability, layout area and ease of compact modeling for circuit simulations in SPICE. In this tutorial we will explore, in turn, each of the key elements in typical active ESD networks including diodes, power busses, and active clamp devices with trigger circuits. We will also review approaches for ESD-hardening of the fragile output driver transistors. Next, a step-by-step methodology for SPICE-based ESD network design and optimization will be introduced. Finally, the flexibility of active ESD networks will be demonstrated in a wide range of IC application examples.

### Learning Outcome

Those attending this course will gain a good understanding of dual-diode and RC-triggered rail clamp-based ESD protection networks for advanced CMOS ICs. This half-day course is intended to provide a solid background in the required ESD devices and network design techniques. The student should leave this class with sufficient understanding to implement robust test structures and preliminary ESD protection networks.

# EOS/ESD Failure Models
## and Mechanisms

Failure criteria and failure models associated with semiconductor breakdown, dielectric breakdown, and metal failure will be discussed, associated with the semiconductor industry and nanostructures.

The tutorial will span from early CMOS technology, modern CMOS, to future CMOS concepts. The tutorial will address LOCOS-based CMOS, STI-based CMOS, to modern CMOS technology (strained Si, MUGFETs, and FINFETs). The failure mechanisms associated with each generation will be addressed. The tutorial will include many technology types - RF CMOS, Silicon Germanium (SiGe), Gallium Arsenide (GaAs), Gallium Nitride (GaN). In this way, the tutorial can address failure mechanisms that occur in RF technologies. The tutorial addresses a wide variety of semiconductors from lasers, to light emitting diodes (LEDs). ESD failure mechanisms will be discussed in magnetic recording (e.g. magneto-resistive (MR) heads, giant magneto-resistive head (GMR), to tunnelling magneto-resistive heads (TMR)). In micro-machines from ratcheted motors, to RF MEMs. In addition, the tutorial includes failure mechanisms associated with electrical overstress (EOS), and latch-up. The tutorial will draw distinctions among EOS, ESD and latch-up.

## Learning Outcome

Those attending this course will understand the fundamental failure mechanisms in CMOS and BiCMOS technology. The course will focus on CMOS, RF CMOS, SOI, and Bipolar technologies. This three-hour course is intended to help those tasked with testing, designing, and understanding failure mechanisms of semiconductor devices.

# Circuit Modeling
## & Simulation for On-Chip Protection

This tutorial addresses modeling and simulation of protection circuit elements and networks under ESD conditions. The high current characteristics and transient responses of devices typically used in ESD protection circuits will be presented. The objective is to ascertain what behaviors have to be captured in models intended for circuit-level simulation of ESD. Specific examples of model implementations will be provided. Parameter extraction and model scalability will be addressed. Thermal modeling will be discussed, as will the issue of modeling the off-state behavior of ESD protection devices. The tutorial assumes some familiarity with device physics and is directed toward persons with an interest in the transistor-level physics of ESD in on-chip protection circuits and in computer-aided design.

### Learning Outcome

Persons attending this course will learn how to characterize devices for ESD modeling purposes and to construct compact models of the device behavior under ESD conditions. They will obtain a good understanding of the trade-offs between model complexity and model accuracy. This course is intended for persons who wish to optimize the design of ESD protection networks using circuit simulation, and/or those who need to do co-design of ESD and active circuitry.

# Latch-up Physics and Design

Latch-up continues to be of interest today in advanced CMOS, mixed signal (MS) CMOS, RF CMOS, BiCMOS, and BiCMOS silicon germanium. The latch-up tutorial will provide a discussion on device-level latch-up physics, latch-up metrics and design criteria, latch-up test structures, test methods, latch-up measurement techniques, device-level CAD simulation, and new latch-up issues. Both internal and external latch-up phenomenon, as well as DC and transient latch-up, will be addressed. Latch-up structures, guard ring physics, and characterization will be discussed in depth. The tutorial will provide examples of discussion on latch-up device level simulation using latch-up scaling issues as examples. Semiconductor process sensitivities to shallow trench isolation (STI), silicides, retrograde n-wells, and p-wells in single-well and dual-well CMOS will be discussed. Latch-up process solutions, such as heavily doped buried layers (HDBL) and triple wells will be shown. Latch-up testing, characterization methods, and latch-up test standards will also be discussed. The tutorial will end with a discussion on state-of-the-art latch-up issues and characterization techniques and tools.

## Learning Outcome

Those attending this course will understand the fundamentals of CMOS latch-up. The course will focus on theory, test structures, application, experimental results, simulation and CAD design systems. Those attending will also understand the impact of design, semiconductor process and circuits on CMOS latch-up.

# Troubleshooting
## On-Chip ESD Failures

Diagnosing and fixing on-chip ESD product qualification failures can often be one of the more challenging aspects of work in ESD. The pressure to quickly find and correct an HBM/MM/CDM failure to qualify a product often compounds the inherent difficulty of troubleshooting. Experience diagnosing failures, though not desirable from a product qualification standpoint, can greatly improve troubleshooting skills. This tutorial will build troubleshooting experience and skills by presenting case studies of actual on-chip HBM failures in a workshop format. The evidence for each case will be revealed and the failure analyzed in the same manner as an actual failure. Participants will be led through and allowed to analyze each failure case, interacting with the instructor to determine its root cause and a solution. The tutorial will identify common concepts, methods, and tools useful in failure diagnosis. Participants should be familiar with CMOS technology, on-chip ESD breakdown phenomena, standard ESD protection circuits, and the HBM test procedure. Participants should also be acquainted with basic CMOS circuit design, should be able to read circuit diagrams, and should have a basic understanding of the function of I/O circuits.

### Learning Outcome

Participants in this tutorial will gain experience identifying the root cause for ESD product qualification failures through actively investigating real cases. Participants will understand the flow for a failure investigation, will practice reading functional schematics to see how ESD interacts with circuits, and will understand what kind of questions to ask to pinpoint the origin of a failure. In addition, the tutorial illustrates a variety of common pitfalls to avoid in I/O and ESD designs as well as the solutions to obtain robust ESD protection in each of the cases studied.

# Device Testing
## IC Component Level HBM, CDM, MM, and TLP

This tutorial addresses the basics of HBM, CDM, MM, and TLP ESD stress testing of the ESD protection structures of ICs. The differences among these models are emphasized and used to show how the different circuit parasities affect the waveforms from each model-type simulator. The importance of doing ESD testing as an integral part of a high-quality component development and qualification effort is stressed. This tutorial covers constant impedance and constant current TLP testing and the TLP I-V characteristic plots, including the snap-back trigger voltages and currents. The evolution of the leakage current as it relates to the failure point and comparisons and correlations between HBM and TLP testing are emphasized. Standards issues and test procedures, including some comparisons between the ESDA and JEDEC standards will be discussed.

### Learning Outcome

Those who take this course will understand the important differences among the four (HBM, MM, CDM, TLP) types of ESD device testing. They will understand the relationships among the  ESD models, the ESD testing and the related ESD standards. The course will teach why TLP ESD testing should be done before HBM, MM and CDM.  The course will also teach why TLP testing is a characterization tool/test compared to the qualification tests using HBM, MM and CDM.

# Transmission Line Pulse Measurements:

## Parametric Analyzer for ESD On-Chip Protection

The transmission line pulse (TLP) technique has often been called the parametric analyzer for on-chip ESD protection. The TLP system utilizes rectangular pulses at current levels and time scales similar to human body model (HBM) events. The rectangular pulse of a TLP system allows the measurement of current-voltage (I-V) curves from which can be extracted a variety of device and circuit parameters. These parameters cannot be measured with the double exponential pulse characteristic of HBM. This tutorial explores the parameters to be measured with a TLP system and discusses the importance of the parameters in the design of on-chip ESD protection circuits. Circuit elements and circuits that will be discussed include n and p MOS transistors, npn bipolar transistors, diodes, resistors, metal runners, power supply clamps, and even full integrated circuits. Also, variations in the test structure layouts, important for understanding the properties of the technology, will be discussed.

### Learning Outcome

Students will learn how to use TLP to understand the properties of integrated circuits and circuit elements in the time and current levels characteristic of ESD events. How TLP I-V curves are extracted from the voltage and current pulses captured by a TLP system will be covered. ESD relevant device parameters extracted from the TLP I-V curves are presented and related to their ESD importance. The importance of the voltage and current as a function of time during the TLP is also presented as well as the issues involved in extracting this data from the raw pulse data.

# Charged Device Model

## Phenomena and Design

This course teaches the basic concepts and ideas required to design-in for Charge Device Model ESD tests. The course will cover a brief history of CDM ESD development, charge and discharge physics, component level IC CDM testing, CDM failure mechanisms, CDM fast transient measurements, CDM circuit simulations, and CDM design-in strategies and characterization.

### Learning Outcome

The attendees of this introductory class will learn the basic ideas and concepts required to design-in for the Charge Device Model ESD discharge event. The student is expected to learn what is the most common CDM failure mechanism and should understand the fundamental properties of a good CDM ESD circuit. In addition, the student should comprehend the basic ideas that determine the different types of CDM circuit design-in strategies and techniques.

# Impact of Technology Scaling
## on ESD High Current Phenomena and Implications for Robust ESD Design

This advanced tutorial covers the impact of silicon technology scaling on ESD device behavior and on subsequent ESD protection design. The physics of CMOS components under high current conditions are discussed. Also, the technology trends for sub-100nm nodes and their implications for the ESD design window will be covered. Finally, sub-50nm technologies challenges will be discussed.

This class is intended for individuals who have taken the basic on-chip protection class and are familiar with the basic device physics for both ESD and latch-up.

### Learning Outcome

Those attending this course will understand the physics of basic ESD components under high current conditions with particular emphasis on the scaling aspects. This course will describe how to experimentally extract high current characteristics to optimize ESD protection circuits and increase the robustness of Input/Output buffers. Finally, the attendees will gain a perspective on ESD intrinsic robustness for future nanometer CMOS technologies.

# ESDA

Founded in 1982, the ESD Association is a not-for- profit, professional organization dedicated to furthering the technology and understanding of electrostatic discharge. The Association sponsors educational programs, develops ESD standards, holds an annual technical symposium, and fosters the exchange of technical information among its members and others.

# ESDA Roadmap

The ESD Association has developed an education program that will provide the ESD program manager with the knowledge to develop an effective control program.

Current advances in electronic device process speed and capability are dramatically outpacing the ability to design in ESD protection for the devices. Major device manufacturers are predicting that device sensitivities will fall well below the current threshold levels by the year 2010.

Companies involved in electronics manufacturing must be prepared to handle these devices or significant losses could occur. Strong understanding of the ESD control capability of the factory, will be required in order to maintain process yields in the near future.

The purpose of the Roadmap is to project the impact of technology scaling in the semiconductor industry.

To develop the Roadmap, ESD device and design experts collaborated from several major corporations. The projections they formulated are based on industry trends and technology constraints, and are not representative solely of the design methods used at their respective companies.

To download a pdf of the Technology Roadmap, visit www.esda.org.

# Benefits
## of ESDA Membership

www.esda.org

Membership in ESDA can provide numerous benefits that can assist in the advancement of your career. In addition to educational resources, membership provides access to a wide network of professional resources. Here are just a few of the benefits of membership:

- Global networking with experts in the field
- Discounted costs associated with tutorials, seminars, Standards and other technical publications
- Access to ESD industry technology
- Access to online, searchable Association membership roster
- Professional development
- Participation in local chapters, Standards development and other committees
- Option to purchase a listing in our bi-monthly newsletter, *Threshold*™, as well as a listing in our Product Service Directory at www.esda.org.

Visit www.esda.org for more information about the organization, and to download a membership application.

www.esda.org

ESD Association
7900 Turin Rd., Bldg. 3
Rome, NY 13440-2069 USA
www.esda.org
Phone: 315-339-6937
Fax: 315-339-6793

1/9/07