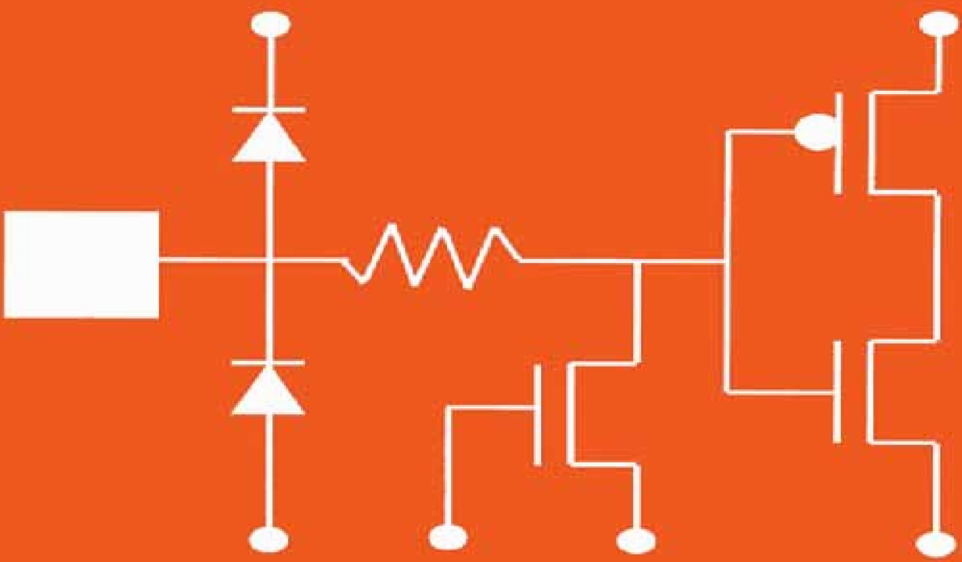
Device

Design

Certification

# The Route to Improved ESD Protection



# ESD Device Design
## Professional

This twelve-course program provides the attendee with the information required to successfully participate in any ESD device protection design program. The student can take any one course, or all twelve courses, to broaden their capabilities in ESD design of device protection.

Upon completion of all twelve courses, and the successful completion of an exam, the attendee can also become an ESD Certified Professional in Device/Design from the ESD Association. Device Design ESD Professional Certification demonstrates knowledge, experience and competency in the area of ESD design for device protection.

As technology progresses to smaller features, the susceptibility to ESD increases so improved protection design requires engineers with up-to-date knowledge to maintain production yields at the highest levels. Taking the course will result in self-development, career advancement and potential employment opportunities.

ESD Device Design Certification designation was developed for individuals that are involved in designing, characterizing and implementing improved ESD protection designs. This end engineer should be able to demonstrate knowledge, experience and competency with ESD protection design.

The following Device Design (DD) courses are offered every year at Symposium and at other times throughout the year. An attendee may receive credit for having taken any of the required Device Design classes if the class was taken in 2003 or later. Included on the following pages are ESD Device Design course descriptions along with check boxes in the bottom right-hand corner. Use the check boxes to help you keep track of your course completion status. Additional information may be obtained at http://www.esda.org/device design.html.

# Course Listings

1. ESD On-Chip Protection in Advanced Technologies: Part I + Part II* (2 half-day) (Previously one full-day course)

2. System Level ESD/EMI: Testing to IEC and Other Standards (half-day)

3. On-chip ESD Protection in RF Technologies (half-day)
   *or:* RF On-Chip ESD Protection Design and Test (half-day)

4. SPICE-Based ESD Protection Design Utilizing Diodes and Active MOSFET Rail Clamp Circuits* (half-day)

5. EOS/ESD Failure Models and Mechanisms* (half-day)

6. Empirical Models for Circuit Level Simulation of On-Chip Protection (quarter-day)
   *or:* Circuit Modeling and Simulation for On-Chip Protection (quarter-day)

7. Latch-up Physics and Design (quarter-day)

8. Troubleshooting On-Chip ESD Failures (half-day)

9. Transmission Line Pulse Measurements: Parametric Analyzer for ESD On-Chip Protection (quarter-day)

10. Charged Device Model Phenomena and Design* (quarter-day)
    *or:* CDM Design and Characterization (quarter-day)

11. Impact of Technology Scaling on ESD High Current Phenomena and Implications for Robust ESD Design (quarter-day)
    *or:* Impact of CMOS Technology Scaling on ESD High Current Phenomena (quarter-day)

12. Device Testing-Component Level: HBM, CDM, MM, and TLP (half-day)

* Please Note: The Device/Design Seminar, a two-day course fulfills the requirements for these classes.

Also Note: A student can complete the requirements in one to three years.

# ESD On-Chip Protection
## in Advanced Technologies: Part I + Part II

This tutorial, presented in two parts, addresses the important issues for understanding ESD and the design of IC protection circuits from basic to advanced deep sub-micron CMOS technologies. The complete tutorial should be useful for design, device, process, product, failure analysis, and reliability engineers and will assist those attending other design related tutorials. The attendee is exposed to all aspects of ESD protection designs from standard NMOS and SCR concepts to advanced designs with gate-biased and substrate driven NMOS protection techniques. Attendees should have a minimum knowledge of MOS device operation in integrated circuits. The overall tutorial also considers digital, analog, RF, and high speed I/O protection. Specific design examples will be presented to assist in understanding the methods for design synthesis. While Part I will be useful for attendees who expect to learn and understand about basic on-chip protection techniques and requirements, Part II (tutorial H) will delve into more advanced designs for high speed and complex I/O designs.

Part I: In the first part, the tutorial will present fundamentals of ESD, testing for ESD, latch-up phenomenon, and its interaction with ESD design. Understanding of protection design methods to meet the human body model (HBM) and the charged device model (CDM) will be presented. The purpose of the first part is to build a background for understanding ESD designs for advanced CMOS, analog, mixed voltage, and high voltage technologies.

Part II: In the second part, the tutorial will present the latest protection device techniques for system on chip (SOC) including the design with drain extended transistors (DENMOS). Several case studies will be presented to inform you about potential design errors. The tutorial will also cover the recent focus on system level ESD and protection strategy. Finally, the tutorial will examine the latest trends in technology scaling and the impact on the ESD roadmap.

**Learning Outcome**

Participants who take this full-day tutorial will acquire a basic understanding of the nature of ESD as it applies to the various commonly used stress models of HBM, MM, and CDM. The tutorial most importantly enables the attendee to successfully recognize the various onchip protection methods that one should implement based on the process technology and the particular circuit application. After completing the course the attendee should be able to formulate ESD protection strategy for a complete I/O chip and be able to champion as an ESD designer and build up his/her expertise in specific areas by choosing to attend some of the other specialized tutorials with the acquired background information from this class.

# System Level ESD/EMI:
## Testing to IEC and Other Standards

This tutorial is intended to help those tasked with testing products to IEC and other system level ESD standards by providing detailed information on IEC 61000-4-2, the most widely used standard, and highlighting the harmonization and differences among IEC, ANSI, Telcordia, and some automotive ESD standards. We will answer common questions regarding test set-ups, test points and procedures, and address key issues, including: 1) Differences between "verification" and "calibration" and when is each required; the influence of ESDA WG14 (TR) on IEC and how it affects the calibration and verification procedures. 2) Test set-up requirements, the test environment, ground connections, and return paths and ground plane effects. 3) Testing procedures with demonstration on actual products, how the tester affects test results, and problems with test result variations due to simulator influences. 4) What points need to be tested and why, guidance on determining "operator accessible" points and ports, exempted points and ports, and what to do around connectors and connector pins. 5) ANSI and other ESD standards, the drive toward harmonization with IEC, why standards will probably never be the same as IEC, and the scope of different standards. This system level ESD tutorial will cover several facets of ESD as applied to electronic systems.

### Learning Outcome

Those attending this course will understand the requirements for system level ESD/EMI testing. This half-day course is intended to help those tasked with testing products to IEC and other system level ESD standards by providing detailed information on IEC 61000-4-2, the most widely used standard, and highlighting the harmonization and differences between IEC, ANSI, Telcordia, and some automotive ESD standards.

# On-chip
## ESD Protection in RF Technologies
## *or:* RF On-Chip ESD Protection Design and Test

In this tutorial, electrostatic discharge (ESD) protection in both MOSFET- and bipolar-based radio frequency (RF) technologies is discussed. It covers ESD protection in RF CMOS, BiCMOS silicon germanium, gallium arsenide, and RF silicon-on-insulator (SOI). The tutorial will focus on how RF ESD design is distinct from digital CMOS ESD design. This tutorial will focus on device physics, technology, ESD layout design, ESD circuits, and design systems. It will present methods for co-synthesizing ESD networks for RF applications. The tutorial will provide examples of RF testing methodologies for ESD qualification of components and systems. HBM, MM, and TLP measurements of RF technologies will be provided. The tutorial will provide ESD input networks, differential pair networks, and ESD power clamps used in both RF CMOS and in RF BiCMOS technologies. The tutorial will also include automated cadence-based design methodologies for ESD-RF development.

**Learning Outcome**

Those attending this course will understand the RF ESD testing, RF ESD failure criteria, RF ESD design methods, RF ESD design synthesis, RF ESD circuits, and RF CAD design methodologies. The course will focus on RF CMOS, RF Silicon Germanium and RF Gallium Arsenide technology. This 3 hour course is intended to help those tasked with testing and designing of RF ESD devices.

# SPICE-Based ESD Protection Design Utilizing Diodes and Active MOSFET Rail Clamp Circuits

I/O ESD protection networks comprising dual diodes to the power/ground rails and networks of RC triggered active MOSFET rail clamp circuits have become prevalent in the industry for low voltage CMOS (<5 volt) process technologies. These networks have become popular because they offer clear advantages over prior ESD solutions in terms of fab portability, scalability, layout area, and ease of compact modeling for circuit simulations in SPICE. In this tutorial, we will explore in turn each of the key elements in active ESD networks including diodes, active clamp devices, and trigger circuits. We will cover in detail the important role that power rail resistance plays in determining the optimum size and placement of clamps in a protected bank of I/Os. We will review approaches for ESD-hardening of I/Os with more robust output driver configurations and secondary input protection circuits. Next, a step-by-step methodology for SPICE-based ESD network design and optimization will be introduced. Examples of this design methodology will be shown for both a “kit-based” and “full-custom” design approach. Finally, depending on time available, we will review a range of special topics including advantages in using isolated PWELL in ESD designs, HV and HV-tolerant network designs, and ESD networks for SOI technologies.

## Learning Outcome

Those attending this course will gain a good understanding of dual-diode and RC-triggered rail clampbased ESD protection networks for advanced CMOS ICs. This half-day course is intended to provide a solid background in the required ESD devices and network design techniques. The student should leave this class with sufficient understanding to implement robust test structures and preliminary ESD protection networks.

# EOS/ESD Failure Models
## and Mechanisms

Electrostatic discharge (ESD) failure mechanisms continue to impact semiconductor components and systems as technologies scale from micro- to nano-electronics.

This tutorial studies electrical overstress, ESD, and latch-up from a failure analysis and case-study approach. It provides a clear insight into the physics of failure from a generalist perspective, followed by investigation of failure mechanisms in specific technologies, circuits, and systems. The tutorial covers both the failure mechanism and the practical solutions to fix the problem from either a technology or circuit methodology.

**Learning Outcome**
Those attending this course will understand the fundamental failure mechanisms in CMOS and BiCMOS technology. The course will focus on CMOS, RF CMOS, SOI, and Bipolar technologies. This three-hour course is intended to help those tasked with testing, designing, and understanding failure mechanisms of semiconductor devices.

# Empirical Models
## for Circuit Level Simulation of On-Chip Protection
## *or:* Circuit Modeling and Simulation for On-Chip Protection

This tutorial addresses modeling and simulation of protection circuit elements and networks under ESD conditions. The high-current characteristics and transient responses of devices typically used in ESD protection circuits will be presented. The objective is to ascertain what behaviors have to be captured in models intended for circuit-level simulation of ESD. Specific examples of model implementations will be provided. Parameter extraction and model scalability will be addressed. Thermal modeling will be discussed, as will be the issue of modeling the off-state behavior of ESD protection devices. This tutorial assumes some familiarity with device physics. It is directed toward persons with an interest in the transistor-level physics of ESD in on-chip protection circuits and an interest in computer-aided design.

**Learning Outcome**

Persons attending this course will learn how to characterize devices for ESD modeling purposes and to construct compact models of the device behavior under ESD conditions. They will obtain a good understanding of the trade-offs between model complexity and model accuracy. This course is intended for persons who wish to optimize the design of ESD protection networks using circuit simulation, and/or those who need to do co-design of ESD and active circuitry.

# Latch-up
## Physics and Design

With the evolution and scaling of CMOS technology, CMOS latch-up has once again been an issue in semiconductor technology. With MOSFET scaling, high-level system-on-chip (SOC) integration, mixed signal and mixed voltage applications, high voltage CMOS (HVCMOS), power CMOS, RF CMOS, BiCMOS, auto industry and aero-space application marketplaces, CMOS latch-up has renewed interest. This tutorial provides a clear insight into the physics, technology and circuit issues with CMOS latch-up, as well as providing solutions and methodologies to provide protection from CMOS latch-up.

**Learning Outcome**

Those attending this course will understand the fundamentals of CMOS latch-up. The course will focus on theory, test structures, application, experimental results, simulation and CAD design systems. Those attending will also understand the impact of design, semiconductor process and circuits on CMOS latch-up.

# Troubleshooting
## On-Chip ESD Failures

Diagnosing and fixing on-chip ESD product qualification failures can often be one of the more challenging aspects of work in ESD. The pressure to quickly find and correct an HBM/MM/CDM failure in order to qualify a product often compounds the inherent difficulty of troubleshooting. Experience diagnosing failures, though not desirable from a product qualification standpoint, can greatly improve troubleshooting skills. This tutorial will build troubleshooting experience and skills by presenting case studies of actual on-chip HBM failures in a workshop format. The evidence for each case will be revealed and the failure analyzed in the same manner as an actual failure. Participants will be led through and allowed to analyze each failure case, interacting with the instructor to determine its root cause and a solution. This tutorial will identify common concepts, methods, and tools useful in failure diagnosis. Participants should be familiar with CMOS technology, on-chip ESD breakdown phenomena, standard ESD protection circuits, and the HBM test procedure. Participants should also be acquainted with basic CMOS circuit design, should be able to read circuit diagrams, and should have a basic understanding of the function of IO circuits.

### Learning Outcome

Participants in this tutorial will gain experience identifying the root cause for ESD product qualification failures through actively investigating real cases. Participants will understand the flow for a failure investigation, will practice reading functional schematics to see how ESD interacts with circuits, and will understand what kind of questions to ask to pinpoint the origin of a failure. In addition, the tutorial illustrates a variety of common pitfalls to avoid in I/O and ESD designs as well as the solutions to obtain robust ESD protection in each of the cases studied.

# Transmission Line Pulse Measurements: Parametric Analyzer for ESD On-Chip Protection

The transmission line pulse (TLP) technique has often been called the parametric analyzer for on-chip ESD protection. The TLP system utilizes rectangular pulses at current levels and time scales similar to human body model (HBM) events. The rectangular pulse of a TLP system allows the measurement of current-voltage (I-V) curves from which a variety of device and circuit parameters can be extracted. These parameters cannot be easily measured with the double exponential pulse characteristic of HBM. This tutorial will explore the parameters to be measured with a TLP system and discuss the importance of the parameters in the design of on-chip ESD protection circuits. Circuit elements and circuits that will be discussed include MOS transistors, diodes, oxides, metal runners, and power supply clamps. Variations in the test structure layouts and their importance during an ESD event will be examined. The extraction of time dependent properties from both standard 100 ns TLP and 5 ns VF-TLP will be covered, as well as how to perform TLP measurements on biased circuit elements. The importance of TLP source impedance on results will also be discussed.

### Learning Outcome

Students will learn how to use TLP to understand the properties of integrated circuits and circuit elements in the time and current levels characteristic of ESD events. How TLP I-V curves are extracted from the voltage and current pulses captured by a TLP system will be covered. ESD relevant device parameters extracted from the TLP I-V curves are presented and related to their ESD importance. The importance of the voltage and current as a function of time during the TLP is also presented as well as the issues involved in extracting this data from the raw pulse data.

# Charged Device Model

## Phenomena and Design

## *or:* CDM Design and Characterization

This course teaches the basic ESD circuit design concepts and ideas required to design-in for charge device model ESD tests. This course focuses on the following areas: 1) CDM failure mechanisms; 2) CDM protection circuit properties; 3) CDM basic design-in strategies; and 4) CDM cross power domain strategies. The goal of the class is to teach what types of circuits fail during a CDM discharge event and reviews the different types of ESD design circuit strategies that can be applied to protect those circuits.

### Learning Outcome

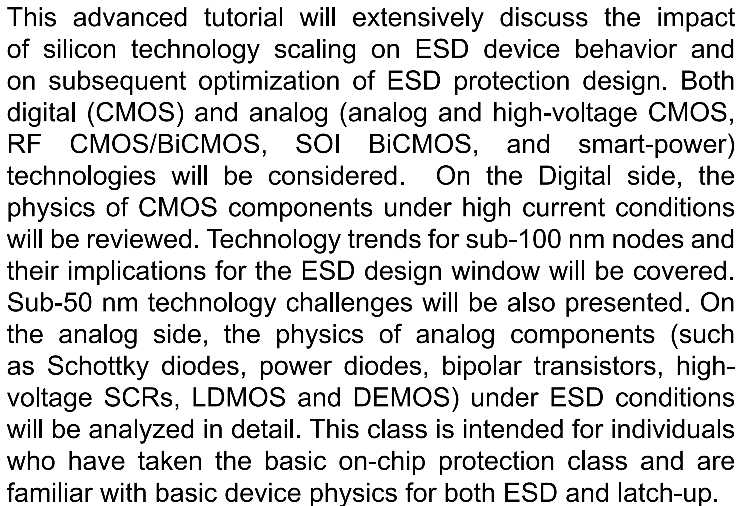
The attendees of this introductory class will learn the basic ideas and concepts required to design-in for the Charge Device Model ESD discharge event. The student is expected to learn what is the most common CDM failure mechanism and should understand the fundamental properties of a good CDM ESD circuit. In addition, the student should comprehend the basic ideas that determine the different types of CDM circuit design-in strategies and techniques.

# Impact of Technology Scaling

## on ESD High Current Phenomena and Implications for Robust ESD Design

## *or:* Impact of CMOS Technology Scaling on ESD High Current Phenomena

ESDA ROAD MAP


This advanced tutorial will extensively discuss the impact of silicon technology scaling on ESD device behavior and on subsequent optimization of ESD protection design. Both digital (CMOS) and analog (analog and high-voltage CMOS, RF CMOS/BiCMOS, SOI BiCMOS, and smart-power) technologies will be considered. On the Digital side, the physics of CMOS components under high current conditions will be reviewed. Technology trends for sub-100 nm nodes and their implications for the ESD design window will be covered. Sub-50 nm technology challenges will be also presented. On the analog side, the physics of analog components (such as Schottky diodes, power diodes, bipolar transistors, high-voltage SCRs, LDMOS and DEMOS) under ESD conditions will be analyzed in detail. This class is intended for individuals who have taken the basic on-chip protection class and are familiar with basic device physics for both ESD and latch-up.

**Learning Outcome**

Those attending this course will understand the physics of basic ESD components under high current conditions with particular emphasis on the scaling aspects. This course will describe how to experimentally extract high current characteristics to optimize ESD protection circuits and increase the robustness of Input/Output buffers. Finally, the attendees will gain a perspective on ESD intrinsic robustness for future nanometer CMOS technologies.

# Device Testing IC Component Level HBM, CDM, MM, and TLP

This tutorial addresses the basics of HBM, CDM, MM, and TLP ESD stress testing of the ESD protection structures of ICs. The differences among these models will be emphasized and then used to show how the different circuit parasitics affect the waveforms from each model-type simulator. The importance of doing ESD testing as an integral part of a high-quality component development and qualification efforts will be stressed. Since industry-wide TLP testing is fairly new, the tutorial will cover constant impedance and constant current TLP testing and also the TLP I-V-L characteristic plots including the snapback trigger voltages (Vt1) and currents (It1). The evolution of the leakage current (L) as it relates to the failure (It2) point will be emphasized, as well as the comparisons and correlations between HBM and TLP testing. Standards issues and test procedures will be discussed and some comparisons will be made between the ESDA and JEDEC ESD standards.

**Learning Outcome**

Those who take this course will understand the important differences among the four (HBM, MM, CDM, TLP) types of ESD device testing. They will understand the relationships among the ESD models, the ESD testing and the related ESD standards. The course will teach why TLP ESD testing should be done before HBM, MM and CDM. The course will also teach why TLP testing is a characterization tool/test compared to the qualification tests using HBM, MM and CDM.

# ESDA

## About the ESD Association

Founded in 1982, the ESD Association is a professional voluntary association dedicated to advancing the theory and practice of electrostatic discharge (ESD) avoidance. The Association is chartered to expand ESD awareness through standards development, educational programs, local chapters, publications, tutorials, certification, and symposia.