

ESD DEVICE DESIGN ESSENTIALS

June 7-8, 2012

DoubleTree Suites by Hilton Seattle Airport/Southcenter, Seattle, WA
Lunch and refreshments provided

ESD DEVICE DESIGN ESSENTIALS

JUNE 7-8, 2011

Instructors: Gianluca Boselli, Texas Instruments;
Michael G. Khazhinsky, Silicon Labs

This two-day seminar consists of concentrated versions of twelve ESDA tutorials which comprise the ESDA Device Design Certification Program.

- ESD On-Chip Protection in Advanced Technologies
- SPICE-Based ESD Protection Design Utilizing Diodes and Active MOSFET Rail Clamp Circuits
- EOS/ESD Failure Models and Mechanisms
- On-Chip ESD Protection in RF Technologies
- Charged Device Model Phenomena and Design
- Latch-up Physics and Design
- Circuit Modeling and Simulation for On-Chip Protection
- Troubleshooting On-Chip ESD Failures
- Device Testing--IC Component Level: HBM, CDM, MM, and TLP
- Impact of Technology Scaling on ESD High Current Phenomena and Implications for Robust ESD Design
- Transmission Line Pulse Measurements: Parametric Analyzer for ESD On-Chip Protection
- System Level ESD/EMI: Testing to IEC and other Standards

DAY 1 JUNE 7

PART I (10:00 AM- 1:00 PM)

This part reviews the fundamentals of ESD testing, high-current physics, and ESD modeling. The focus is on device-level (HBM, CDM, MM, TLP) and system level testing, impact of technology scaling on ESD high current phenomena, as well as circuit modeling and simulation for on-chip protection.

PART II (2:00 PM-6:00 PM)

The principles from part I are then applied to ESD Protection Design. This part describes ESD on-chip protection in advanced technologies, SPICE-based ESD protection design utilizing diodes, and active MOSFET rail clamp circuits.

DAY 2 JUNE 8

PART III (10:00 AM- 1:00 PM)

This part describes special ESD design cases, including Charged Device Model (CDM) phenomena and design, on-chip ESD protection in RF Technologies, and latch-up physics and design.

PART IV (2:00 PM-6:00 PM)

The final section discusses EOS/ESD failure models and mechanisms. The seminar concludes with practical examples for troubleshooting of on-chip ESD failures.

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ABOUT THE INSTRUCTORS

Gianluca Boselli completed his Master in EE at the University of Parma, Italy, in 1996. In 2001 he completed his Ph.D. at the University of Twente, The Netherlands. In 2001 he joined Texas Instruments, Dallas, Texas, where he focused on ESD and Latch-up development for advanced CMOS technologies. Recently his responsibilities extended into ESD development of Analog technologies. He authored several papers in the area of ESD and Latch-up. He presented his work at major conferences, including EOS/ESD Symposium, IEDM, and IRPS. He also presented several invited papers and/or tutorials at the EOS/ESD Symposium, IRPS, IEDM, ESREF and RCJ. Dr. Boselli has been the recipient of the "Best Paper Award" on behalf of Microelectronics Reliability Journal in 2000. He received "The Best Paper Award" at the EOS/ESD Symposium 2002. He also received the "The Best Presentation Award" at the EOS/ESD Symposium in 2002 and in 2006. Dr. Boselli is a member of ESD Association and an IEEE senior member. He is currently a member of the Board of Directors of the ESD Association, where he is the Symposium Business Unit Manager. Dr. Boselli serves on the TPC of the EOS/ESD Symposium, IRPS and ESREF. Dr. Boselli has served as TPC Chair at the EOS/ESD Symposium 2006, Vice-General Chair at the EOS/ESD Symposium 2007 and General Chair at the EOS/ESD Symposium 2008. Dr. Boselli holds fourteen patents with several pending. Dr. Boselli serves in the Editorial Board of the IEEE Transactions on Device and Materials Reliability (T-DMR).

Michael G. Khazhinsky is currently an ESD staff engineer/designer at Silicon Labs in Austin, Texas. Prior to joining Silicon Labs, he worked at Motorola and Freescale Semiconductors where he was in charge of the TCAD development for the new and emerging CMOS and NVM process technologies, as well as the development of ESD, latch-up and I/O physical architecture design solutions with a focus on SOI and ESD EDA. Michael earned the M.S. degrees in Electrical Engineering and Physics from Moscow State Institute of Electronic Engineering and the Ph.D. degree in Physics from Western Michigan University. Michael is a Senior Member of IEEE and a member of the ESD Association Board of Directors. Michael served as a member of the IRPS, IPFA and EOS/ESD Symposium Technical Program Committees, as well as a Workshop Chair and Technical Program Chair of EOS/ESD Symposium. He is currently on the Symposium Management Committee and is the General Chair of the 2012 EOS/ESD Symposium. Michael co-authored over 30 external papers and gave a number of invited talks on ESD, process/device TCAD, and photonic crystals. He was a co-recipient of six EOS/ESD Symposium and SOI Symposium "Best Paper" and "Best Presentation" awards. Michael currently holds fifteen patents on ESD design, with additional patents pending.

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REGISTER ONLINE AT WWW.ESDA.ORG

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	Cost before 5/4/12		Cost after 5/4/12	
	Members	Non-Members	Members	Non-Members
Essentials 2 Day Seminar	\$1,510	\$1,610	\$1,710	\$1,710

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online at
www.esda.org

Cancellation & refund requests will be honored if received in writing no later than May 4th 2012, and are subject to a \$50 fee. Any other approved dispositions will also be assessed a \$50 fee.

Payment Information

Payment is required at time of registration. Only checks drawn in U.S. currency on a U.S. bank that is a member of the Federal Reserve will be accepted; make checks payable to ESD Association. Visa®, Mastercard®, and American Express® and Discover® are accepted.

Amount enclosed \$ _____ Check Credit Card

Credit card type: Visa® Mastercard® American Express® Discover®

Credit card number: _____ Expiration date: _____

Name on card: _____ Security code: _____

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Accommodations:

DoubleTree Suites by Hilton Seattle Airport - Southcenter
16500 Southcenter Parkway Seattle, WA 98188
Tel: 1-206-575-8220 • Fax: 1-206-575-4743
www.Seattle.DoubleTree.com

Mention ESDA for
Hotel rate \$129 per night
<http://esda.org/calendar.html>

Note: This is not the hotel at the airport, but rather three miles away.

ESD Association • 7900 Turin Rd Bld 3 • Rome NY 13440
Phone 315-339-6937 • Fax 315-339-6793 • info@esda.org • www.esda.org

