

## **EOS/ESD Symposium Best Paper Awards**

### **1979**

O. McAteer  
An Effective ESD Awareness Program

### **1980 Tie**

J. Keller Protection of MOS Integrated Circuits From Destruction By Electrostatic Discharge	S. Halperin Facility Evaluation Isolating Environmental ESD Problems
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### **1981**

B. Unger, R. Chemelli  
P. Bossart, M. Hudock  
Evaluation of Integrated Circuit Shipping Tubes

### **1982**

O. McAteer, R. Twist, R. Walker  
Latent ESD Failures

### **1983**

R. Enoch, R. Shaw, R. Taylor  
ESD Sensitivity of NMOS LSI Circuits and Their Failure Characteristics

### **1984**

L. DeChiaro  
Device Susceptibility Testing and Design Hardening

### **1985**

D. Pierce  
Electro-Thermomigration as an Electrical Overstress Failure Mechanism

### **1986 Tie**

A. Rubalcava, D. Stunkard, W. Roesch Electrostatic Discharge Effects on Gallium Arsenide Integrated Circuits	T. Maloney Contact Injection: A Major Cause of ESD Failure in Integrated Circuits
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### **1987 Tie**

E. Lai, J. Plaster ESD Control in the Automotive Electronics Industry A Case Study	Y. Fong, C. Hu The Effects of High Field Transients on thin Gate Oxide MOSFETS
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### **1988 TIE**

C. Duvvury, R. Rountree Output ESD Protection Techniques for Advanced CMOS Process	R. Renninger, D. Lin, M. Jon, T. Diep, T. Welsher A Microwave Bandwidth Waveform Monitor for Charged- Device Model Simulators
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### **1989**

R. Renninger, M. Jon D. Lin, T. Diep, T. Welsher  
A Field-Induced Charged Device Model Simulator

### **1990**

T. Maloney  
Enhanced P+ Substrate Tap Conductance in the Presence of NPN Snapback

**1991**

R. Renninger  
Mechanisms Of Charged- Device Electrostatic Discharges

**1992**

K. Bock, H. Hartnagel Circuits for High-Frequency Devices Fieldemitter-Based ESD-Protection and IC's

**1993**

K. Verhaege, P. Roussel, G. Groeseneken, H. Maes, H. Gieser, C. Russ, P. Egger, X. Guggenmos, F. Kuper  
Analysis of HBM ESD Testers and Specifications Using a 4th Order Lumped Element Model

**1994 TIE**

A. Amerasekera, C. Duvvury  
The Impact of Technology Scaling on  
ESD Robustness and Protection  
Circuit Design

M. Chaine, C. Liang, H. San  
A Correlation Study Between Different  
Types of CDM Testers and "REAL"  
Manufacturing In-Line leakage Failures

**1995**

A. Wallash, T. Hughbanks, S. Voldman  
ESD Failure Mechanisms of Inductive and Magnetoresistive Recording Heads

**1996**

H. Gieser, M. Haunschild  
Very-Fast Transmission Line Pulsing of Integrated Structures and the Charged Device Model Submicron  
CMOS Processes

**1997**

J. Chen, A. Amerasekera, C. Duvvury  
Design Methodology for Optimizing Gate Driven ESD Protection Circuits in Submicron CMOS processes  
***Presented in 98, photo in 1999 Proceedings***

**1998**

V. Gupta, A. Amerasekera, S. Ramaswamy, A. Tsao  
ESD-related Process Effects in Mixed-Voltage Sub- 0.5µm Technologies  
***Presented in 99, photo in 2000 Proceedings***

**1999**

J. Smith  
An Anti-Snapback Circuit Technique for Inhibiting Parasitic Bipolar Conduction During EOS/ESD Events  
***Presented in 00, photo in 2001 Proceedings***

**2000**

J. Miller, M. Khazinsky, J. Weldon  
Engineering the Cascoded NMOS Output Buffer for Maximum V<sub>t1</sub>  
***Presented in 01, photo in 2002 Proceedings***

**2001**

C. Torres, J. W. Miller, M. Stockinger, M. D. Akers, M. G. Khazinsky, J. C. Weldon  
Modular, Portable, and Easily Simulated ESD Protection Networks for Advanced CMOS Technologies  
***Presented in 02, photo in 2003 Proceedings***

**2002**

G. Boselli, C. Duvvury, V. Reddy, Texas Instruments Inc.  
Efficient pnp Characteristics of pMOS Transistors in Sub-0.13  $\mu\text{m}$  ESD Protection Circuits  
***Presented in 03, photo in 2004 Proceedings***

**2003**

M. Stockinger, J. W. Miller, M. G. Khazhinsky, C. A. Torres, J. C. Weldon, B. D. Preble, M. J. Bayer, M. Akers, Motorola; V. G. Kamat, Synopsis, Inc.  
Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies  
***Presented in 04, photo in 2005 Proceedings***

**2004**

M. G. Khazhinsky, J. W. Miller, M. Stockinger, J. C. Weldon; Freescale Semiconductor, Inc.  
Engineering Single NMOS and PMOS Output Buffers for Maximum Failure Voltage in Advanced CMOS Technologies  
***Presented in 05, photo in 2006 Proceedings***

**2005**

ESD Evaluation of the Emerging MuGFET Technology  
C. Russ, H. Gossner, T. Schulz, N. Chaudhary, K. Schroefer, Infineon Technologies;  
W. Xiong, A. Marshall, C. Duvvury, C. R. Cleavelin, Texas Instruments  
***Presented in 06, photo in 2007 Proceedings***

**2006**

*Ultra-thin Gate Oxide Reliability in the ESD Time Domain*  
A. Ille, Infineon Technologies and Université de Provence-ISEN; W. Stadler, A. Kerber, T. Pompl, T. Brodbeck, K. Esmark, Infineon Technologies; A. Bravaix, Université de Provence-ISEN  
***Presented in 07, photo in 2008 Proceedings***

**2007**

*Harmful Voltage Overshoots Due to Turn-On Behaviour of ESD Protections During Fast Transients*  
T. Smedes, N. Guitard, NXP Semiconductors  
***Presented in 08, photo in 2009 Proceedings***

**2008**

*A study of Term Pulses and Cabled MR Sensors*  
Icko Eric Timothy Iben, IBM  
***Presented in 09, photo in 2010 Proceedings***

**2009**

*Characterization and Simulation of Real-World Cable Discharge Events*  
Wolfgang Stadler, Tilo Brodbeck, Josef Niemeshheim, Reinhold Gaertner, Infineon Technologies; Kathleen Muhonen, Penn State College, The Behrend College  
***Presented in 10, photo in 2011 Proceedings***

**2010**

*On the Dynamic Destruction of LDMOS Transistors beyond Voltage Overshoots in High Voltage ESD*  
Yiqun Cao, Ulrich Glaser, Joost Willemsen, Stephan Frei, and Matthias Stecher, Infineon Technologies, and Technische Universität Dortmund  
***Presented in 11, photo in 2012 Proceedings***